



CORA-MBAD FOR ZYNQ 7000

MODEL BASED DEFINITION AND IMPLEMENTATION OF
RECONFIGURABLE COTS AVIONICS

MBSE2020

September 2020

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European Space Agency



CORA-MBAD FOR ZYNQ 7000

MODEL BASED DEFINITION AND IMPLEMENTATION OF RECONFIGURABLE COTS AVIONICS

•*Duration:* ~10 months

•*Prime:* GMV ES

•*Main Objectives:*

1. Provide functionality to easily deploy functional blocks in either HW or SW implementations, from identical source models
2. Follow a model-based approach
3. Achieve a high degree of toolchain automation (e.g. via code generation)
4. Support a ZynQ 7000 SoC target
5. Address representative use case

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OBJECTIVES

CORA-MBAD FOR ZYNQ 7000 OBJECTIVES

CoRA-MBAD “Compact Reconfigurable Avionics - Model Based Avionics Design”

HW/SW co-design toolchain providing functionality to easily deploy functional blocks in either HW or SW implementations, from identical source models.

TASTE + GR740 + BRAVE medium FPGA

CoRA-MBAD for ZynQ 7000

Adapt said toolchain to a ZynQ 7000 SoC target, motivated by low-cost missions that will use platforms based on COTS.

TASTE + Xilinx SoC (ARM + large FPGA)

CORA-MBAD FOR ZYNQ 7000 OBJECTIVES

To switch between HW and SW forms, the toolchain implements the **automatic transformation** of C source code (whether manually written or generated by a code generator like those in Matlab/Simulink) into Hardware (VHDL) source files.

To perform an automatic generation of the needed **consistent communication interfaces** supporting the exchange of commands and data between functional blocks executed on the processing system (PS) and on the programmable logic (PL) sides of the Xilinx SoC.



Xilinx Zynq-7000 SoC ZC706 Evaluation Kit

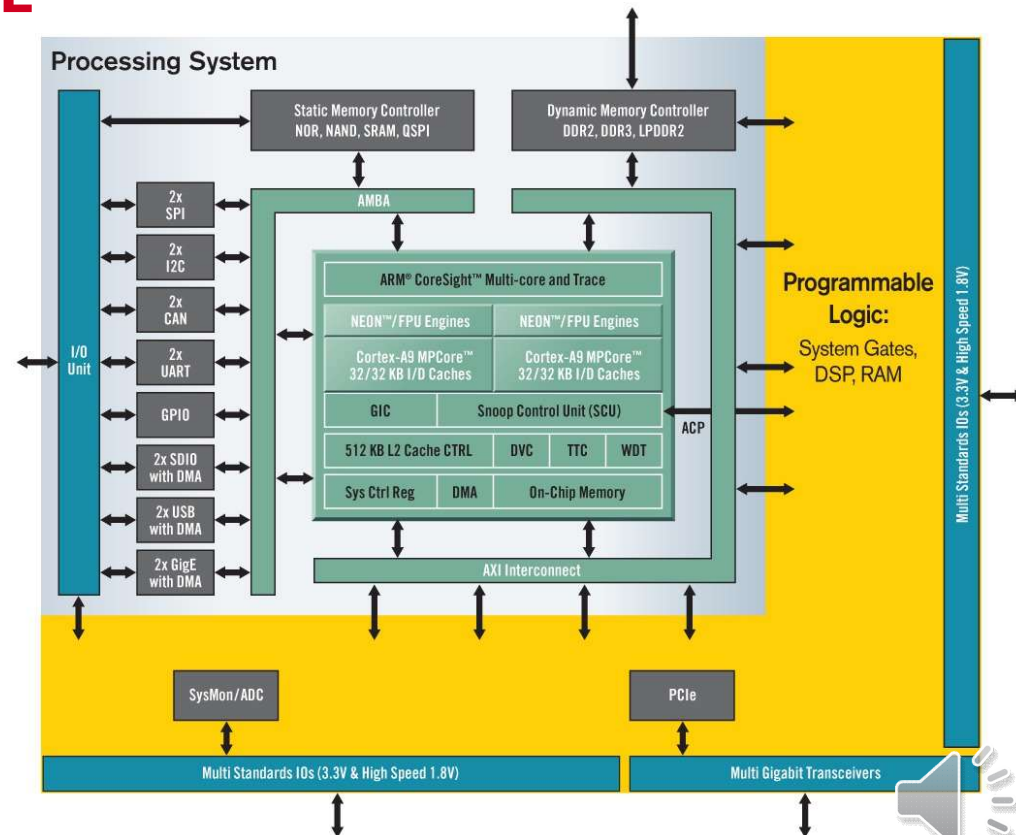
- PS: Dual ARM Cortex-A9 core processors
- PL: Artix-7 FPGA
- 1 GB of embedded DDR3 memory
- Transceivers
- FMC connector
- PCI Express, Ethernet, general purpose IO and UART interfaces

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ZYNQ-7000 ARCHITECTURE

SoC with programmable hardware and software parts

- Allow implement hardware/software co-design in a single device
- AMBA AXI interfaces between PS and PL
- 32 or 64 bits high bandwidth communication between PS and PL
- 32 or 64 bits direct high bandwidth communication between DDR3 memory controller and PL
- Specific low bandwidth and complexity communication with AXI_LITE (very useful for control registers)



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TASTE provides heterogeneous application level modelling and implementation facilities, and importantly transparent and robust middleware level automation capabilities, in particular for communication aspects.

<https://taste.tools>



Hands-on videos: Simulink

A nice way to see what TASTE does, is to watch it applied hands-on, in building an application from scratch.

In this video, you'll see it being used to automatically integrate C code with a Simulink design.

Hands-on videos: FPGAs

This video showcases how TASTE automatically creates device drivers and VHDL skeletons for the HW parts of a system.



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The toolchain was adapted to leverage the latest TASTE enhancements: The **TASTE's Kazoo** tool was adapted to build the modelled systems with significantly increased build performance, especially in rebuilds. It efficiently produces derived models, code and scripts using AdaCore's "templates-parser" for templates processing and files generation.

TASTE's Kazoo allows for simple expansion and update of the supported targets.

<http://taste.tuxfamily.org/wiki/index.php?title=Kazoo>

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Basic usage

Kazoo is integrated in TASTE as one of the main tools for generating and building the code of the system under development. The calls to kazoo are normally a project using Kazoo, user normally run a single command:

```
$ taste
```

If user would like to use kazoo directly, or tweak it's behaviour, the following example Makefile presents the calls to kazoo that generate the code skeletons and

```
KAZOO?=kazoo

all: c

c: work/glue_built
  $(MAKE) -C work

skeletons: InterfaceView.aadl DataView.aadl
  $(KAZOO) --gw -o work
  $(MAKE) -C work dataview

work/glue_built: InterfaceView.aadl DeploymentView.aadl DataView.aadl
  $(KAZOO) -p --glue --gw -o work
  touch work/glue_built

clean:
  $(MAKE) -C work clean

.PHONY: clean skeletons c
```

Kazoo will read the default input AADL models and generate code to the selected output directory. Parameter `--output` chooses the output directory for generation, `--glue` enables glue code generation and `-p` or `--polyorb-hi-c` turns on use of PolyORB-Hi-C runtime.

In the result directory `work` will be created and filled with generated models and source files.

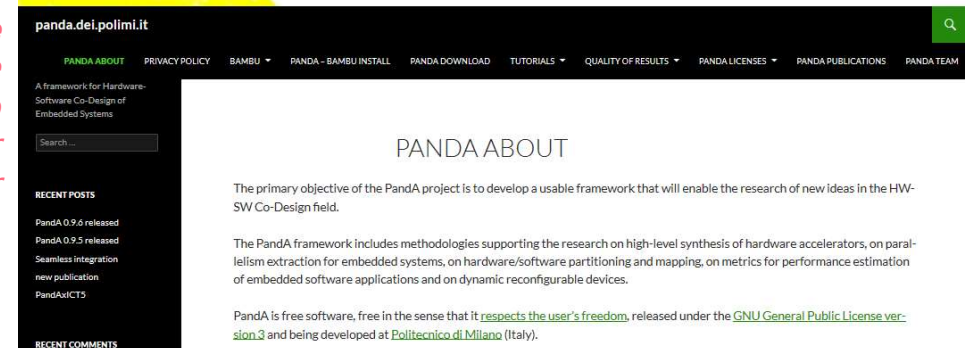


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For Matlab/Simulink models, the MBAD System relies on model-to-code transformation performed by MathWorks **Embedded Coder** and on high-level synthesis of C code performed by **Bambu**.

*Note that both **TASTE** and **Bambu** are open-source SW tools, so subsystems built in pure C can be synthesized and executed on the FPGA with no external dependencies. Bambu is FPGA vendor independent, hence it can be used with minor adaptations needed for each FPGA specific component.*

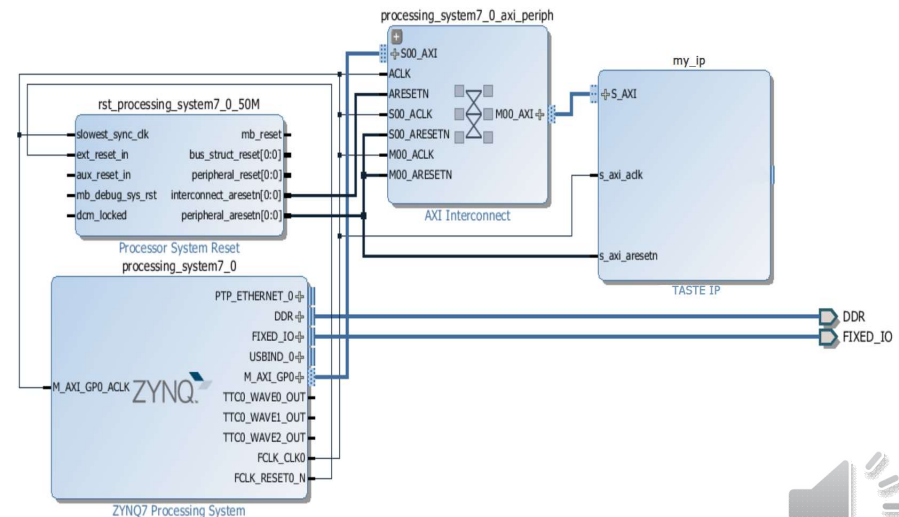
<https://www.mathworks.com/products/embedded-coder.html>
<https://panda.dei.polimi.it/>



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Vivado is an EDA (Electronic Design Automation) tool for FPGA and SoC, developed by Xilinx, with capabilities for low and high level synthesis, bitstream generation, timing analysis, simulation, etc.

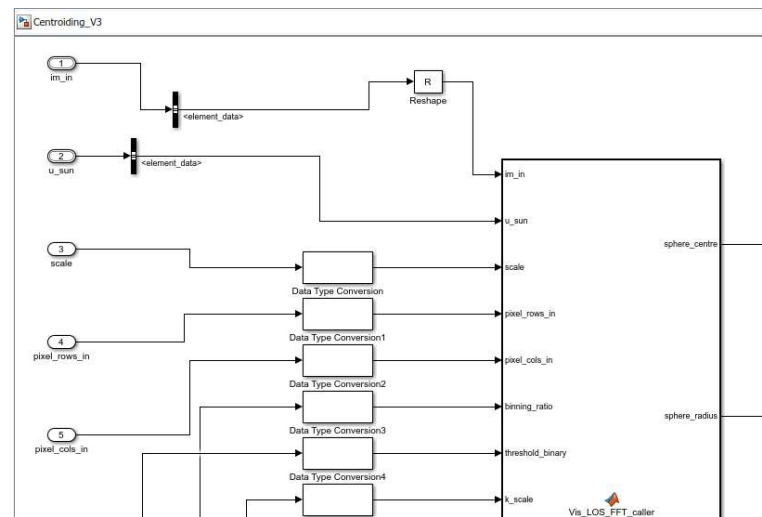
<https://www.xilinx.com/products/design-tools/vivado.html>



CORA-MBAD FOR ZYNQ 7000 TOOLING

Matlab Simulink commonly used by domain engineers to design dynamic systems, e.g. the control and guidance of satellites designed by a GNC team, producing cyclically actuation data from sensor data, are best modelled with mathematics, data flows or functional models. This environment is extensible to e.g. incorporate as well autocoding facilities such as Embedded Coder.

<https://www.mathworks.com/products/simulink.html>

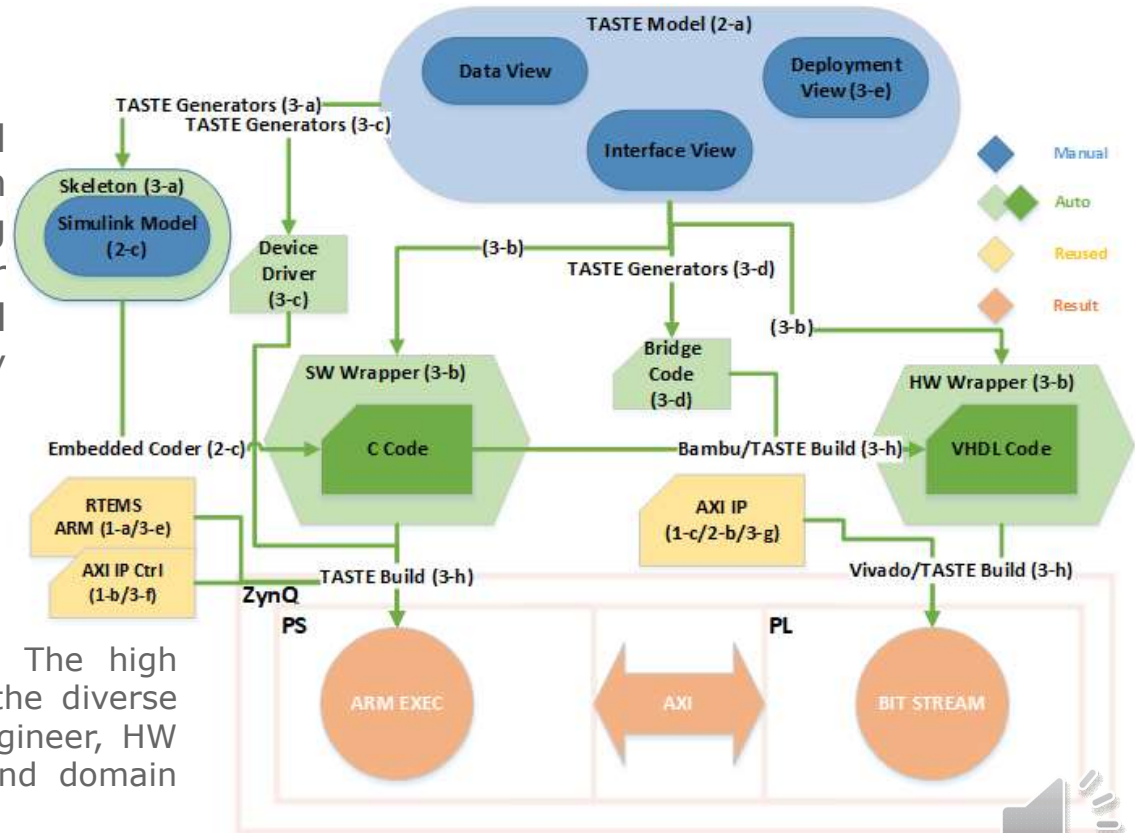


TOOLING

A **pivot open toolchain** gluing all elements together: **TASTE**, being an open framework targeting heterogeneous systems, is particularly suitable to **integrate and orchestrate** all the other necessary elements.



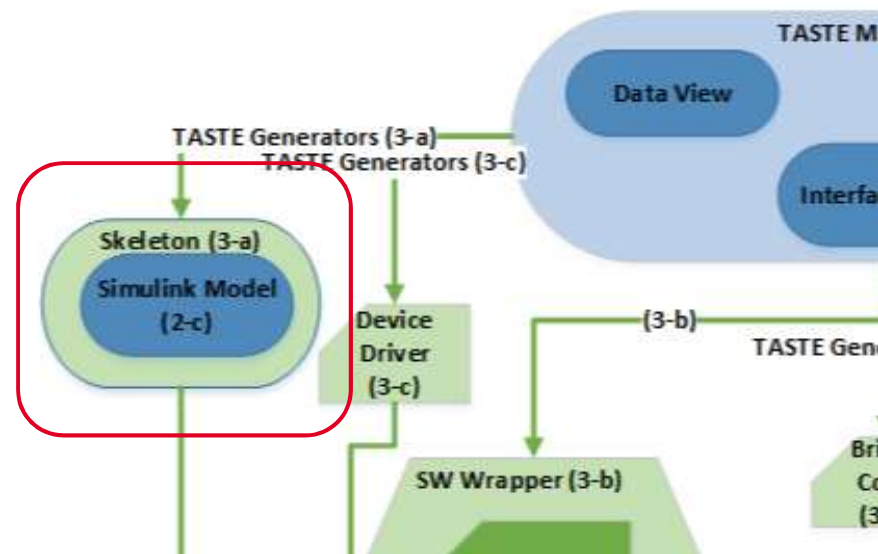
Multifaceted team in co-engineering: The high technical degree of the activity required the diverse skills and close collaboration of a: SW engineer, HW engineer, design environment engineer, and domain engineer.



CORA-MBAD FOR ZYNQ 7000 TOOLING

From a common ASN.1 data model and an AADL minimalistic component interface model it consistently and automatically exports:

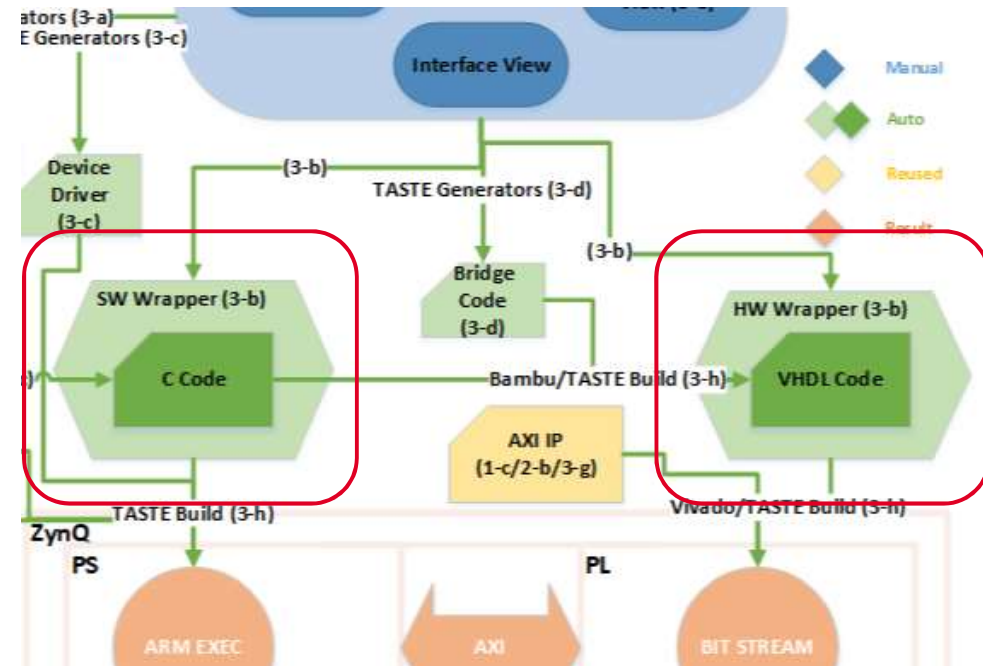
- **Interface definition** in the target language of choice with consistent inputs and outputs (in our demonstrator a Simulink model)



CORA-MBAD FOR ZYNQ 7000 TOOLING

From a common ASN.1 data model and an AADL minimalistic component interface model it consistently and automatically exports:

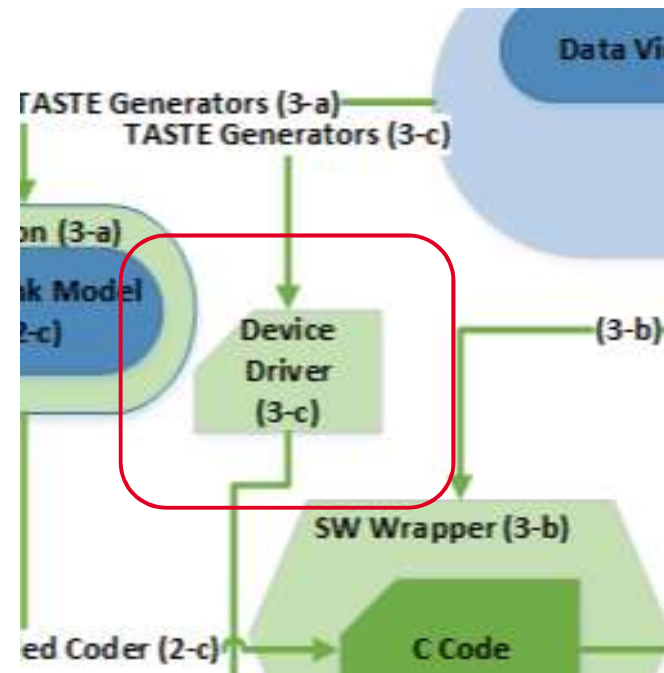
- **SW and HW wrapper** interface code that transparently guarantees the correct communication between the target's functions. Importantly these interface wrappers automatically grow or shrink according to the number and type of inputs and outputs.



CORA-MBAD FOR ZYNQ 7000 TOOLING

From a common ASN.1 data model and an AADL minimalistic component interface model it consistently and automatically exports:

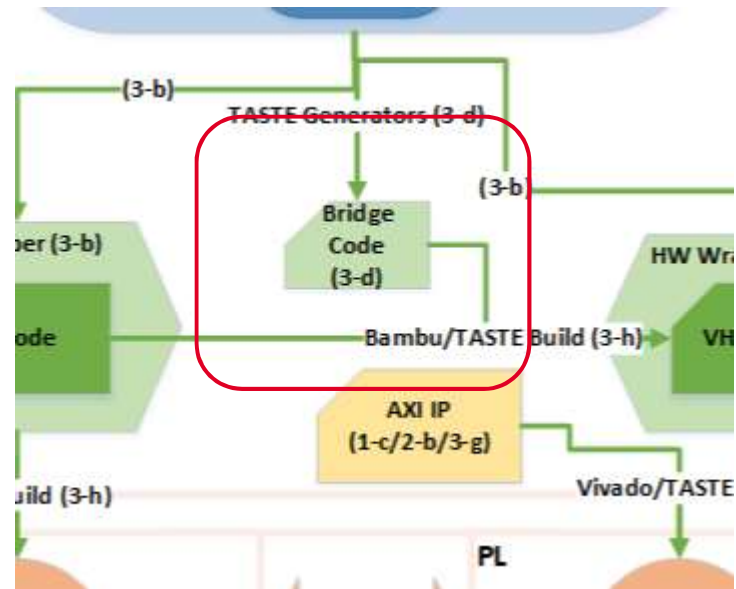
- **SW device driver** to provide SW-HW communication with the HW implementation of the target function.



CORA-MBAD FOR ZYNQ 7000 TOOLING

From a common ASN.1 data model and an AADL minimalistic component interface model it consistently and automatically exports:

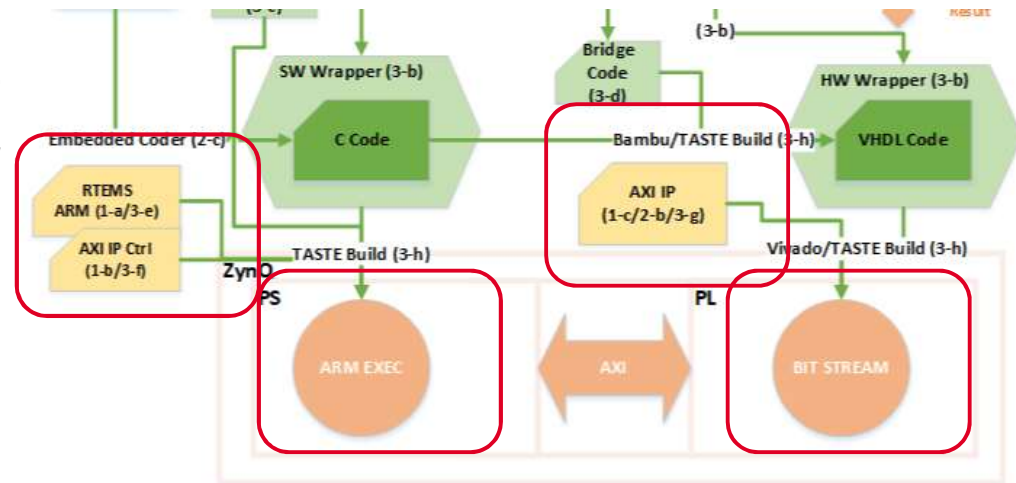
- **"Bridge" code** with the necessary adaptations and extra inputs needed in the transition between two autocoding tools, in this case between Embedded Coder and Bambu.



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Additionally, TASTE:

- integrates the custom **cross-compiler** as part of a new deployment target
- links with the **BSP** to use the necessary **HW drivers**
- orchestrates the calls to all needed **autocode and compilation tooling** - e.g. forwarding the Embedded Coder output as a Bambu input together with the generated consistent bridge
- calls the **synthesis, placement and routing** facilities of Vivado and generates FPGA bitfiles



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ARM SUPPORT

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CORA-MBAD FOR ZYNQ 7000 ARM SUPPORT

Support for the **ARM Cortex A9** development toolchain (RTEMS ARM support)

The **RTEMS 5.1** custom built cross compiler for ARM Cortex A9, equipped with the needed BSPs and validated on target. Testing revealed timing issues, so **BSP customization** had to take place to properly configure clock frequency.

<https://lists.rtems.org>
<https://www.rtems.org/>



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ARM/FPGA COMMUNICATION SUPPORT

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ARM/FPGA COMMUNICATION SUPPORT

Support for the **Advanced eXtensible Interface (AXI)** communication interface for on-chip communication.

(SW) AXI IP core control driver providing the necessarily interface configuration, initialization and read/write access to the SW applications.

Support for the **Xilinx FPGA** development toolchain (**Vivado**)

(HW) An AXI interconnect IP Core to manage and connect the AXI ports in the PS with the AXI ports of each of the modules/IPs implemented in the PL. At the same time, an AXI DMA IP controller to manage stream data transmissions between PS and PL.



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ARM/FPGA COMMUNICATION SUPPORT

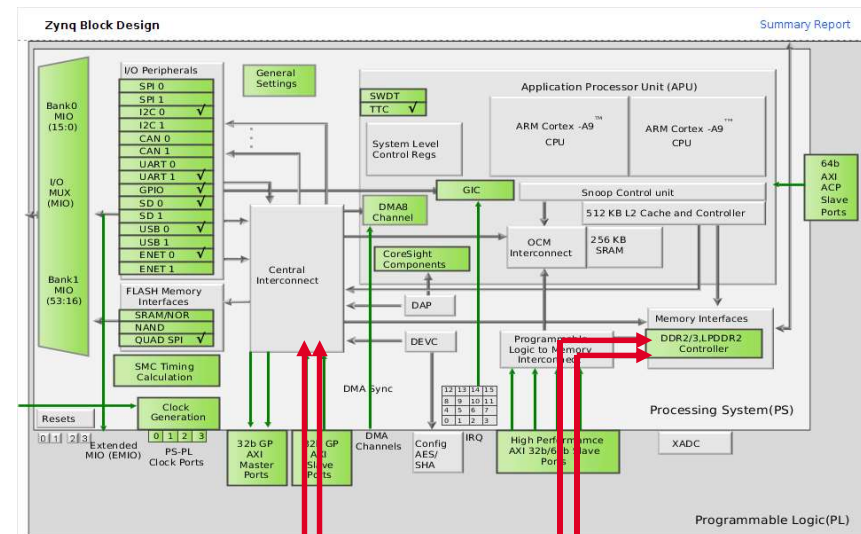
CoRA-ZynQ makes use of AXI bridges of Zynq-7000 architecture to connect PS with PL.

Three independent interfaces are implemented in order to provide different capabilities:

- one AXI interface used to write and read configuration registers
- one AXI interface fully devoted to write and read large blocks of memory inside FPGA
- one AXI stream interface to support stream data processing

The number of registers or memories addressed through AXI interfaces can be configured to optimize the resource allocation of the FPGA.

In addition, AXI stream transmission can be directed to achieve up to 32 different destinations through the same interface.



TASTE WRAPPER

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CORA-MBAD FOR ZYNQ 7000 USE CASES

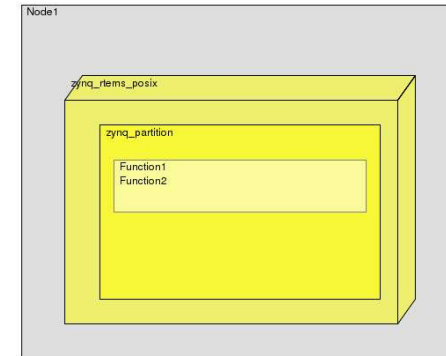
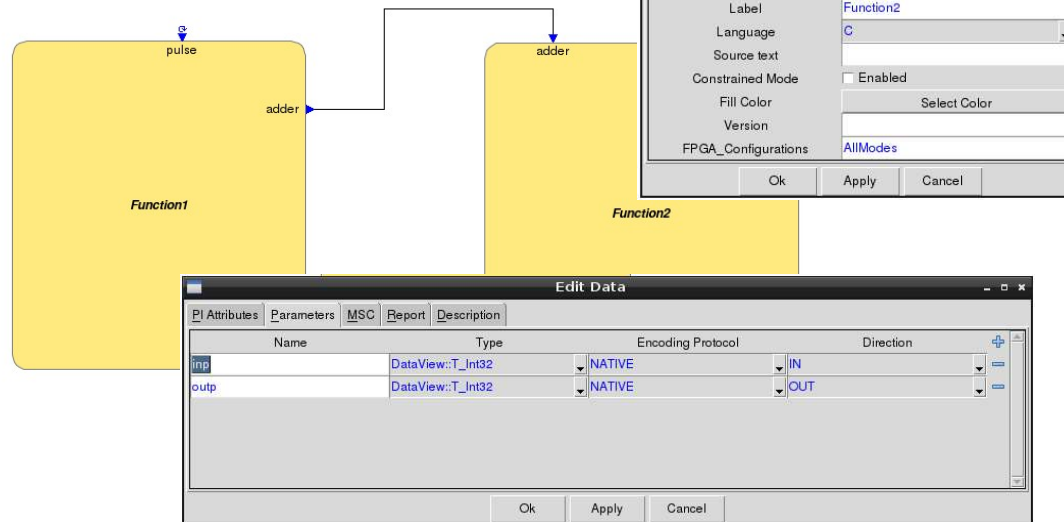
The use cases implemented have as prime objectives to:

- 1) demonstrate the toolchain new target support
- 2) support a space representative application

CORA-MBAD FOR ZYNQ 7000 USE CASES

Simple Use Case – Prime numbers

- Compute prime numbers from C code, on Zynq-7000:
 - Caller function in C, running on ARM.
 - Compute function in C, running on FPGA.



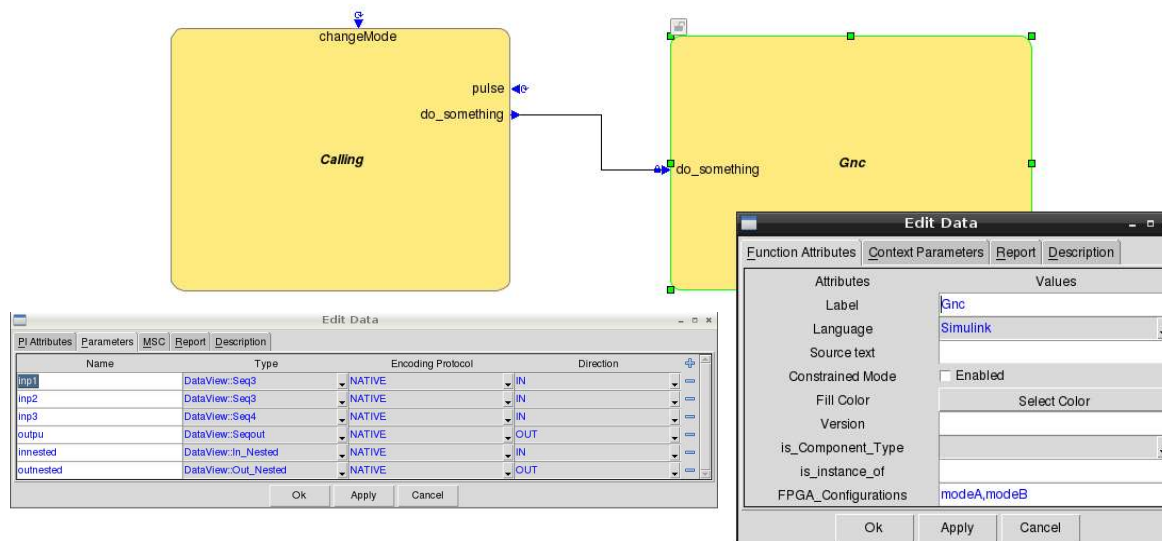
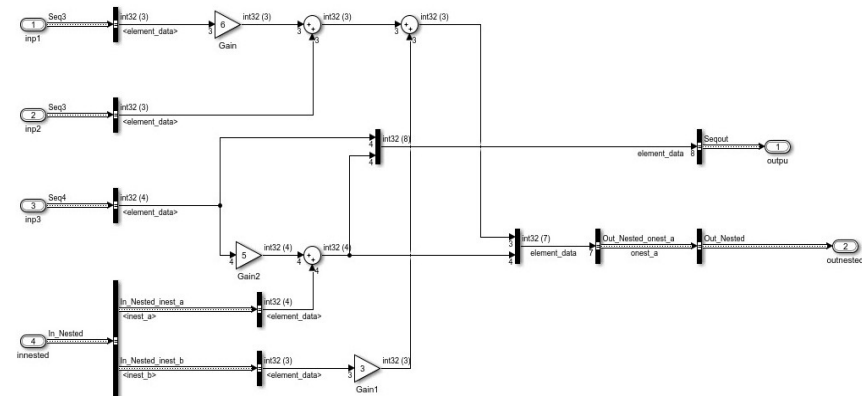
```
void function2_PI_adder
(const asnlSccT_Int32 *IN_inp,
 asnlSccT_Int32 *OUT_outp)
{
    // Write your code here
    if( *IN_inp % 2 == 0){
        *OUT_outp = 2;
        return;
    } else {
        for (int i=3; i <= *IN_inp / 2; i+=2){
            if(0 == (*IN_inp % i)){
                *OUT_outp = 1;
                return;
            }
        }
        *OUT_outp = *IN_inp;
    }
}
```

```
[function1_PI_pulse] Sent 8, Got 2
[function1_PI_pulse] Sent 9, Got 3
[function1_PI_pulse] Sent 10, Got 2
[function1_PI_pulse] Sent 11, Got 11
[function1_PI_pulse] Sent 12, Got 2
[function1_PI_pulse] Sent 13, Got 13
[function1_PI_pulse] Sent 14, Got 2
[function1_PI_pulse] Sent 15, Got 3
[function1_PI_pulse] Sent 16, Got 2
[function1_PI_pulse] Sent 17, Got 17
[function1_PI_pulse] Sent 18, Got 2
[function1_PI_pulse] Sent 19, Got 19
```

CORA-MBAD FOR ZYNQ 7000 USE CASES

Simple Use Case – GNC

- Compute simple GNC algorithm from Simulink code, on Zynq-7000:
 - Caller function in C, running on ARM.
 - Compute function in Simulink, running on FPGA.



```

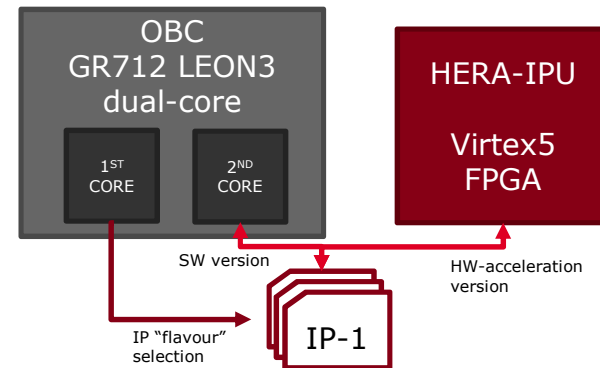
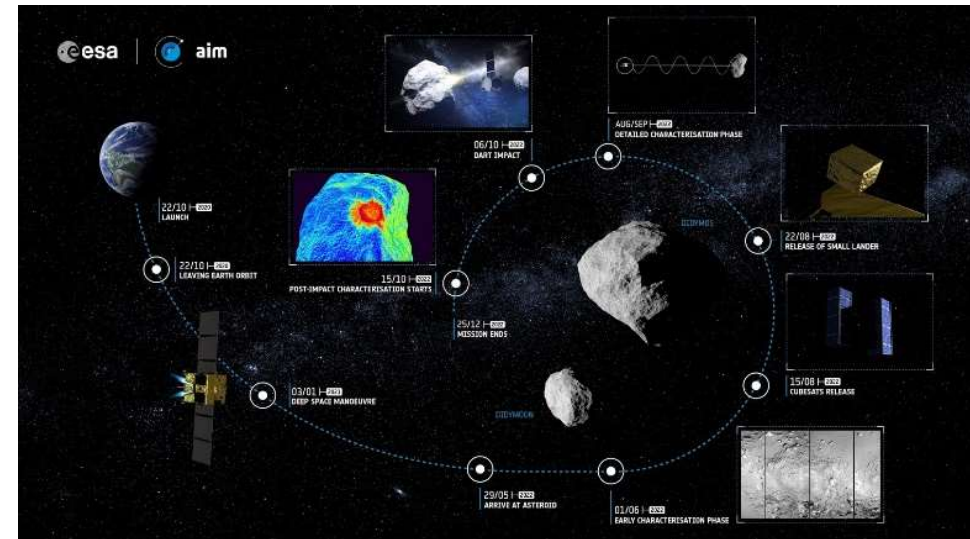
Data View | Interface View | Deployment View | Concurrency View | AADL
1 TASTE-Dataview DEFINITIONS ::=
2 BEGIN
3 IMPORTS T-Int32, T-UInt32, T-Int8, T-UInt8, T-Boolean FROM TASTE-BasicTypes;
4
5 TASTE-Boolean ::= BOOLEAN
6
7 -- ASN.1 Type definitions must start with an uppercase
8 -- Field names in records (SEQUENCE) must start with a lowercase
9 -- Underscores are not allowed: use dash (hyphen)
10
11 MyInteger ::= INTEGER (-411673351.. 763937697)
12 -- MyReal ::= REAL (0.0 .. 1.0)
13
14 Seq3 ::= SEQUENCE (SIZE (3)) OF MyInteger
15 Seq4 ::= SEQUENCE (SIZE (4)) OF MyInteger
16 Seqout ::= SEQUENCE (SIZE (8)) OF MyInteger
17
18 In-Nested ::= SEQUENCE {
19   inest-a SEQUENCE (SIZE (4)) OF T-Int32,
20   inest-b SEQUENCE (SIZE (3)) OF T-Int32
21 }
22
23 Out-Nested ::= SEQUENCE {
24   onest-a SEQUENCE (SIZE (7)) OF T-Int32
25 }
26
27 -- Simple types
28
    
```



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HERA mission

- Autonomous Vision-Based Navigation
- Proximity operations
- Computer-vision algorithms are computationally costive in terms of execution time and memory
 - Offload SW Processor
 - Acceleration by means of FPGA
 - Large data to be processed 1024*1024 pixels
 - Real-Time high-performances
- HW-accelerated functions
 - Computer-vision Lambertian sphere matching of asteroid body
 - Feature Detection and Tracking surface terrain of asteroid
 - Interchange SW functions with FPGA ones and among them

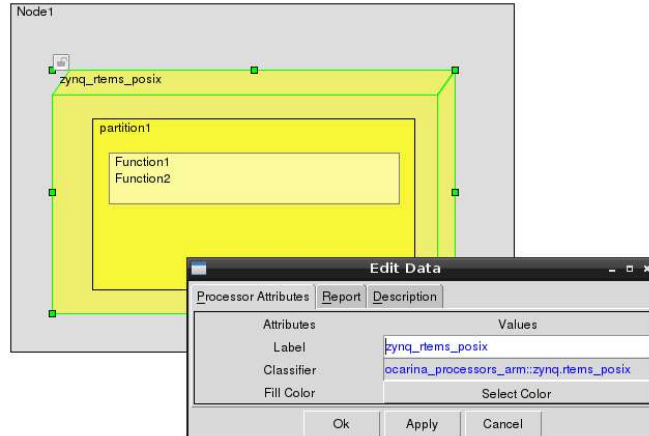
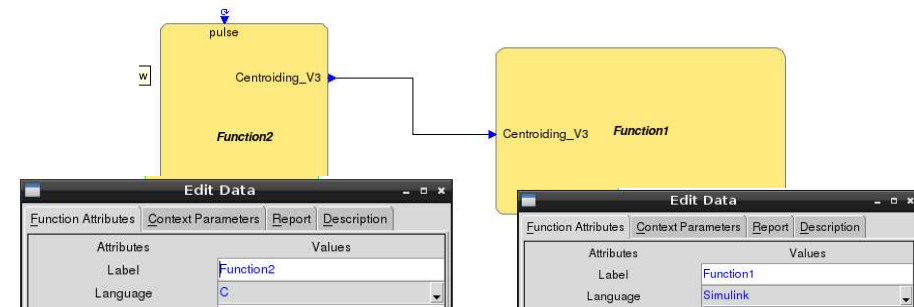


CORA-MBAD FOR ZYNQ 7000 USE CASES

HERA mission

TASTE model designed for Use Case algorithm integration:

- ASN.1 Data types tailored to use case IOs.
- Interface View with a calling interface to the Simulink generated algorithm.
- Deployment on Zynq-7000 target.



Attribute	DataView:MyReal	NATIVE	IN
pixel_rows_in	DataView:MyReal	NATIVE	IN
pixel_cols_in	DataView:MyReal	NATIVE	IN
binning_ratio	DataView:MyReal	NATIVE	IN
threshold_binary	DataView:MyReal	NATIVE	IN
k_scale	DataView:MyRealSeq5	NATIVE	IN
k_scale_step	DataView:MyReal	NATIVE	IN
auto_k_scale	DataView:MyReal	NATIVE	IN
radius_peak	DataView:MyReal	NATIVE	IN
margin_radius_rel	DataView:MyReal	NATIVE	IN
COB_diff_thr	DataView:MyReal	NATIVE	IN
CAM_FOV	DataView:MyReal	NATIVE	IN
asteroid_real_diameter	DataView:MyReal	NATIVE	IN
sphere_centre	DataView:MyRealSeq2	NATIVE	OUT
sphere_radius	DataView:MyReal	NATIVE	OUT
best_valid_Rs	DataView:MyRealSeq5	NATIVE	OUT

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HERA mission

The Matlab design reused is not tailored for a HW implementation (e.g. no parallel nor fixed-point design) which naturally represents some challenges to the autocoding facilities and HW resource usage.

Such tailoring was not yet performed due to project scope and time availability.

SW RUN



```
[[Function2] Startup...  
[function1] Centroiding_V3_initialize  
[Function2] PI_pulse  
[function1] Centroiding_V3_step  
[Function2] PI_pulse done!  
[Function2] Elapsed Time - 2.005620539 s  
Centroiding_V3 done with iteration 0  
    sphere_centre      {520.000000, 500.000000}  
    sphere_radius      201.791794  
    cent_valid_flg      TRUE  
    apparent_altitude  22115.820312
```

```
Expected sphere_radius 201.791794 (0x40693956605ee569), got 201.791794 (0x4069395660000000)  
Expected apparent_altitude 22115.820313 (0x40d598f4800218df), got 22115.820312 (0x40d598f480000000)
```



CORA-MBAD FOR ZYNQ 7000 USE CASES

HERA mission

Targeting **prototyping** activities, the present approach is instead leveraging to the maximum possible extent the **configurability and autocoding strengths of the toolchain**, avoiding any manual work, e.g. by exploring:

- the rich Embedded Coder and Bambu **options**
- types of possible SW-HW **interfaces** generated (e.g. external memory access, streaming type parameters) and resulting HW resource allocation.

some Bambu options relevant:

bambu --compiler=I386_CLANG4 --experimental-setup=BAMBU-TASTE --no-iob --clock-period=10 -O2 ...

some Embedded Coder options relevant:

*long long support
reference interfaces*

Some metrics of the Bambu generated HW kernel:

```
<item stringID="XILINX_SLICE" value="30202"/>
<item stringID="XILINX_SLICE_REGISTERS" value="53786"/>
<item stringID="XILINX_SLICE_LUTS" value="98319"/>
<item stringID="XILINX_BLOCK_RAMFIFO" value="83"/>
<item stringID="XILINX_IOPIN" value="0"/>
<item stringID="XILINX_DSPS" value="92"/>
<item stringID="XILINX_POWER" value="0.416"/>
<item stringID="XILINX_DESIGN_DELAY" value="24.028"/>
```

CORA-MBAD FOR ZYNQ 7000 USE CASES

HERA mission

Bambu options are enriched for the specific HERA mission use case and it's needs on **PandA-Bambu v0.9.7**:

- User allocation of external memory
- Floating point computation considerations
- Specific TASTE setup

Bambu options:

bambu

```
--compiler=I386_CLANG4
--experimental-setup=BAMBU-TASTE
--funroll-loops
--no-iob
--clock-period=5
--fno-inline -O2
--speculative-sdc-scheduling -DSTATIC=
--top-fname=bambu_Centroiding_V3
--generate-interface=INFER -v4
--panda-parameter=none-registered-ptrdefault=1
-lm --xml-memory-allocation=memory_allocation.xml
--evaluation --device-name=xc7z045-2ffg900-VVD
--no-clean --max-sim-cycles=1000000000
--max-ulp=1073741825
--bram-high-latency=4
--memory-ctrl-type=D21
bambu_Centroiding_V3_array.c
Centroiding_V3.c
ert_main.c rtGetInf.c rtGetNaN.c rt_nonfinite.c
```



CORA-MBAD FOR ZYNQ 7000 USE CASES

HERA mission

Hardware limitations

Some considerations should be taken into account when complex systems like HERA, composed by several intensive algorithms in terms of memory access and allocation, are implemented on FPGAs:

- Design should implement as less accesses to memory as possible in order to increment the performance of the application.
- Accesses to memory should have a low latency (ideally embedded memory blocks into FPGA).

However, in some cases it is impossible to allocate all the needed memory into RAM blocks and external memories are required.



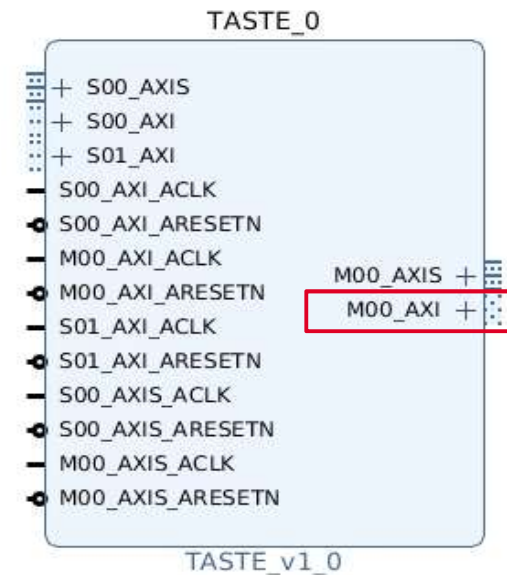
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HERA mission

Advance TASTE Wrapper

In order to solve the memory limitations in HERA design (or any other design intensive in memory) a new AXI interface has been added to connect with any external memory controller with an AXI user interface.

This new interface allows the generated Bambu design to read and write from/to an external memory. In the specific case of HERA design, the SODIMM DDR3 allocated in ZC706 board and accessible by the PL.



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HERA mission

Advance TASTE Wrapper Status

- Advance TASTE Wrapper IP generated and interfaces validated in simulation
- HERA block design implemented

To be performed

- Validation of HERA design in simulation
- Validation of HERA design in ZC706



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Conclusions

- TASTE's Kazoo facilitates toolchain evolution
- Role of Design Environment Engineer becoming increasingly important
- Increased collaboration between SW and HW engineers
- Functions can be fully automatically deployed in SW and HW from a high-level domain model (e.g. Simulink)
- Generated SW-HW interface and HW interface with Bambu kernel for computation is otherwise very challenging - CoRA-MBAD allows for rapid implementation iterations
- The configuration of the autocoding tools goes a long way in making integration easier and resulting in more efficient designs
- TASTE's toolchain allows for easy scalability of HW interfaces, fitting to applications needs

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Future work

- Address runtime reconfiguration
- Improve autocoding and synthesis results
- Trade-off analysis with manual implementations
- Address more use cases, targetting diversified purposes (e.g. speed, memory, interfaces, etc.)
- Stress test TASTE translators for robustness
- Support advanced interfaces for modern EGSE integration
- and other



Thank you

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