Verification of SEU-mitigation techniques in 3rd/4th generation Flash FPGA

I. INTRODUCTION

Flash-based FPGAs are relatively new additions to the portfolio of space-grade FPGAs, and Microsemi is the main provider of these parts. Microsemi has developed two Flash-based FPGA families specially for space: RT Polarfire and RTG4 (the specimen under test see Figure 1). These new families offer a high number of high-performance programmable logic resources, large and fast onboard memories, and high performance I/O - SERDES, LVDS, DDR, etc. All the elements are very appealing in high-bandwidth data processing payload applications, but also high-performance on-board computing so a detailed understanding of the behaviour of the FPGA fabric under radiation is necessary.

AS&D, in collaboration with NASA/GSFC (see [1]) have done a study on the SEE characterization of the logic fabric in the RTG4, i.e. SEUs in flip-flops, global routing behaviour (SETs in clock and reset lines), as well as configuration cell updates and reprogrammability susceptibility to SEE. In addition to that The Radiation Effects group in ESTEC/ESA also run an activity on the characterization of the memory blocks in RTG4.

Figure 1: RTGA4 FPGA

In order to expand the knowledge of this brand-new technology, ARQUIMEA and UC3M in consortium presented a proposal based on ARQUIMEA's background on microelectronics design and radiation testing of ICs and UC3M's experience on fault tolerant design, emulation and verification of mitigation techniques. The consortium were selected to accomplish the following tasks:

- Carlos III University of Madrid (UC3M): Development of (formal) verification methods for verifying the proper implementation of SEU/SET mitigation techniques for Flash based FPGAs.

- ARQUIMEA Ingeniería (ARQ): To perform an extensive radiation test campaign, targeting RTG4 FPGA from Microsemi (RTG4 in particular) for: Characterization of PLL performance (SEE sensitivity) under radiation, sensitivity of the FPGA fabric, and of the test vehicles used, to SEFI and Characterization of the I/O blocks. 3.3V/2.5V/1.8V/1.5V/1.2V LVCMOS, LVTTL, PCI, LVDS, LVDS33, SSTL2I, SSTL2II, HSTLI, HSTLII, and SERDES.

II. MAIN RESULTS

A. *Formal Verifications Tools*

The developed Formal Verification Tool (FVTool) consists in a console application, with a twofold objective.

It can be used to formally verify the correctness of a variety of SEE mitigation techniques to harden digital designs. It is intended as well to formally verify the functional equivalence between a hardened design and the original version (before hardening). FVTool reports on the success or failure of equivalence analysis as well as on the correct implementation of the mitigation techniques. In case of failure, it shows a counterexample in order to help designers to identify the origin of the difference.

FVTool is applied in three steps, as shown in Figure 2, by using several commands:

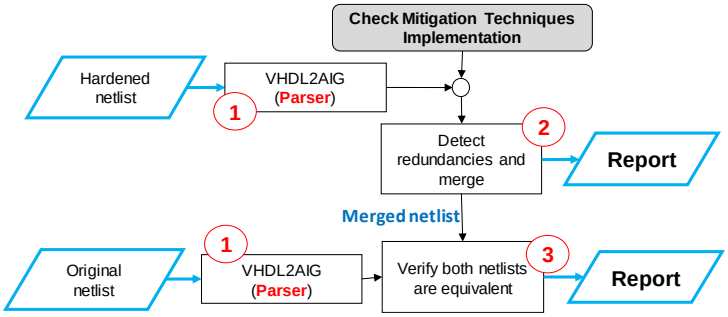

Figure 2: Execution Flow

1. Parsing the input files to generate AIG formats (.hag file). This first step generates the intermediate files that will be analysed and processed in the following steps.
2. Verifying the correctness of the mitigation techniques. This step generates another intermediate file, also in AIG format, where the existing redundancies have been removed (a merged netlist). In case errors in the mitigation techniques are detected, they are reported as well as an input vector as proof. The supported techniques are:
    a. Local, distributed, block and I/O TMR
    b. Safe FSM encoding (automatic error recovery of the FSM to the state specified in the "Reset" condition)

c. Safe Case FSM (automatic error recovery of the FSM to the state specified in the "others/default" clause)
d. Hamming-3 FSM encoding (detection of invalid FSM transitions)
e. Duplicate and compare
f. SET filtering by triplication of the clock and reset trees, with insertion of delay elements on each of the three clock/reset nets

3. Verifying the functional equivalence between the pre-processed hardened version of the circuit and the original one.

B. Radiation Testing

The parts radiated in this activity are RTG4 FPGAs from Microsemi, manufactured on a low power µMC 65nm process, with the main features detailed:

Table 1: Radiation specifications

Device	RT4G150-CB1657PROTO
Manufacturer	Microsemi
Operating Temperature Range	Tj (Junction) From -55ºC to 125 ºC θJB (LGA1657) =0,22ºC/W
Package	CBGA1657 - DWG KYOCERA KD-YB4319
Package Size:	1.693" x 1.693" (43 mm x 43 mm)

Eight DUTs were provided by ESA to the project team. Six out of the eight parts were radiation tested whereas two of them were left as spare. Two designs were available for programming the parts: Design A and Design B. Each design contained a different set of test vehicles (Windowed Shift Register, Ring Oscillators, Counters, SpaceWire, CCSDS, CAN Bus, ARM M0, SERDES, PLL, CCC, Output Pad, Input Pad to Output Pad & Power-On Reset). All parts were back grinded so that the radiation testing could be performed on them. Some tests vehicles were conceived to check their performance against SETs whereas others were inspected for their SEU sensitivity. Latch up monitoring was done on all the parts during SET and SEU runs at room temperature. A detailed test setup (Figure 3) and Design A (Figure 4) & Design B architecture (Figure 5), can be found hereafter:

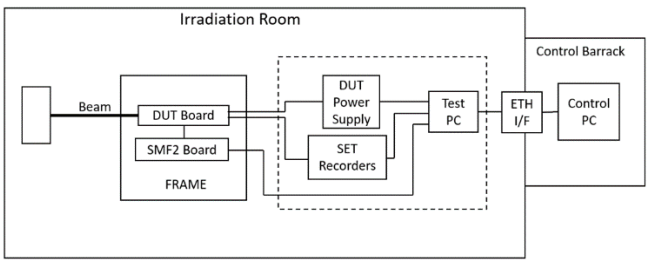

Figure 3: Radiation tests setup block diagram

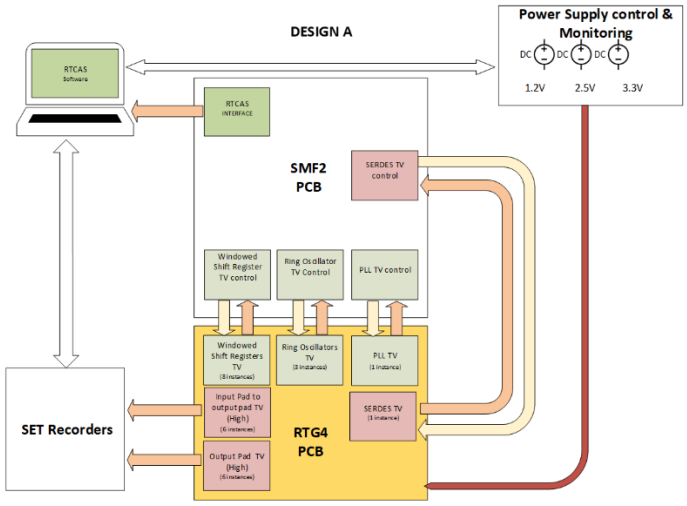

Figure 4: Design A detailed test setup view

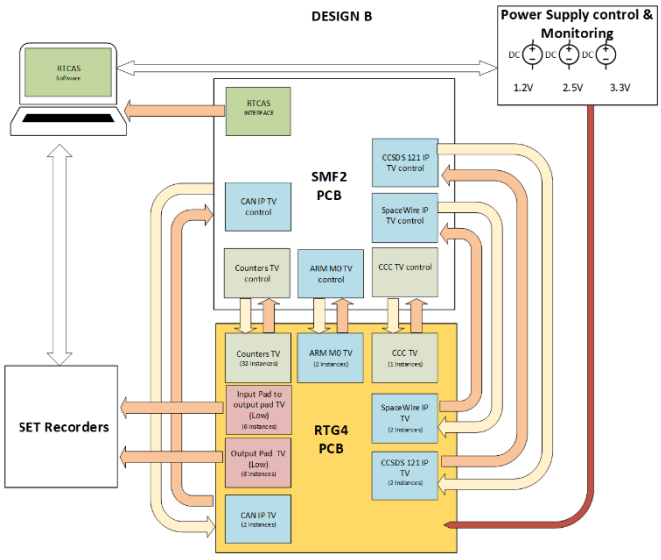

Figure 5: Design B detailed test setup view

1) Heavy Ions Results

The test to characterize the performance against heavy ions were defined by different TV, as mentioned above, these TV (Windowed Shift Register, Ring Oscillators, Counters, SpaceWire, CCSDS, CAN Bus, ARM M0, SERDES, PLL & CCC) show results in accordance with previous researches, [2] and [3].

Some tests were designed for the pads with the following results:

The input to output pad configuration test results show that the occurrence of SETs when the pads are set to HIGH or to LOW level is different depending on the technology. The PADs set to high level are more sensitive to transients that when they are when set to low.

As for the output configuration, test results cannot be generalized in this respect since some pads like LVCMOS33/25 show a higher count whereas the rest seem to be performing similarly with independence of the value set to the pad.

In general, it can be said that high speed pad technologies are more sensible to this effect in terms of number of transients collected and sensibility to lower energies. SSTL2 and LVDS got transients with low energies (13.4MeV), 3.3V technologies as LVCMOS33 and LVTTL33 instead were robust up to high energy values (48.5MeV) getting very little transients per run. LVCMOS25 response was slightly worse, getting low level transients at 24.6MeV.

Let Threshold was very similar for the input to output configuration as for the output standalone one, whereas the number of events is slightly lower in the case of the output configuration which means that the transient contribution from input pads is very small.

I addition to that, the Power-On Reset window trigger for the recording of POR events was configured from 2.3v to 2.75V. Two SET events were recorded in this test vehicle, one on RUN 16 and another one on RUN 17. Error counters in Shift registers and PLL test vehicles for RUN16 present a big error jump that might be caused by a POR SET. In RUN number 17, Shift Registers and PLL Test Vehicles counters got saturation, because of that, data results from RUN 17 for all test vehicles were discarded. No events were recorded up to 48.5MeV

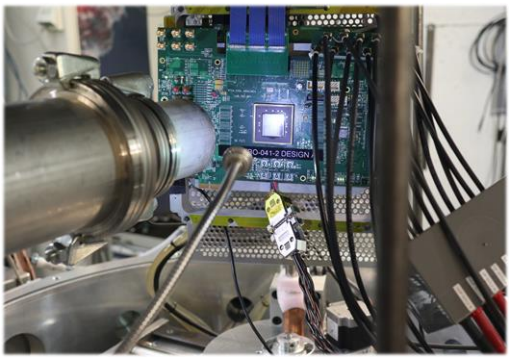

Figure 6: Ion beam and DUT

2) Protons Results

The test results recorded for the different TV (Windowed Shift Register, Ring Oscillators, Counters, SpaceWire, CCSDS, CAN Bus, ARM M0, SERDES, PLL & CCC) reveals good performance, as no mayor events were recorded.

Some tests were designed to verify the pads: SETs have been observed in some tested pads both when checking the input to output connection and the output. Almost all the recorded SETs are wide.

The input to output pad configuration test results show that very low events were recorded at HIGH and some as LOW. As for the output configuration, very few events were recorded on the high-speed pads when set to HIGH. Output pads set to LOW have shown no transients.

III. CONCLUSIONS

According to the experimental results, the VHDL parser and AIG generation software module have passed all the tests. Regarding the verification module, it can be stated that the considered hardening techniques have been successfully included and that FVTool is able to formally verify if the implemented error mitigation techniques are correct or not. It generates a verified netlist without the redundant logic due to mitigation techniques, what allows the comparison with respect to a not hardened version.

With respect to the equivalence checker, the result is successful for TMR, DTMR, BTMR and DWC for circuits without FSMs. For circuits with FSMs, the result of the equivalence checking depends on the synthesis over the unreachable states, what is out of the control of the FVTool.

In conclusion, the formal verification tool developed has reached most of its goals although there are some limitations to be looked at for improvement in future works.

The radiation testing campaigns provided a quite interesting set of results. On one hand, the radiation performance of the RTG4 FPGAs reported in previous reports like [2] and [3] has been confirmed. For the main FPGA internal building blocks two main regions of operation are clearly identified: al lower energies the number of errors is smaller and the SET filtering feature improves significantly the performances whereas at higher energies the number of errors is bigger and the SET filtering has no effect (being therefore the SEU the dominating factor). The SET filtering feature also improves the performances at high frequencies where the SET events have a higher impact. The results of other FPGA fabric building blocks like the PLL and the SERDES are also in line with the ones reported in the literature. The PLL presents some SET and SEFI sensitivity but with a cross section good enough for most of the applications whereas the SERDES presents a big casuistic of error types with a degraded BER under radiation, including a complex scenario of SEFIs.

On the other hand, the testing performed in this activity shows some results that had not been previously reported, i.e. the SET sensitivity of the pads. SETs have been observed in all the tested pads both when checking the input to output connection as well as when checking the outputs fixed at a constant value. Many of those SETs have a width below 10 ns however very wide pulse transients have been recorded as well. Following this, SETs recorded in the pads could have been produced by the POR internal circuitry, due to lack of architectural information on how it is implemented, it is not possible to confirm those SETs were generated by POR reset.

As for the investigations found on the IPs, it was confirmed that the radiation performance is quite

dependent on the design and the observability /recoverability of the potential errors.

In beam programming has also been tested concluding that with low fluxes, the reprogramming of the parts can be done at various energy levels.

IV. REFERENCES

[1] “NEPP Independent Single Event Upset Testing of the Microsemi RTG4: Preliminary Data”, Berg et al, June 2016.

[2] Single Event Effects Hardening on 65 nm Flash Based Field Programmable Gate Array. 2016_RADECS_DW _Paper_JJW

[3] "Radiation testing of EEE parts in support of ESA R&D activities", Call of Order 2 "Heavy ion SEE Testing of Microsemi RTG4 flash based FPGA", ESTEC TEC-QEC Statement of Work for Call of Order 2 to ESTEC/ESA Contract No. 4000113