ARQUIMEA
Passion for technology

26/05/2020

Final Presentation

Verification of SEU mitigation techniques in 3rd/4th generation FPGAs

ARQUIMEA

Agenda

- 9:30 – 9:35 Introduction
- 9:35 – 9:50 Verification techniques main results, lessons learnt and conclusions
- 9:50 – 10:05 Radiation testing main results, lessons learnt and conclusions
- 10:05 – 10:10 Final conclusions
- 10:10 - 10:15 Questions and answers

ARQUIMEA

Introduction Scope

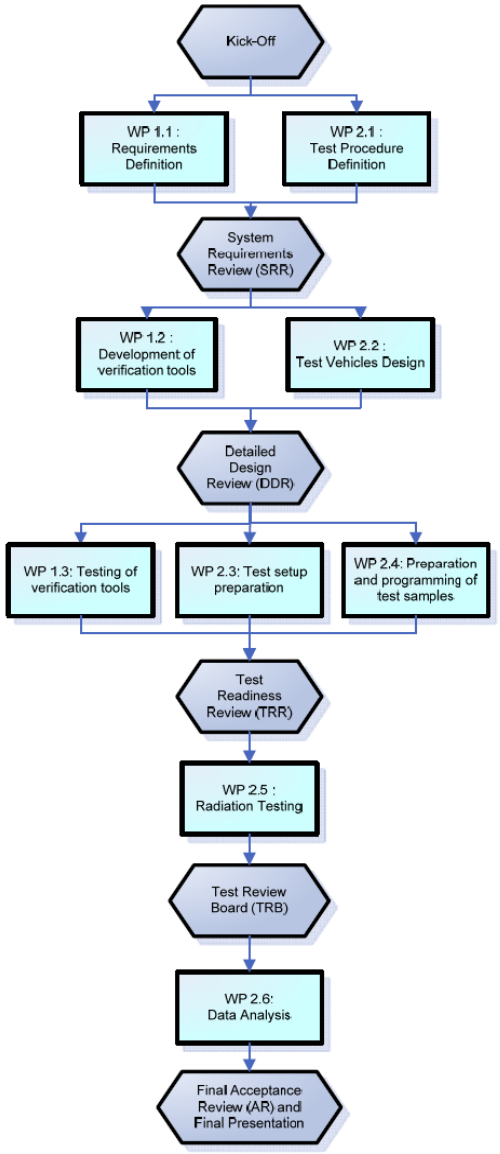
- The project had two main objectives or tasks:
  - Task 1 as detailed in the SoW: "*This task will address the development of formal verification methods for verifying the proper implementation of SEU/SET mitigation techniques for Flash based FPGAs, applied at RTL or netlist level (e.g. TMR, "safe" Finite State Machines, etc.)".*
  - Task 2 as detailed in the SoW: *The objective of this task shall be an extensive radiation test campaign, targeting 4th generation Flash FPGAs (Microsemi RTG4), with the following aims:*
    a) *Characterization of PLL performance (SEE sensitivity) under radiation.*
    b) *Sensitivity of the FPGA fabric, and of the test vehicles used, to SEFI.*
    c) *Characterization of the I/O blocks. In particular, the following types of I/O buffers will be characterized: 3.3V/2.5V/1.8V/1.5V/1.2V LVCMOS, LVTTL, PCI, LVDS, LVDS33, SSTL2I, SSTL2II, HSTLI, HSTLII, and SERDES.*
- The activity was conceived to last 18 months, but the project evolution was such that it finally took 21 months.

Introduction The team

- The project had two partners:
  - uc3m was in charge of task 1
  - ARQUIMEA was responsible for the overall project management and task 2

Introduction

Project workflow



Formal Verification methods Specifications

- Software tool to formally verify proper implementation of SEU/SET mitigation techniques.
  - It shall be implemented as a set of stand-alone scripts or executable programs
  - Dependencies from specific commercial tools should be avoided
  - Mitigation techniques:
    - TMR, DWC
    - Safe FSM encoding, Hamming, ...
  - 3rd and 4th generation Flash FPGAs

Formal Verification methods Proposed solution

- **FVTool: Verihard**
  - Twofold goal:
    - Verify mitigation techniques → They do **correct/detect errors**
    - Verify equivalence with the original version of the circuit → Mitigation techniques **do not modify** the original **functionality**
  - Command-line tool developed by using C++, Windows (64, 32) and Linux support
  - Input files must be structural VHDL netlists.
  - The tool applied formal verification techniques based on **Combinational Equivalence Checking** over structural graphs (AND-Inverter Graph, AIG)

Formal verification techniques

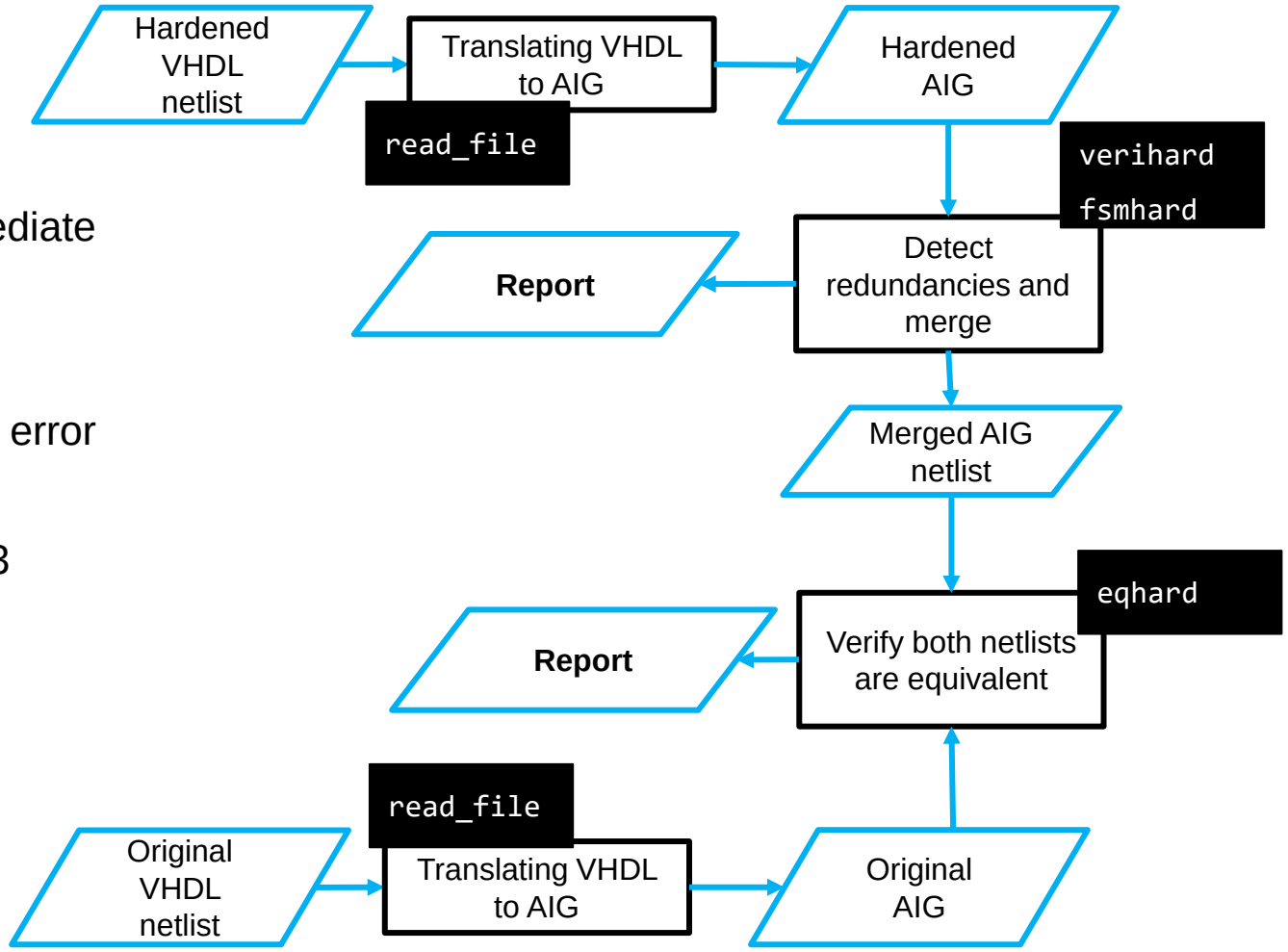
- ❑ Structural hashing
- ❑ Implication-based reasoning
- ❑ Satisfiability solving

Auxiliary techniques

- ❑ Random simulation
- ❑ Name matching

Formal Verification methods Proposed solution

- The tool consists of three software modules
  1. VHDL parser
     - Structural VHDL netlist → AIG intermediate format
  2. Verification of hardened design
     - Detect errors in the implementation of error mitigation techniques
     - Merge redundancies to perform step 3
  3. Equivalence checking



Formal Verification methods Tool use

VeriHard esa uc3m

TCL scripts

0 VHDL netlist generation: synthesize the original and the hardened version

1º Parse the netlist to generate the AIG file: original and hardened versions → AIG file

```
G:\FVTool\examples>read_file spacewire.vhm
Warning: Signal SLOWCLK is not used
Warning: Signal TXCLK is not used
Warning: Signal SLOWCLK is not used
Warning: Signal SLOWCLK is not used
Warning: Signal RDCLK is not used
Warning: Signal CFG_SLOW_CE is not used
```

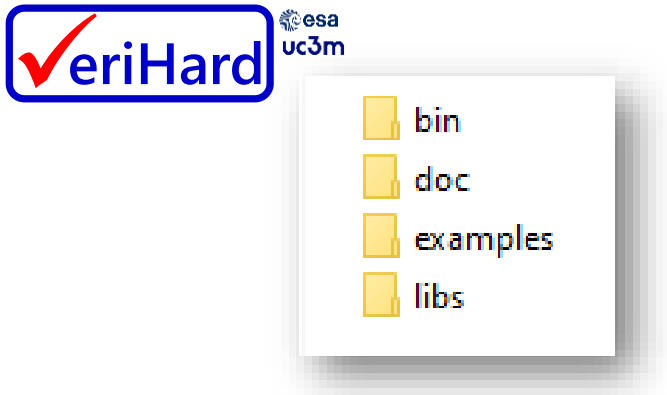
2º Verify the hardening techniques → Merged AIG file

```
G:\FVTool\examples>verihard --tmr init_fsm
VERIFY: Fault \INTFCE_STATE[5]_Z212\ stuck-at 0 is redundant!
VERIFY: Fault \INTFCE_STATE[5]_Z212\ stuck-at 1 is redundant!
VERIFY: Fault \INTFCE_STATE[4]_Z213\ stuck-at 0 is redundant!
VERIFY: Fault \INTFCE_STATE[4]_Z213\ stuck-at 1 is redundant!
```

3º Verify functional equivalence of original and hardened versions

- Correct
- Incorrect → test vector

Formal Verification methods Tool use



bin

- eqhard.exe
- flatten_all.exe
- fsmhard.exe
- install_path.bat
- library_print_test_comp.exe
- merge_logic.exe
- read_file.exe
- test_verihard.exe
- test_violin_aig.exe
- verihard.exe
- violin.exe
- violin_aig.exe
- write_file.exe

libs

Technology libraries

- gtech
- igloo2
- proasic3e
- proasic3l
- rtg4
- smartfusion2
- synplify

Workspace

fvtool_env.violin

```
-----------------------------------------
-- VIOLIN Environment variables
-----------------------------------------
set library_path ".";
set work_path ".\work";
set match rule from "( TMR[123])" to "";
```

Launch tool from the folder where environment file is stored

Formal Verification methods Tool validation

- Windows / Linux
- Tests with simple benchmarks (useful for debugging the tool)
  - Correct versions of the hardening techniques
  - Wrong implementations
- Tests with the test vehicles (ARM, CAN, SpaceWire, CCSDS121)
  - Single mitigation techniques
  - Combined mitigation techniques

Formal Verification methods Requirements, capabilities and limitations

- The circuit must be fully synchronous
- One asynchronous initialization signal is supported but it is handled as a synchronous signal
- Works on structural VHDL netlists (synthesized)
- Formal verification of the mitigation techniques

Supported mitigation techniques	Limitations
Local TMR	---
Distributed TMR	---
Block TMR, DWC	---
Safe FSM encoding	Only one flip-flop for generating invalid state condition is supported
Safe case FSM	
Hamming-3 FSM encoding	Additional user information is required to improve code identification
SET filtering	---
Combining techniques: Verification in sequence	It requires improvements on the redundancy merging tool

Formal Verification methods Requirements, capabilities and limitations

- Equivalence checking: formal verification of functional equivalence
  - Limitations due to combinational equivalence checking techniques
    - #inputs, #outputs, #ffs must be equal
    - It requires same hierarchy levels
    - Logic changes across flip-flops (retiming) is not supported
    - Does not verify FSMs when logic for unreachable states is different

Formal Verification methods Lessons learnt

- **Mainly related with the Equivalence Checking**
- **Options of the synthesizer tool for generating the VHDL structural netlist of original and hardened versions are critical**
  - In a hierarchical circuit, keep the hierarchy. The interface of two circuits to compare by equivalence checking must be the same.
  - Invalid states for FSMs
  - Replication of flip-flops
  - Reset flip-flops for safe encoding condition → only one reset flip-flops is supported by the current version
- **Sequential verification techniques may be required for complex cases**

Formal Verification methods Conclusions and Future Work

- The formal verification tool meets all the requirements
- According to the experimental tests:
  - Parser and AIG generation 
  - Verifying mitigation techniques → there are some limitations when several techniques are applied
  - Verifying functional equivalence → limitations due to limitation of combinational equivalence checking techniques
- Future improvements:
  - Add Sequential Equivalence Checking (SEC) for FSMs or particular cases where flip-flops do not directly match
  - Enhancing capabilities by allowing additional user constraints (identifying Hamming-3 codes, invalid states in FSMs)
  - Improve performance and usability

Radiation testing Requirements and test vehicle design

- At SRR the requirements specification and a preliminary test plan were closed. This milestone gave the green light for the test vehicle design activity.

- The test vehicles were split into two different designs:

  - Design A: which addressed mainly the FPGA fabric and contained shift registers, ring oscillators, a SERDES, a PLL and several input and output pads to be investigated.

  - Design B: which addressed both some additional FPGA fabric and particular IP cores. It contained counters, a POR, a CCC, a Spacewire, CAN, ARM M0 and CCSDS IP cores and also several input and output pads to be radiation tested.

ARQUIMEA

Radiation testing Specimens under test

- Radiation of RTG4 FPGAs from Microsemi (RT4G150-CB1657PROTO) manufactured on a low power µMC 65nm process.

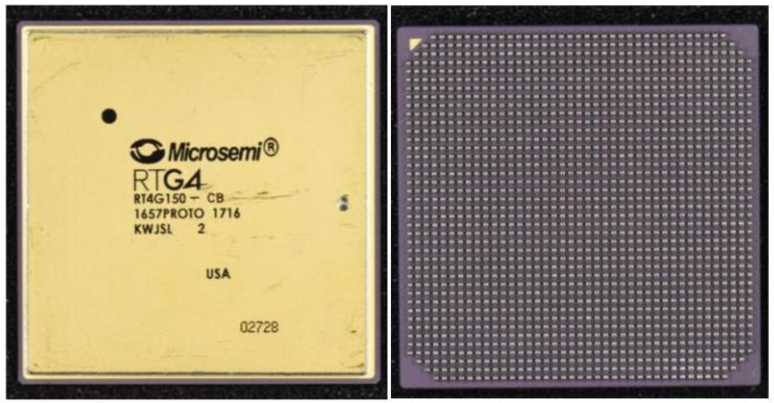
- Eight DUTs were provided by ESA to the project team. Two designs were available for programming the parts: Design A and Design B.

Test Vehicles (TV)	TV Number	Design Type	Heavy Ion		Proton	
			SET	SEU	SET	SEU
Windowed Shift Register	7	A		X		X
Ring Oscillators	3	A	X		X	
Counters	32	B		X		X
Output Pad	6	A & B	X		X	
Input Pad to output pad	6	A & B	X		X	
SpaceWire CODEC	2	B		X		X
CCSDS 121	2	B		X		X
CAN Bus Controller	2	B		X		X
ARM M0	2	B		X		X
SerDes	1	A		X		
PLL	1	B	X		X	
Power-On Reset	1	A & B		X		X
CCC	1	A	X		X	

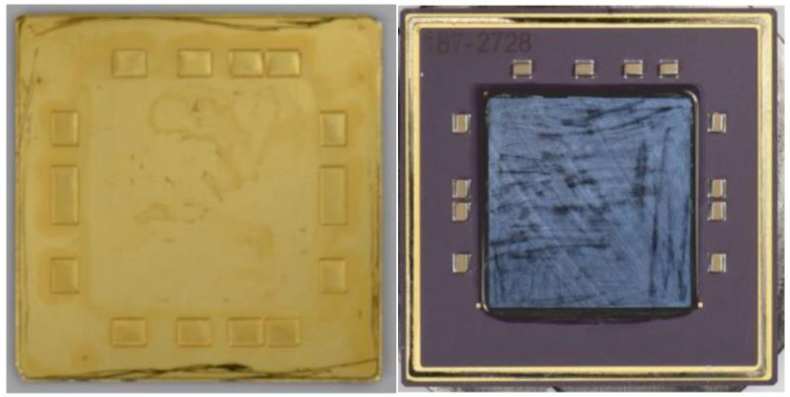
DUTs	Serial Number	Date Code	Back-grinding depth	Design Type	Radiation Test	Re-balled	Comments
DUT1	2730	1716	55 – 64µm	A	HI & Proton		
DUT2	7143	1638	54 – 69µm	A	HI & Proton		
DUT3	7147	1638	63 – 78µm	A	HI & Proton		
DUT4	7148	1638	69 – 76µm	B	HI & Proton		SPW1 configured as RX and SPW2 as RX Hardened
DUT5	7158	1638	58 – 65µm	B	HI & Proton		SPW1 configured as TX and SPW2 as TX Hardened
DUT6	2728	1716	63 – 73µm	B	HI & Proton	X	SPW1 configured as RX and SPW2 as RX Hardened
DUT7	2690	1716	50 – 70µm	-	Spare	X	
DUT8	2692	1716	60 – 69µm	-	Spare	X	

Radiation testing Parts back-grinding

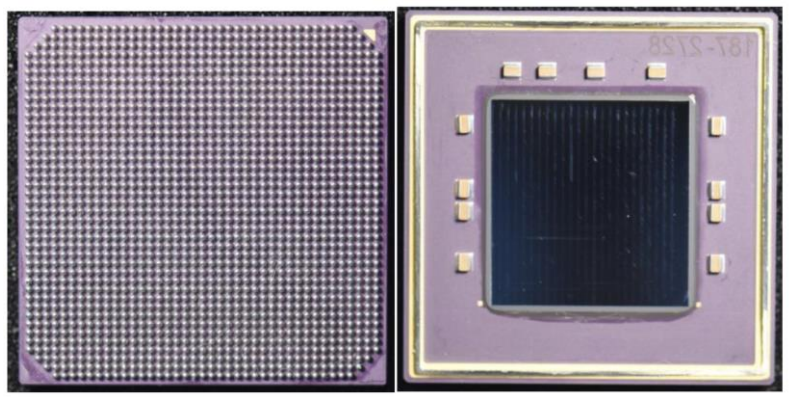
- The parts had to be de-lidded and back grinded following the recommendations provided by Microsemi.



Before opening



After de-lidding

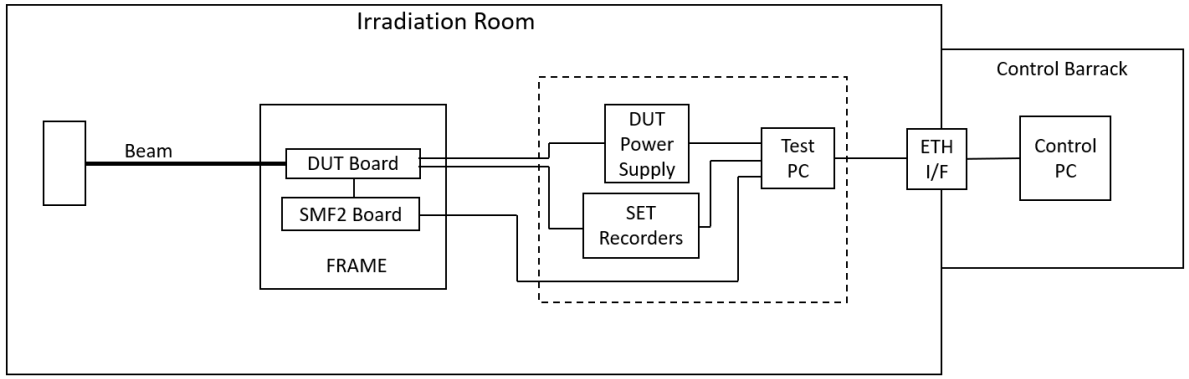


After back grinding

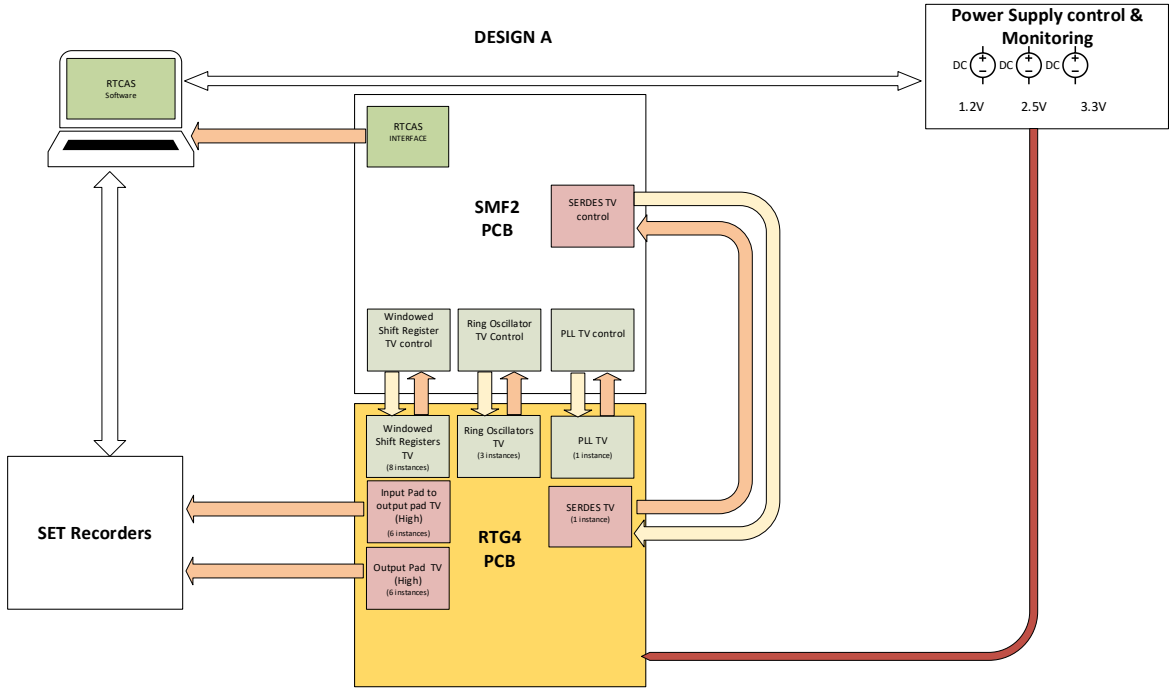
Radiation testing Test setup description

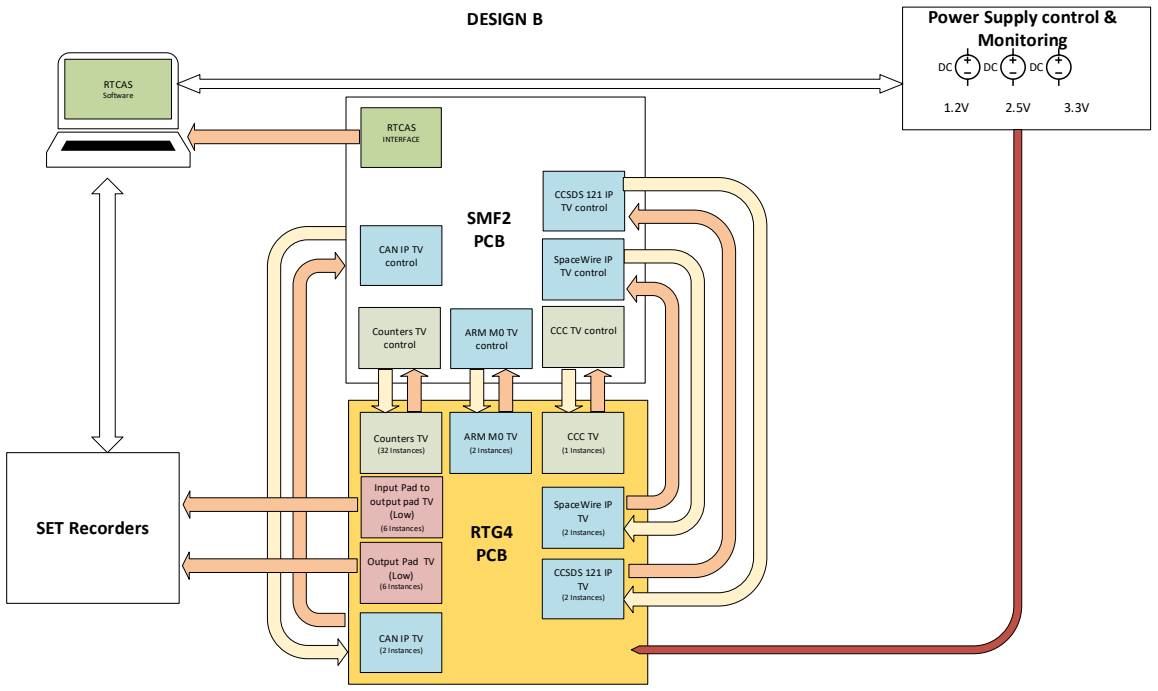
- The setup consists on the elements detailed hereafter

  - **DUT Board:** RTG4 Evaluation kit modified and populated with the DUT and the necessary components to perform the tests.
  - **SMF2 Board:** SMF2 Evaluation kit configured to be connected to the DUT Board and to the Test PC
  - **FRAME**: It will hold DUT and SFM2 boards in the irradiation chamber.
  - **DUT Power Supply:** Power supply controlled remotely by RTCAS software which powers the DUT board and detects SELs.
  - **SET Recorders:** Devices to log SETs of the proper TVs from the DUT
  - **Test PC:** This PC will run the RTCAS software to control the behavior of the SMF2 and DUT boards, to run the tests and to log data from the test. It also log Single Event Transients from the SET recorders.
  - **ETH I/F:** Ethernet interface for remote control of the Test PC between the Control Barrack and the irradiation room.
  - **Control PC:** This PC will be used to control the Test PC remotely from the Control Barrack of the facility.



Radiation testing Test setup (Design A and B)





Radiation testing Test setup issues

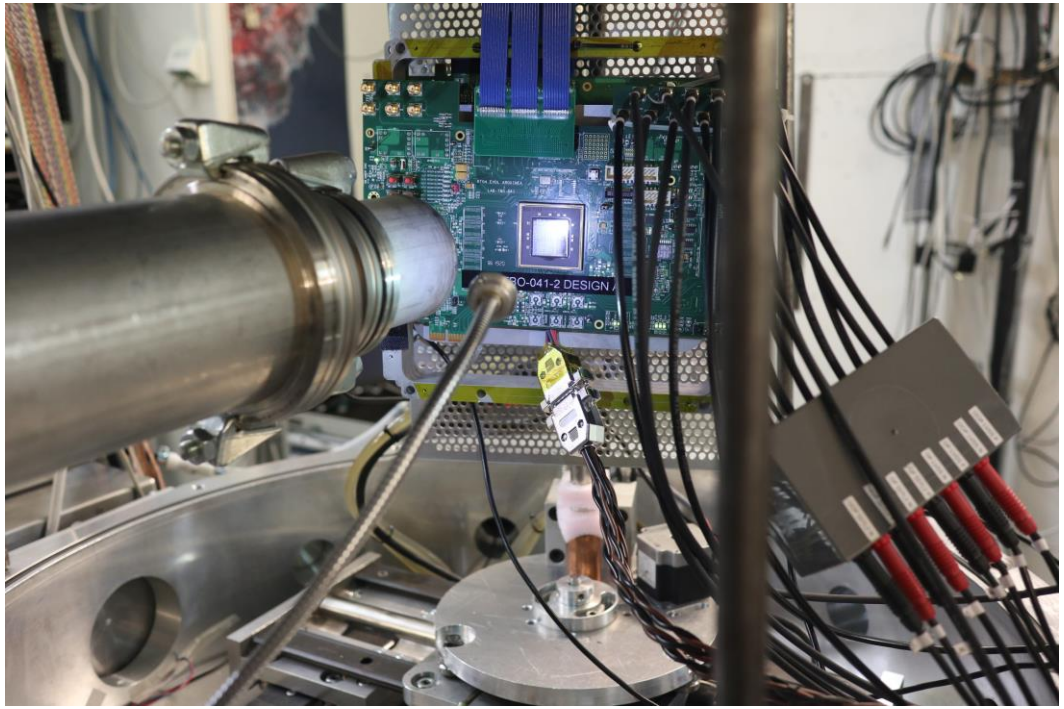
- Some of the FPGAs had to be unsoldered due to a misconfiguration on the pick and place equipment.
- The unsoldering process melted the FPGA balls, so the affected parts had to be re-balled. Once the re-balling process was completed, the affected FPGAs were soldered back on the PCBs.
- All tests vehicles and all FPGAs were fully tested, before the equipment was shipped to the radiation facility.

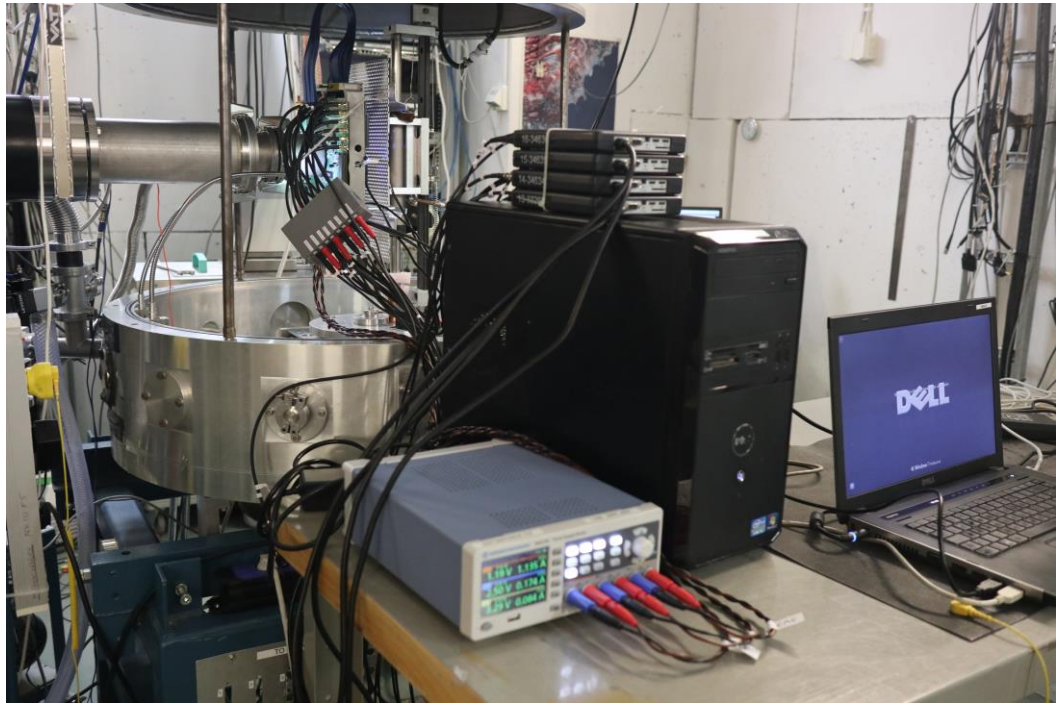
Radiation testing Radiation campaigns

- The Heavy ions test campaign took place at RADEF, Finland, in two shifts on November the 4th and 5th.
- During the Heavy Ion test campaign a few areas for improvement of the test setup observability were annotated, so that they could be considered for the proton test campaign.
- The Protons test campaign took place at PSI, Switzerland, in three shifts on November the 12th, 13th and 14th .

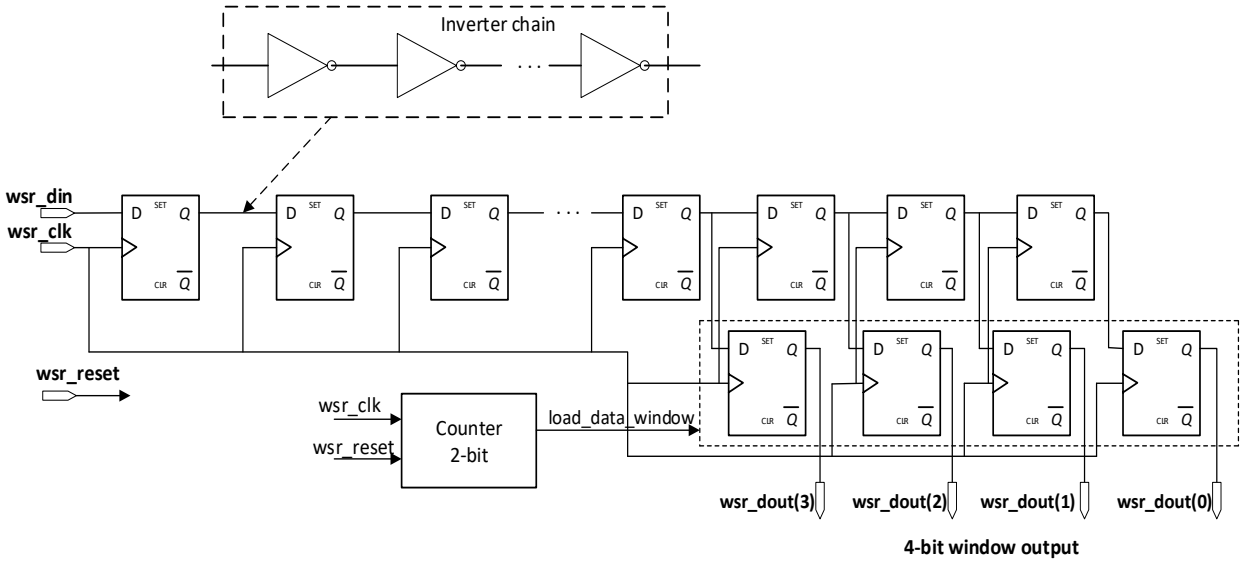
ARQUIMEA

Radiation testing Heavy ions tests at RADEF



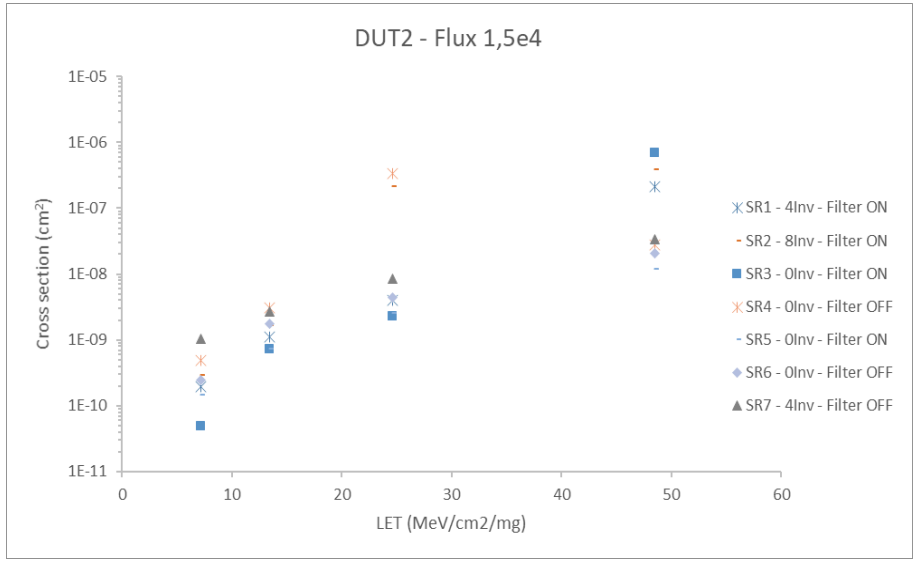


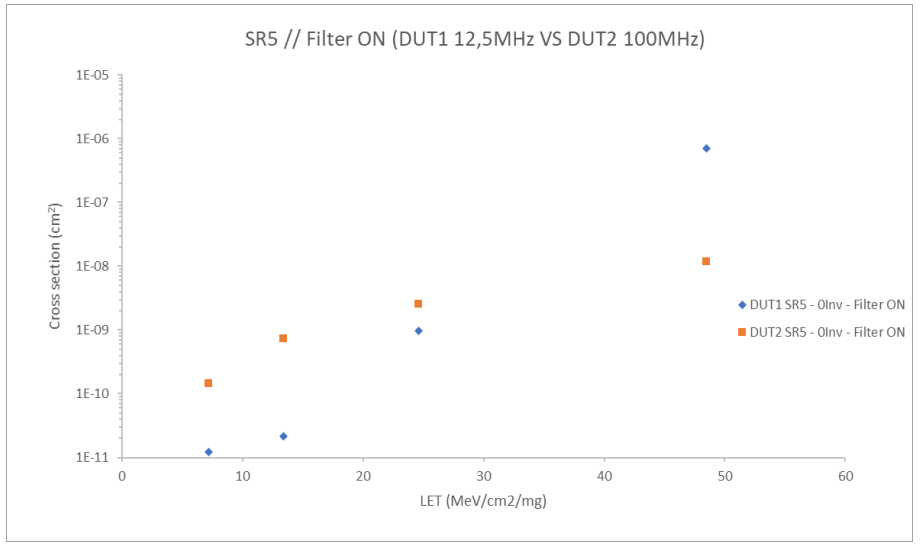
Radiation testing Heavy ions results - WSRs



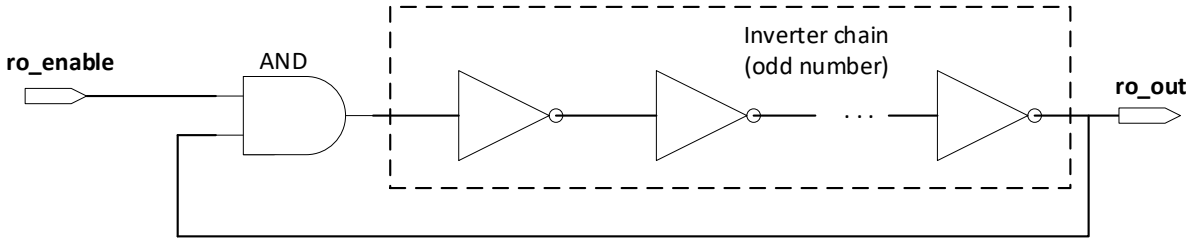
Radiation testing Heavy ions results - WSRs

- The results on the shift registers test vehicles, show that there are two clear regions with a different response
  - At lower energies, the number of errors is smaller, and the SET filtering has an impact on error reduction.
  - At higher energies, in the range of 45-50 MeVcm2/mg, the number of errors is significantly bigger, and the effect of SET filtering is negligible, being the SEU the dominating factor
- The errors increase with the inverters used in the SR configuration.
- At higher frequencies the effects of SETs are more relevant than at lower frequencies



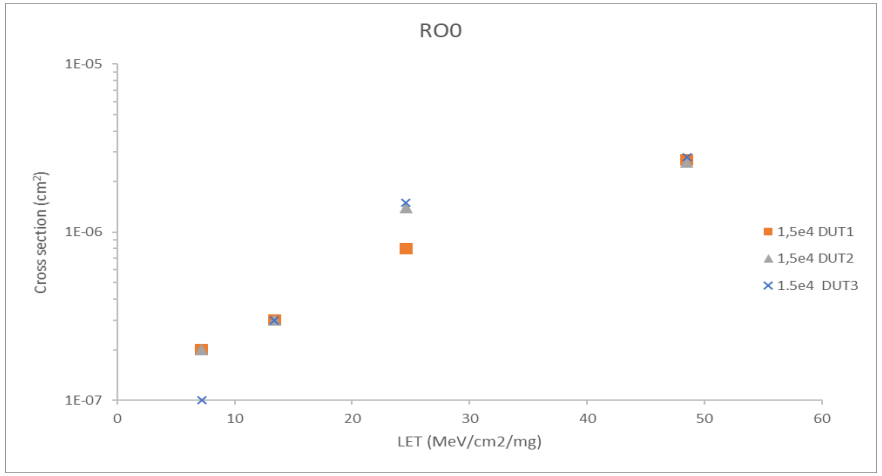


Radiation testing Heavy ions results - ROs

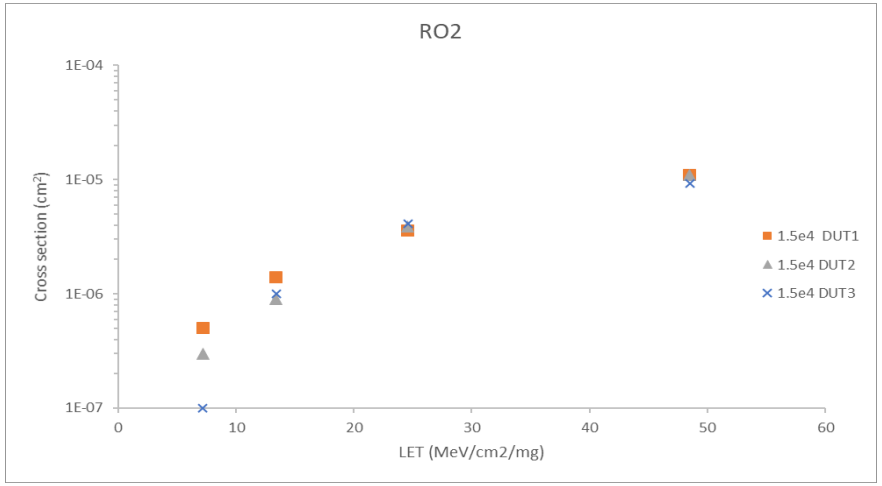


Radiation testing Heavy ions results - ROs

- The SET response of the ring oscillator test vehicles shows that errors are first observed at a LETth on the range of 5-8 MeVcm2/mg.
- The method for SET detection is a variation on the RO frequency higher than a fixed threshold (typically 10%).
- The higher the number of inverter cells, the higher the number of errors observed → the inverter cells are letting the SETs pass through, not filtering them out.

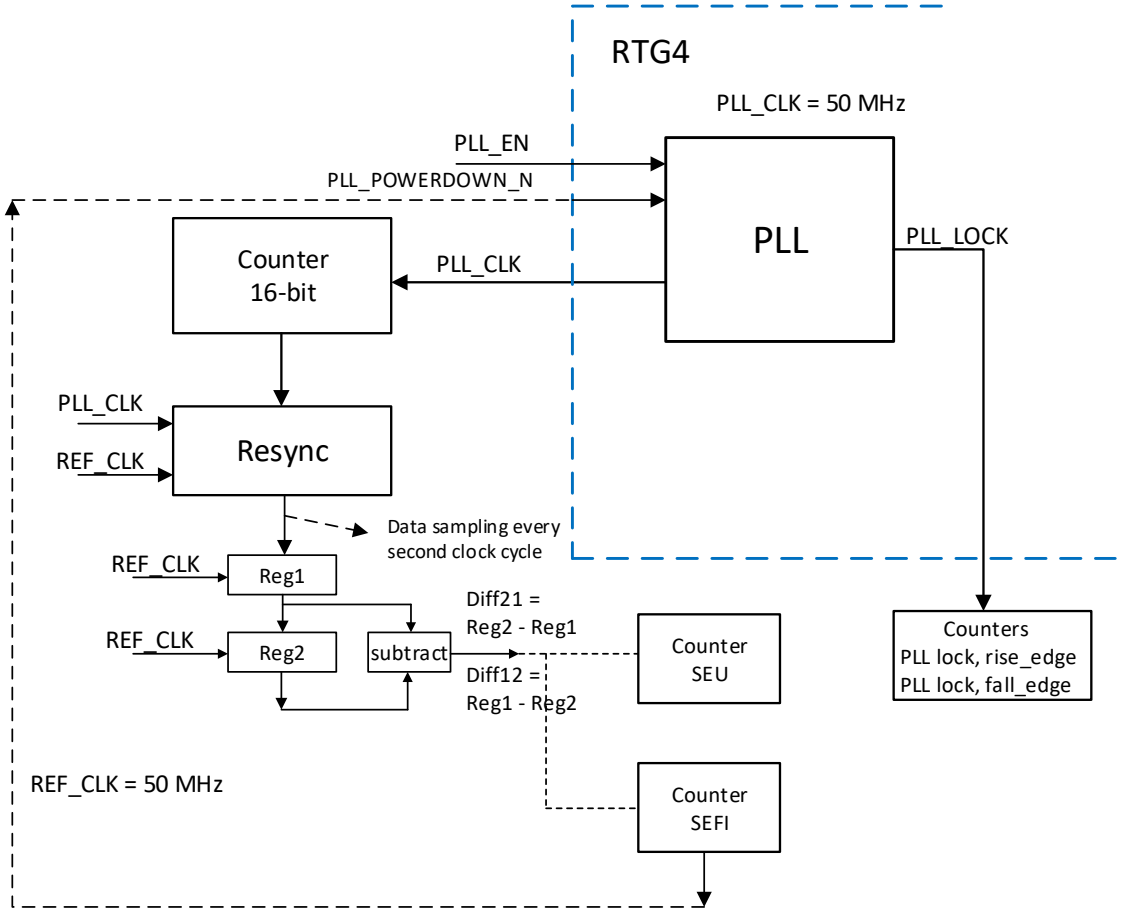


RO 0 with 201 inverters



RO 0 with 807 inverters

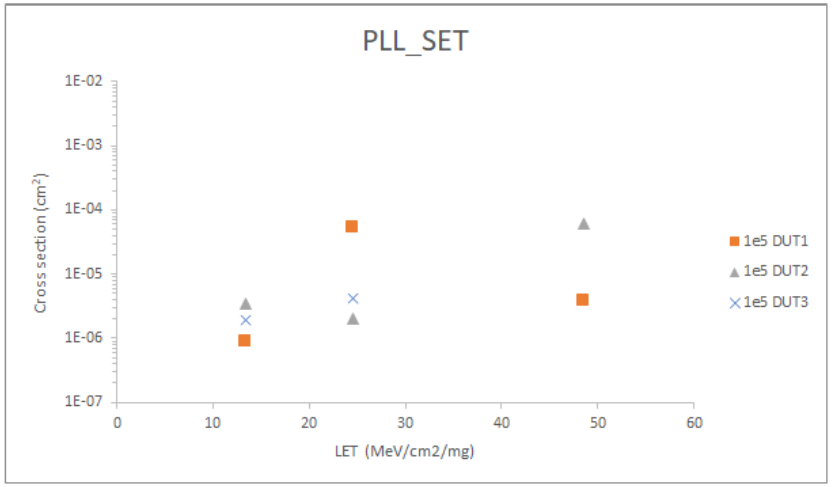
Radiation testing Heavy ions results - PLL

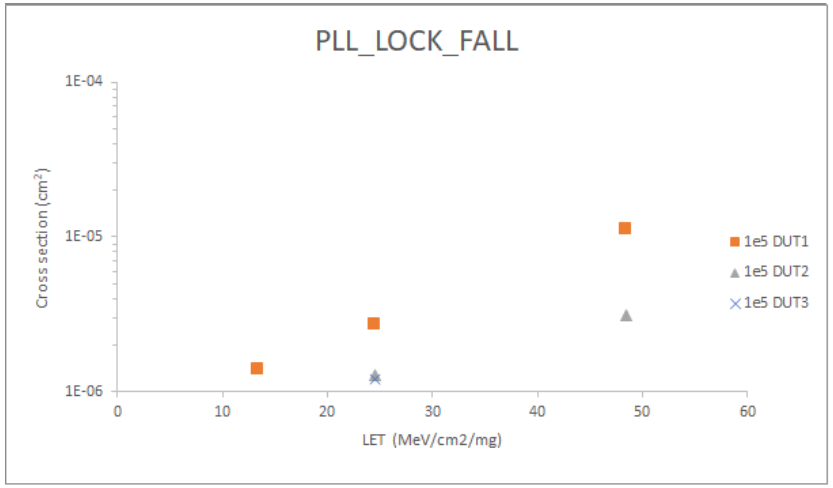


ARQUIMEA

Radiation testing Heavy ions results - PLL

- The test results on the PLL TV show that the errors recorded could be divided in two:
  - SETs that cause that the frequency of the TV is altered in the order of 10% for a single clock cycle
  - PLL lock failure errors that affect more than one clock cycle that could be identified as self-recovered SEFIs.

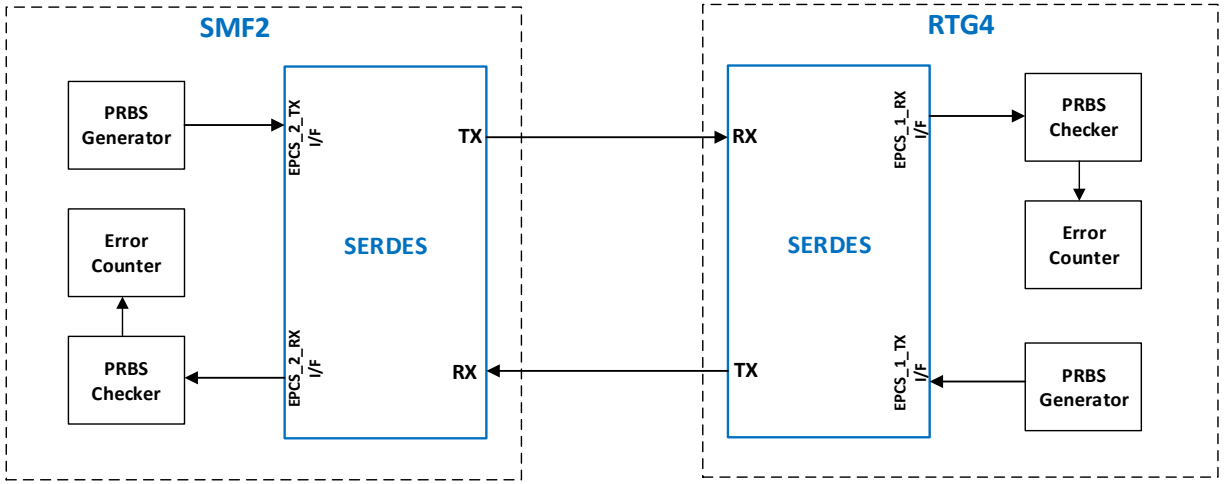


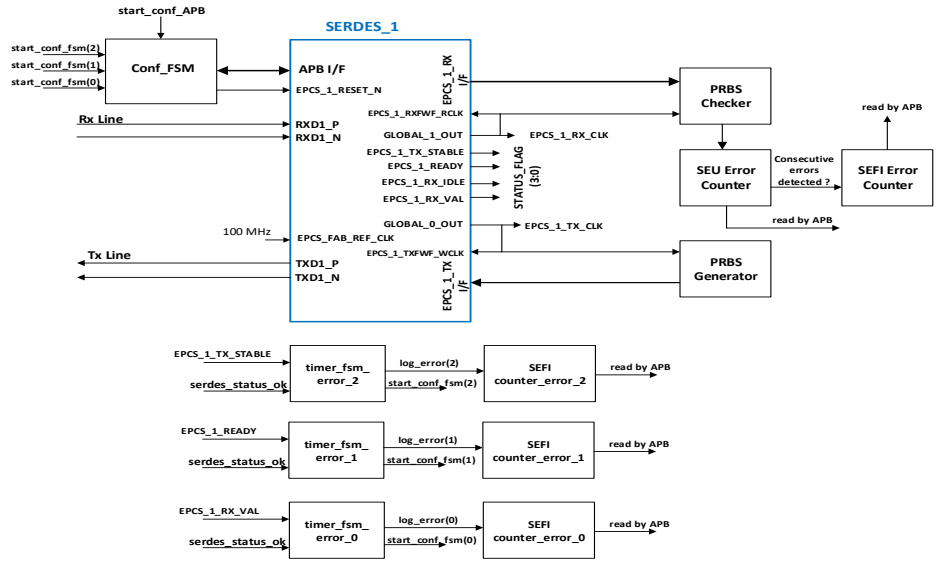


Radiation testing Heavy ions results - SERDES

- The Serdes RTG4 IP is configured with the following parameters:
  - Protocol: EPCS mode, lane 1
  - Reference clock frequency: fabric clock of 100 MHz
  - EPCS bus width: 20 bits
  - Data throughput: 2.0 Gbps

- Control logic around the Serdes IP is hardened using TMR technique as well as Hamming-3 coding for FSMs.

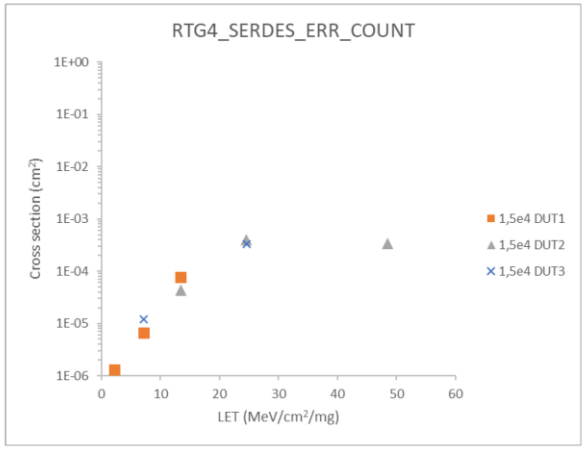




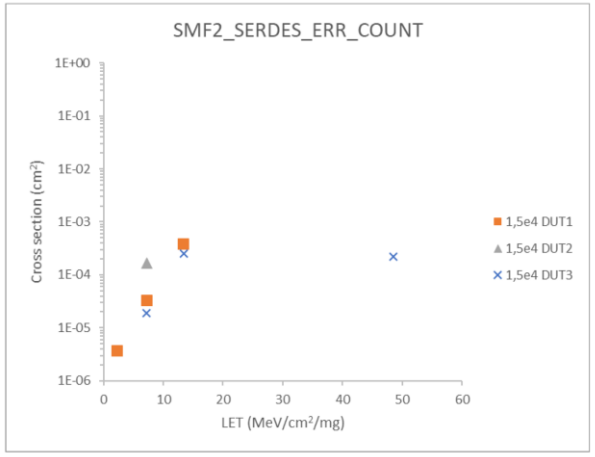
Radiation testing Heavy ions results - SERDES

- The results on the SERDES TV show a great number of errors. The casuistic of the errors recorded is also diverse.

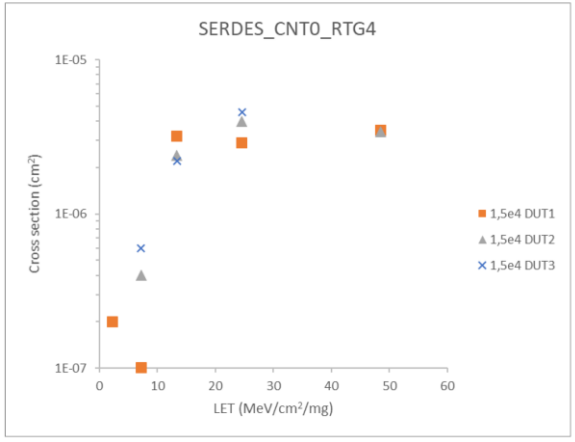
- In some runs the counters used for error recording were saturated or ramped up quite quickly which could be a symptom of a SEFI occurrence.



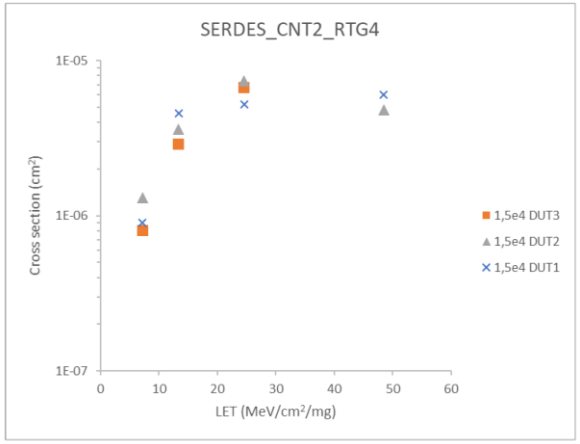
RX error counter (SEFIS removed)



RX error counter (SEFIS removed)



PLL not locked SEFI



CDR not locked SEFI

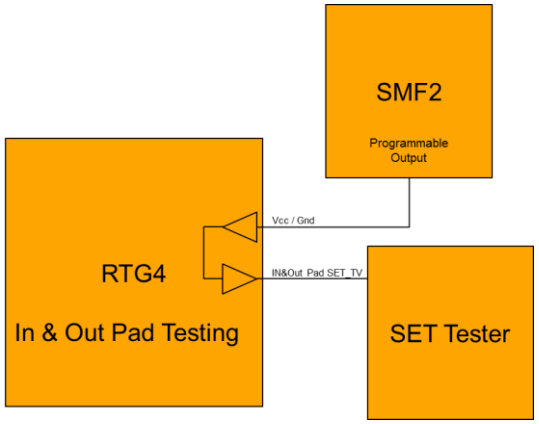
Radiation testing Heavy ions results – I/O pads

- SETs have been observed in all the tested pads both when checking the input to output connection as well as when checking just the output.
- A great amount of the recorded SETs have a width below 10 ns (which is the resolution of the transient recorder) however very wide pulse transients have been recorded as well.
- Unfortunately, the test equipment used to record the transients in most cases was limited to a maximum SET width of 160 ns.

Radiation testing Heavy ions results – I/O pads

- The input to output pad configuration test results also show that the occurrence of SETs when the pads are set to HIGH or to LOW level is different depending on the technology.

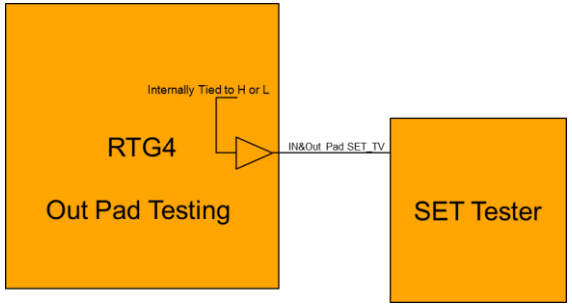
- The PADs set to high level are more sensitive to transients that when they are when set to low.



	Mean number of SETs captured per DUT (PAD at High)	Mean number of SETs captured per DUT (PAD at Low)
I2OP_LVCMOS33	6,5	4
I2OP_LVCMOS25	8	5
I2OP_LVTTL33	4	1
I2OP_LVDS	58	34
I2OP_SSTL2_D	14	11
I2OP LVCMOS25 HS	28,5	2

Radiation testing Heavy ions results – I/O pads

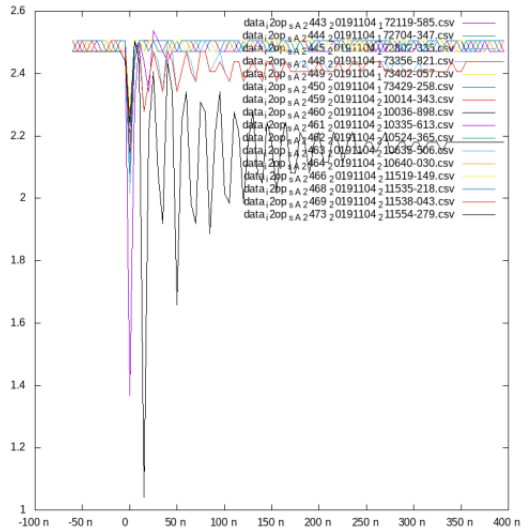
- For the output configuration, test results cannot be generalized in this respect since some pads like LVCMOS33/25 show a higher count whereas the rest seem to be performing similarly with independence of the value set to the pad.



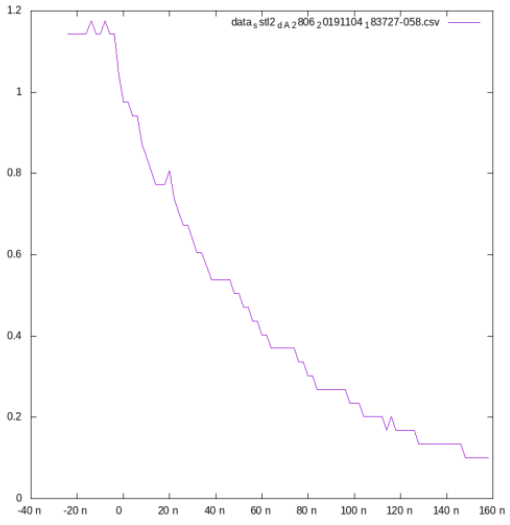
	Mean number of SETs captured per DUT (PAD at High)	Mean number of SETs captured per DUT (PAD at Low)
OP_LVCMOS33	1,5	4
OP_LVCMOS25	1	7
OP_LVTTL33	2,5	1
OP_POR25	2	1
OP_LVDS	49,5	46
OP_SSTL2_D	13,5	11

Radiation testing Heavy ions results – I/O pads

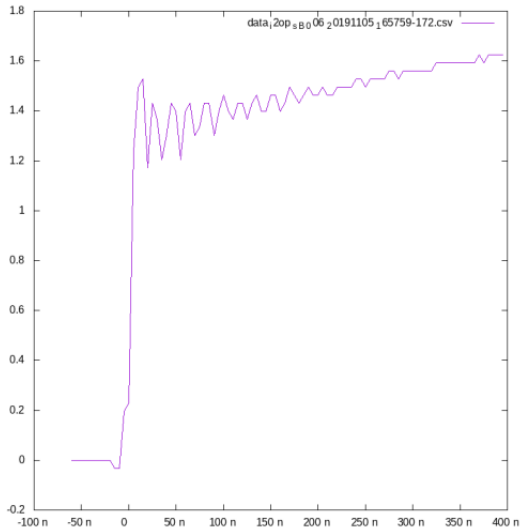
- In general, high speed pad technologies are more sensible to this effect in terms of number of transients collected and sensibility to lower energies. SSTL2 and LVDS got transients with low energies (13.4MeV), 3.3V technologies as LVCMOS33 and LVTTL33 instead were robust up to high energy values (48.5MeV) getting very little transients per run. LVCMOS25 response was slightly worse, getting low level transients at 24.6MeV.
- Let Threshold was very similar for the input to output configuration as for the output standalone one, whereas the number of events is just slightly lower in the case of the output configuration which means that the transient contribution from input pads is very small.



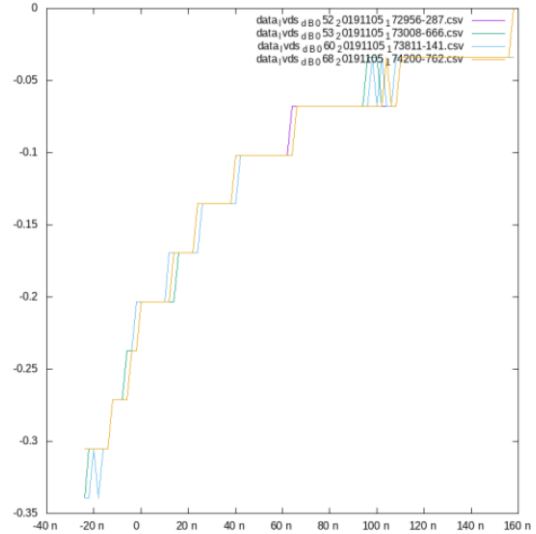
Transients recorded in I to O pad A_I2OP_LVCMOS25 set to HIGH level at 48.5 MeV/cm2/mg)



Transients recorded in output pad A_OP_SSTL2 set to HIGH level at 13.4 MeV/cm2/mg



Transients recorded in I to O pad B_I2OP_LVTTL33 set to LOW level at 48.5 MeV/cm2/mg



Transients recorded in output pad B_OP_LVDS set to LOW level at 24.6 MeV/cm2/mg

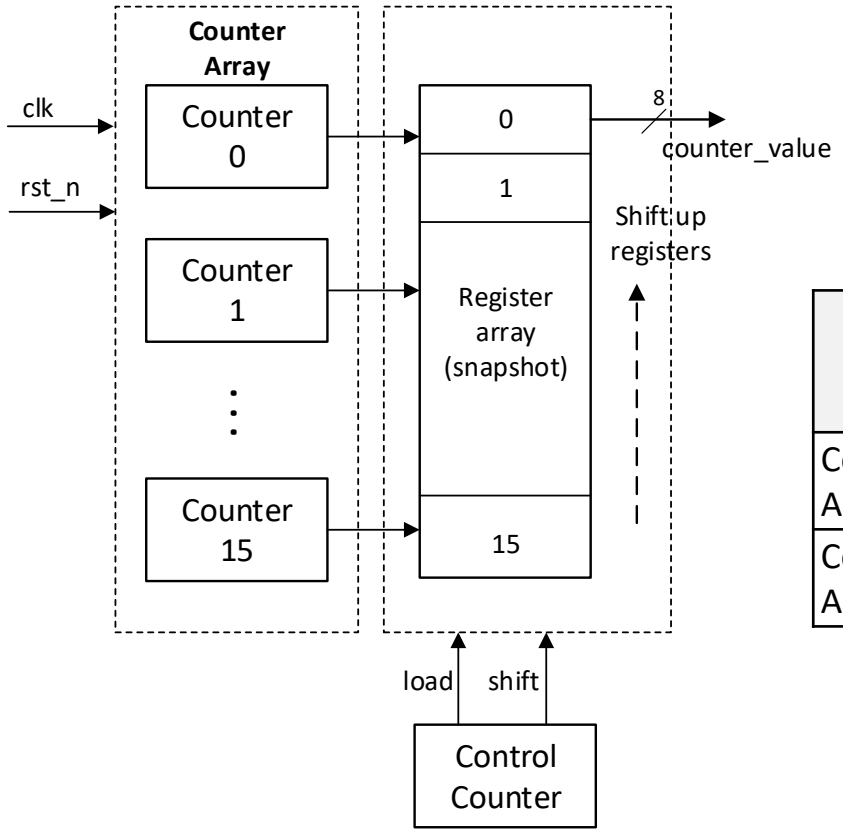
Radiation testing Heavy ions results – POR

- The POR TV is the SYSRESET macro from RTG4 macro cell library which is directly instantiated on the top-level of DUTA design. The “power_on_reset” signal is the output pin of SYSRESET macro connected to a CMOS2.5V pad and tested on transients.

- Two SET events were recorded in this test vehicle, one on RUN 16 and another one on RUN 17.

- No events were recorded up to 48.5MeV

Radiation testing Heavy ions results - Counters

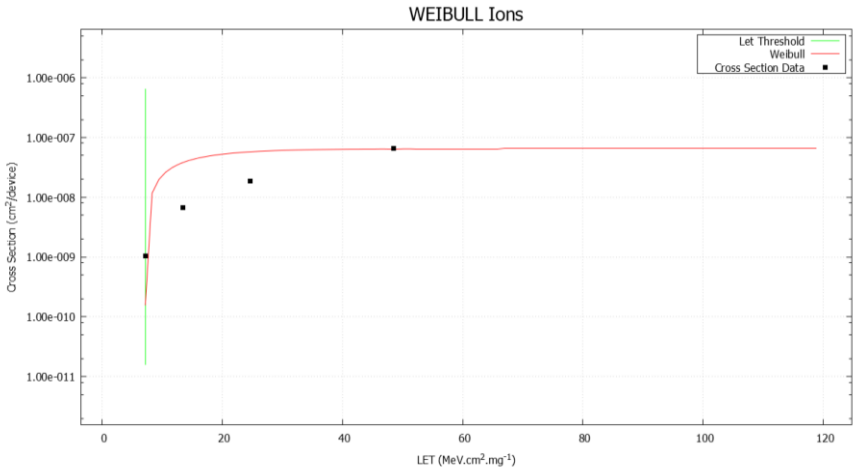


	Num. of DUT counters	Max counter Value	Reset	Max clock	SEU lock-up protection
Counter Array 1	16	200	async	100 MHz	On
Counter Array 2	16	200	async	100 MHz	Off

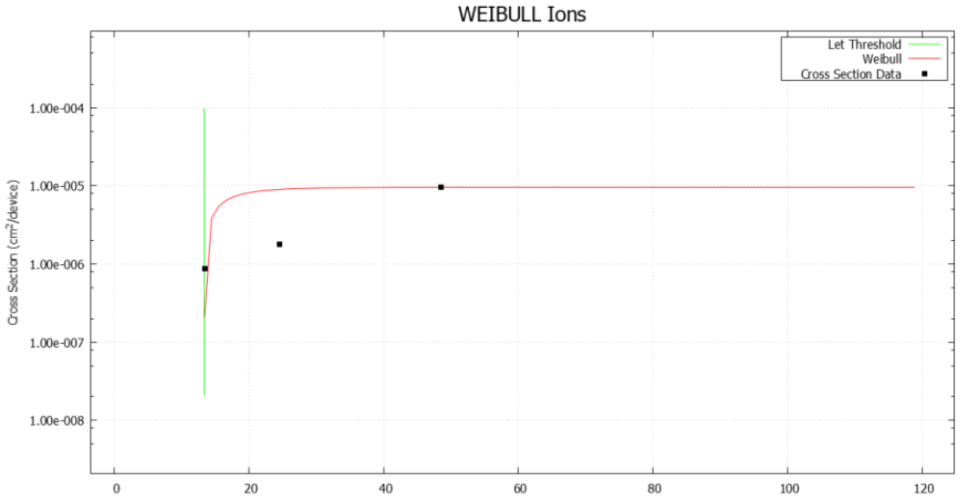
Radiation testing Heavy ions results - Counters

- Both counter arrays got errors during the tests. The number of errors were mainly in the range of 20 to 70. No significant differences were observed between the SEU lock-up protected array and the one without that mitigation.

- The Cross-Section plotted in the following figures represent the total number of counter errors, for a DFF SEU cross section translation, cross section must be divided by 16 shift registers and by 8 because the depth of the counter.



Counter Array with lock-up protection Weibull fit (per bit) as mean from 3 DUTS

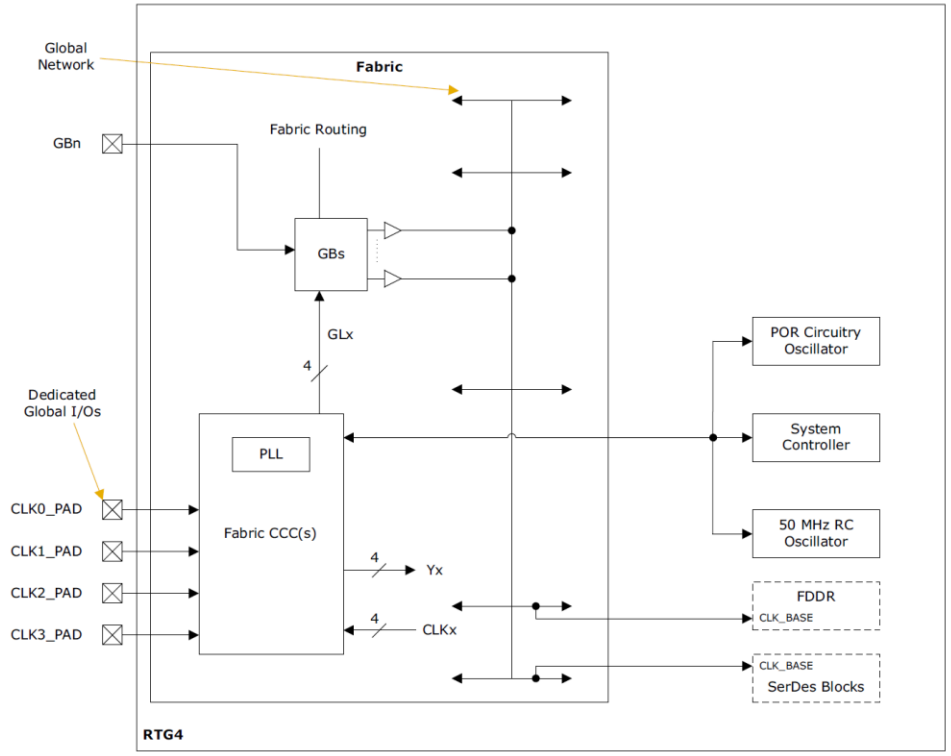


Counter Array without lock-up protection Weibull fit (per bit) as mean from 3 DUTS

Radiation testing Heavy ions results - CCC

- The aim of this test vehicle is to neglect the PLL block contribution in the CCC. The PLL core will be powered down and bypassed (by asserting PLL_BYPASS_N = ‘0).

- The 50 MHz on-chip oscillator (RC oscillator) is used as reference

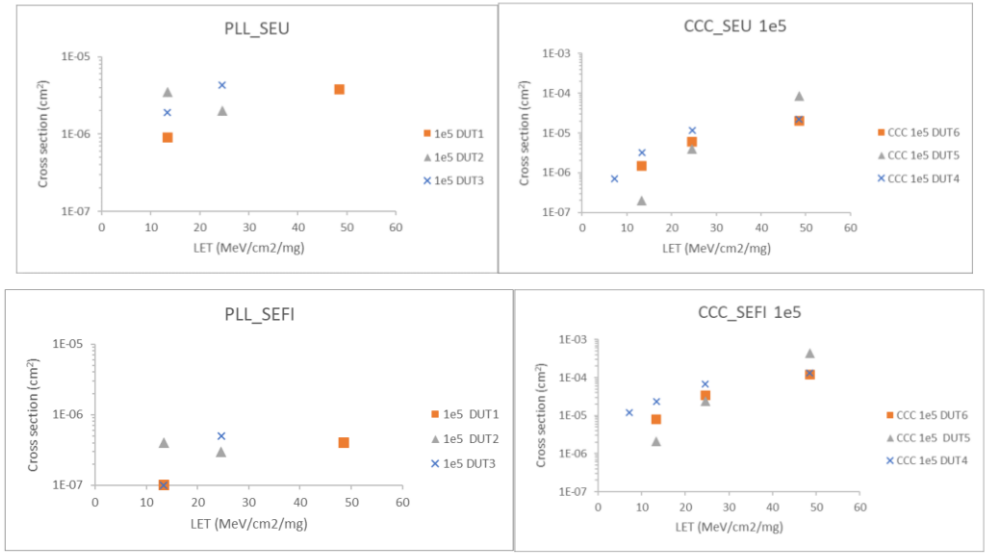


ARQUIMEA

Radiation testing Heavy ions results - CCC

- Two type of errors were monitored:
  - CCC_SEU
  - Recoverable CCC_SEFI (considered as three consecutive errors) .
- The number of errors were in the range of tens to hundreds in both cases

- Total SEU errors and SEFIS on the CCC are higher than in the PLL TV



Radiation testing Heavy ions results – CCSDS, SpW and CAN IPs

- These three IPs were tested implemented on the RTG4 devices

- Two instances of each of the IPs were instantiated, one just as the IP is provided (unhardened version) and another with the application of some further hardening techniques (hardened version). The differences between unhardened and hardened versions are the following:
  - Hamming-3 coding (at RTL VHDL level) in all Finite State Machines
  - SET filtering (by enabling this option in Libero SoC tool)
  - TMR (by setting Synplify attribute “syn_radhardlevel” to “tmr”)

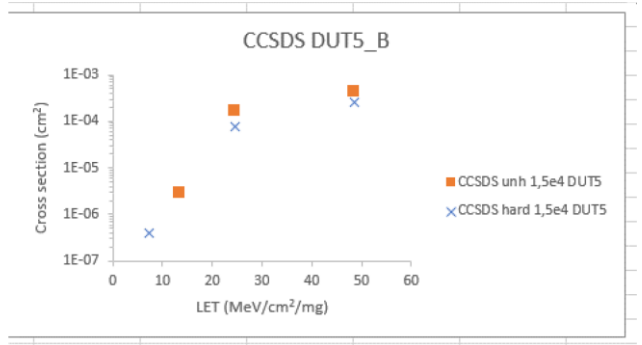
- The results are heavily dependent on the IP

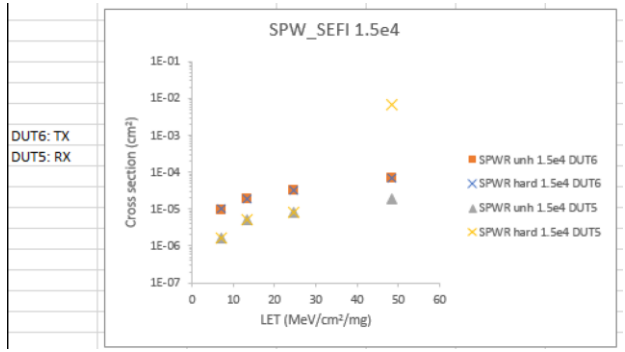
Radiation testing Heavy ions results – CCSDS, SpW, CAN IPs

- CCSDS: the number of errors were in the range of hundreds to thousands in both the unhardened and the hardened versions. The hardening slightly improves cross section for all DUTs and fluxes in the LET range of 10 to 30 MeV/cm2/mg (SET filtering).

- Spacewire: hardening efforts do not show a visible effect. Two types of errors monitored, SEU (one bit different in a frame) and SEFI (connection loss). The number of SEUs saturated the counters. The number of SEFIs (connection loss) was in the rage of hundreds to thousands.

- CAN: the number of errors was very low in all cases.





ARQUIMEA

Radiation testing Heavy ions results – ARM

- An ARM 0 test vehicle was also tested but the number of errors of the actual implementation was too big to get meaningful results

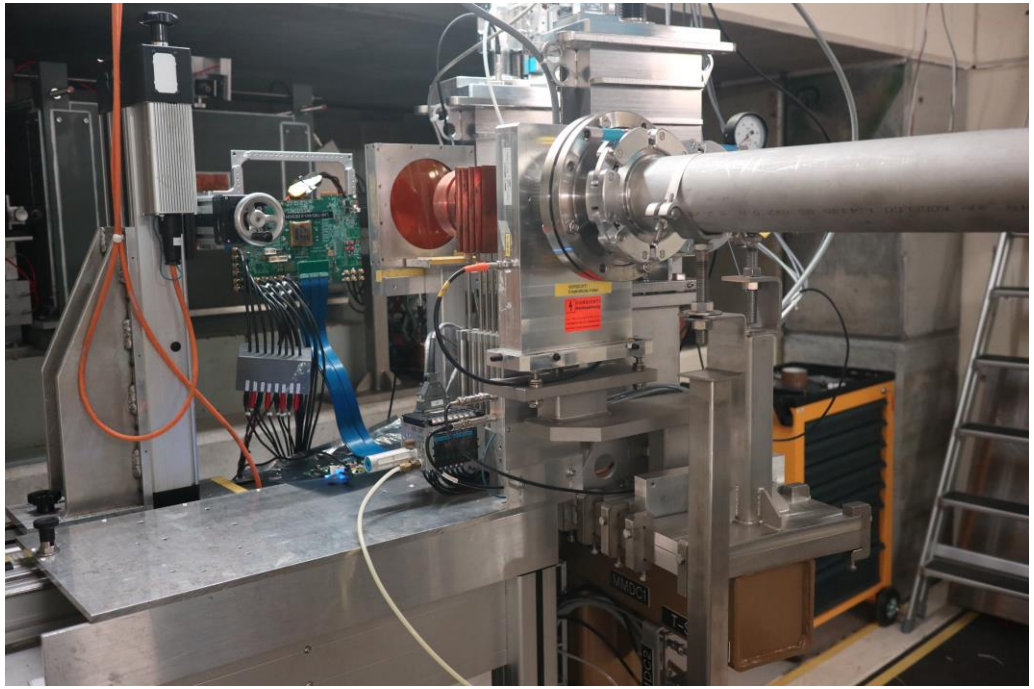
ARQUIMEA

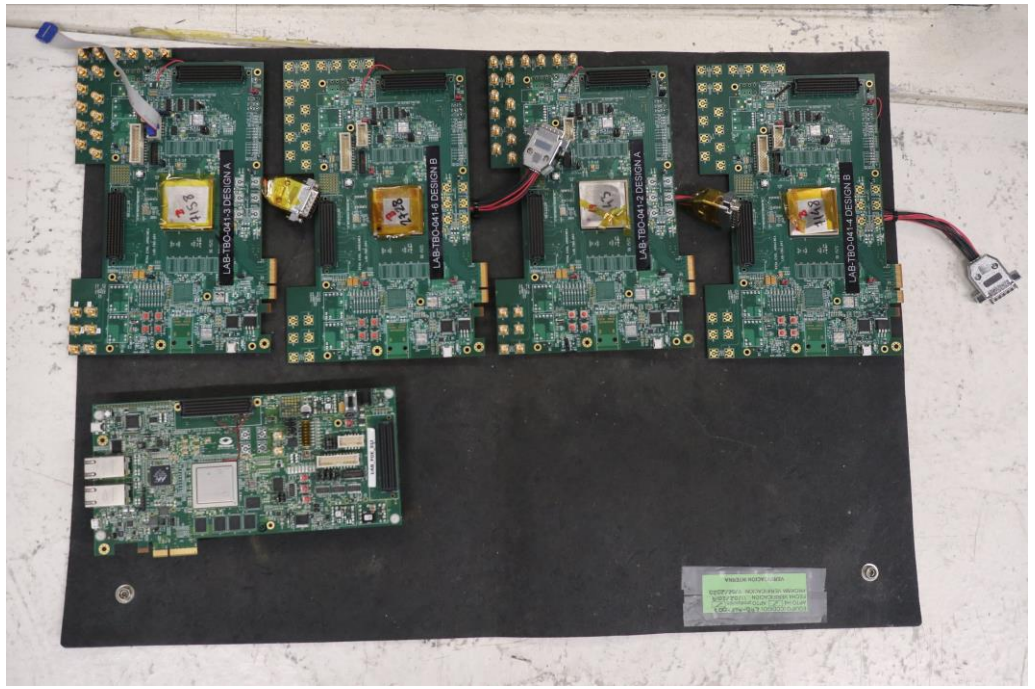
Radiation testing Heavy ions results – In beam programming

- In beam programming was also carried out but the results were not very successful. The flux used was excessive.
- Accelerated testing is suitable when errors are not time-dependent, but the programming task is restricted to a determined time so the flux cannot be set-up as high.

ARQUIMEA

Radiation testing Proton test at PSI





ARQUIMEA

Radiation testing Proton results

- The number of recorded errors was very low most of the test vehicles so no particular conclusions could be extracted
- The SERDES test vehicle only recorded two events on the PLL not locked error counter, 61 events on the TC error counter and 31 events on the RX error counter
- A few SETs have been observed in some tested pads both when checking the input to output connection as well as when checking just the output. Almost all the recorded SETs are wide.

	Mean number of SETs captured per DUT (PAD at High)	Mean number of SETs captured per DUT (PAD at Low)
I2OP_LVCMOS33	0	0
I2OP_LVCMOS25	0	1
I2OP_LVTTL33	0.5	0
I2OP_LVDS	0	0
I2OP_SSTL2_D	0.5	1
I2OP LVCMOS25 HS	0.5	0

Input to output pad SETs

	Mean number of SETs captured per DUT (PAD at High)	Mean number of SETs captured per DUT (PAD at Low)
OP_LVCMOS33	0	0
OP_LVCMOS25	0	0
OP_LVTTL33	0	0
OP_POR25	0	0
OP_LVDS	2	0
OP_SSTL2_D	2	0

Output pad SETs

ARQUIMEA

Radiation testing Proton results – In beam programming

- A number of In-Beam programming tests were carried out at PSI. The programming was successful for medium / low fluxes at any energy.

Program	Verify	Flux	Energy
Fail		2,377E+11	200.00
Fail		2,372E+11	200.00
Fail		2,398E+11	200.00
Fail		2,074E+10	200.00
Pass	OK	2390000000	200.00
Pass	OK	2252000000	200.00
Pass	OK	2,337E+10	200.00
Pass	Error	8,704E+10	50.80
Pass	Error	8,874E+10	50.80
Pass	Error	8,878E+10	50.80
Pass	OK	8707000000	50.80
Pass	OK	8681000000	50.80
Pass	OK	8671000000	50.80
Fail		8,39E+10	50.80
Fail		7448000000	50.80
Fail		2,31E+10	200.00
Pass	OK	2,313E+10	200.00
Fail		2,305E+10	200.00
Pass	Error	1,878E+10	151.18

ARQUIMEA

Radiation testing Lessons learnt

- **Test setup**
  - Screw type connectors and rigid cables made a bit more complicated the exchanging of boards
  - Wrong mounting of a few boards required that the FPGA balling had to be reworked
  - Equipment had to be left at PSI because of contamination and later had to be imported back since in was taken there as hand luggage.
- **Hardware design description**
  - Dedicated test equipment for CAN and SpW would have allowed more observability
  - Error counters register size was not big enough in some cases
  - Consider beforehand the effects of SEFIS on regular SEU counters
  - In beam programming at realistic flux

Radiation testing Conclusions (I)

- The radiation performance of the RTG4 FPGAs reported in previous reports was confirmed
  - For the main FPGA internal building blocks two main regions of operation are clearly identified:
    - At lower energies the number of errors is smaller and the SET filtering feature improves significantly the performances
    - At higher energies the number of errors is bigger and the SET filtering has no effect (being therefore the SEU the dominating factor).
  - The SET filtering feature also improves the performances at high frequencies where the SET events have a higher impact.
  - The results of other FPGA fabric building blocks like the PLL and the SERDES are also in line with the ones reported in the literature. The PLL presents some SET and SEFI sensitivity but with a cross section good enough for most of the applications whereas the SERDES presents a big casuistic of error types with a degraded BER under radiation, including a complex scenario of SEFIs.
  - In beam programming has also been tested concluding that with low fluxes, the reprogramming of the parts can be done at various energy levels .

Radiation testing Conclusions (II)

- The testing performed in this activity shows some results that had not been previously reported:
  - SETs have been observed in all the tested pads both when checking the input to output connection as well as when checking the outputs fixed at a constant value. Many of those SETs have a width below 10 ns however very wide pulse transients have been recorded as well.
  - The POR circuitry was routed to a pad in order to characterize its radiation performance and a few SETs were observed as well. Nevertheless, it cannot be fully confirmed if all measured SETs on this test vehicle are related to the actual POR or the pad. Further investigations on this matter are recommended.
- As for the investigations found on the IPs, it was confirmed that the radiation performance is quite dependent on the design and the observability/recoverability of the potential errors.

Radiation testing future work

- Further testing on the parts (the ones used, and the ones left as spare) could be easily conducted in the future based on the developed setups in order to get further knowledge on this technology. In particular:
  - Other I/Os types can be investigated against SETs
  - The POR circuitry can be carefully analyzed and radiation tested
  - More ad-hoc tests on the SERDES could be implemented
  - The ARM0 test vehicle could be checked including memory scrubbing
  - In beam programming at low flux in Heavy Ions
  - Perform CAN and SpW testing with external equipment

Questions? – Thank you!

Marta Portela

marta.portela@uc3m.es

Daniel González

dgonzalez@Arquimea.com

ARQUIMEA

Passion for technology

www.arquimea.com

Daniel González
CTO/COO
dgonzalez@arquimea.com
+34 607527275

ARQUIMEA INGENIERÍA, SLU
c/ Margarita Salas 10, 28918 Leganés (Madrid) – ES
Tel.: +34 91 689 80 94 / sales@arquimea.com

ARQUIMEA DEUTSCHLAND GmbH
Im Technologiepark 1, 15236 Frankfurt (Oder) – DE
Tel.: +49 335 557 1717 / sales@arquimea.com