Space PowerLink, Phase 1

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Thales Alenia Space

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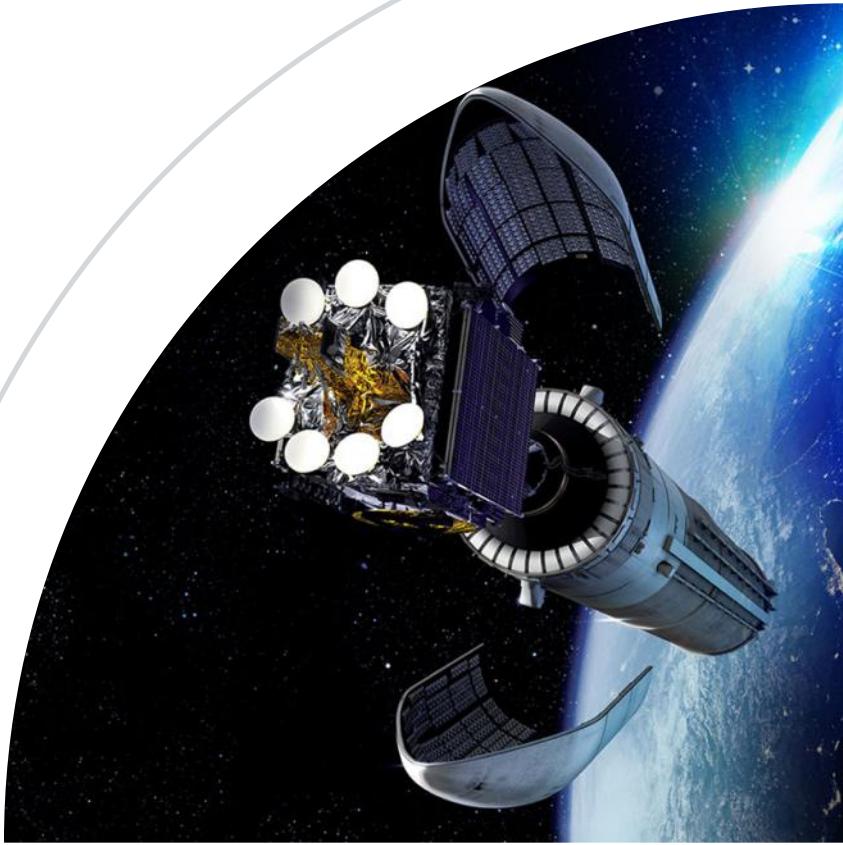
Background and Context



Background & Context

Current spacecraft architectures use centralised monitoring of a large number of discrete lines and separate power lines,.

- this leads to a bulky and heavy harness (e.g. up to 15% of dry mass) with congestion at the centralized unit i.e. RIU

Courtesy to Bepi-Colombo

Courtesy of EarthCare

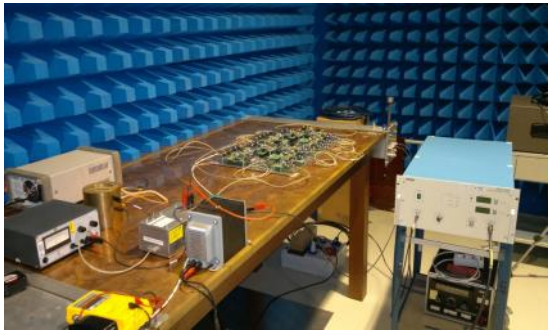
	ExoMars (small)		Bepicolombo (Medium)		Rosetta (Large)	
S/C Total Mass	200Kg		1150Kg		1500Kg	
S/C Total Power	200W		500W		2000W	
	Mass	Power	Mass	Power	Mass	Power
Centralised (inc. redundancy)	8.75Kg	3.65W	29Kg	9.13W	163.4Kg	33.6W
Decentralised (inc. redundancy)	4.75Kg	4.28W	11.2Kg	9.88W	52.2Kg	33.3W
Change	-4Kg	+0.63W	-17.8Kg	+0.75W	-111.2Kg	-0.3W
Change (%)	-45.7%	+17.3%	-61.4%	+7.6%	-68.1%	-0.9%
	% of S/C	% of S/C	% of S/C	% of S/C	% of S/C	% of S/C
Centralised	4.4%	1.8%	2.5%	1.82%	10.9%	1.68%
Decentralised	2.4%	2.1%	1%	2%	3.5%	1.67%
Change	-2%	+0.3%	-1.5%	+0.18%	-7.4%	-0.01%

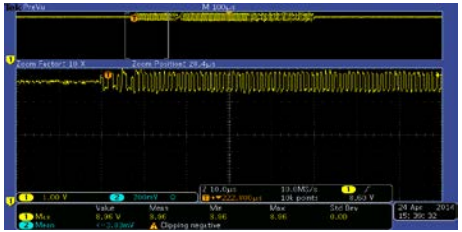
Initial TRP Activity

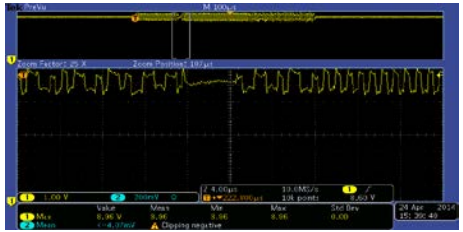
TRP Activity “Power Link: Two-Wire Power and Data Link” (4000112415/14/NL/LF)

- the proof of concept of Mix of data and power lines technology
- TRL2
- Preliminary specification of this new technology

Completed 2015







Summary Objectives of Powerlink

Phase 1:

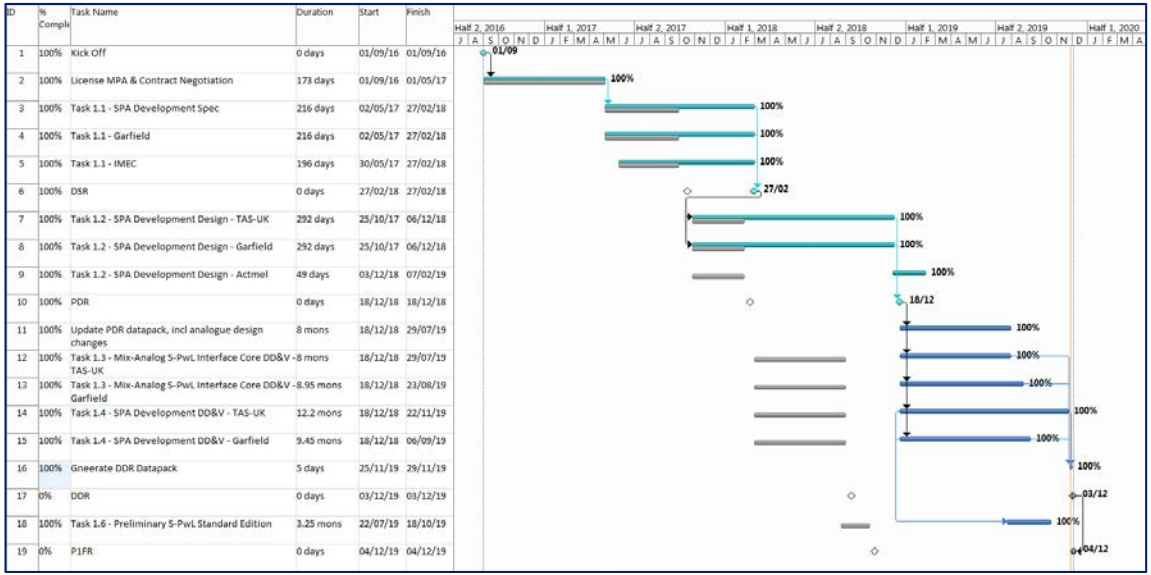
- The design the S-PwL Controller/Terminal ASIC (i.e. SPA device), including a Mixed-Analog S-PwL Interface Core and the issue of a baseline SPT specification for standardisation (i.e. objectives of Phase 1 of the current activity)

Phase 2:

- The manufacturing, characterisation and radiation testing of the SPA device and the issue of a final S-PwL-T specification for standardisation (i.e. objectives of Phase 2 of the current activity). The final device shall be a fully-fledged space qualified device

Phase 1 only has been completed to date

Schedule & Review Status



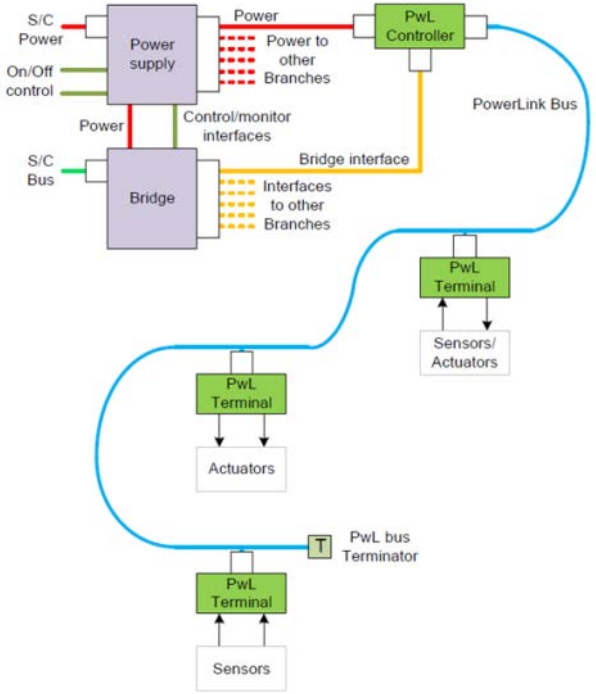
ID	% Complete	Task Name	Duration	Start	Finish
1	100%	Kick Off	0 days	01/09/16	01/09/16
2	100%	License MPA & Contract Negotiation	173 days	01/09/16	01/05/17
3	100%	Task 1.1 - SPA Development Spec	216 days	02/05/17	27/02/18
4	100%	Task 1.1 - Garfield	216 days	02/05/17	27/02/18
5	100%	Task 1.1 - IMEC	196 days	30/05/17	27/02/18
6	100%	DSR	0 days	27/02/18	27/02/18
7	100%	Task 1.2 - SPA Development Design - TAS-UK	292 days	25/10/17	06/12/18
8	100%	Task 1.2 - SPA Development Design - Garfield	292 days	25/10/17	06/12/18
9	100%	Task 1.2 - SPA Development Design - Actmel	49 days	03/12/18	07/02/19
10	100%	PDR	0 days	18/12/18	18/12/18
11	100%	Update PDR datapack, incl analogue design changes	8 mons	18/12/18	29/07/19
12	100%	Task 1.3 - Mix-Analog S-PwL Interface Core DD&V - TAS-UK	8 mons	18/12/18	29/07/19
13	100%	Task 1.3 - Mix-Analog S-PwL Interface Core DD&V - Garfield	8.95 mons	18/12/18	23/08/19
14	100%	Task 1.4 - SPA Development DD&V - TAS-UK	12.2 mons	18/12/18	22/11/19
15	100%	Task 1.4 - SPA Development DD&V - Garfield	9.45 mons	18/12/18	06/09/19
16	100%	Gneerate DDR Datapack	5 days	25/11/19	29/11/19
17	0%	DDR	0 days	03/12/19	03/12/19
18	100%	Task 1.6 - Preliminary S-PwL Standard Edition	3.25 mons	22/07/19	18/10/19
19	0%	P1FR	0 days	04/12/19	04/12/19

Milestone	Date
Kick-off	01/05/2017
Development Specification Review	27/02/2018
Preliminary Design Review	18/12/2018
Detailed Design Review	03/12/2019
Phase 1 Final Review	03-04 Dec 2019

Schedule delays caused by the following:

- Completion of the trade-off, identified that a change in foundry was required. This took extensive time to confirm library and IP Core requirements
- Long term sickness of the Lead Engineer, prior to replacement and handover of the role

Architecture, Requirement and Trade-off



Date 12/05/2020

Ref. = Space Powerlink SET-PFD

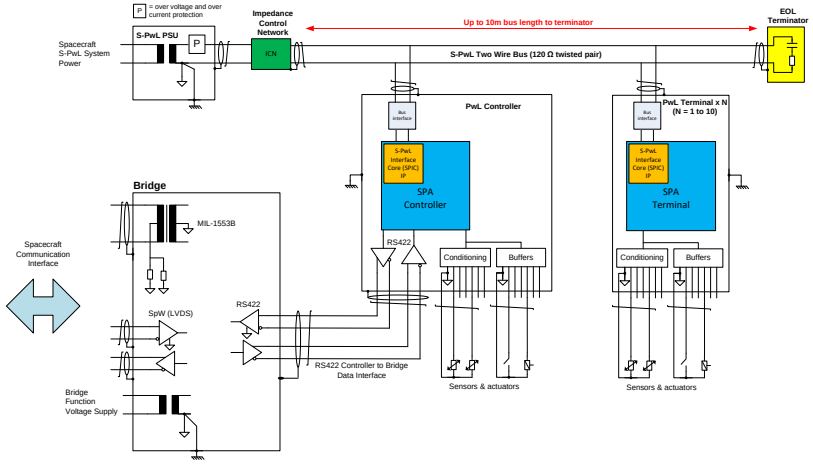
Space Powerlink System Context*

S-PwL is based on a unified medium for the power distribution and communication.

- The S-PwL Bus transports both the power and the data exchanges over only 2 wires.

The S-PwL bus supports up to 10 Terminals, each bus is called an S-PwL Branch. Consisting of:

- 1 off S-PwL PSU voltage output with over voltage and over current protection
- 1 off S-PwL Impedance Control Network (ICN)
- Up to 10m of S-PwL cable (100 Ω twisted pair)
- 1 off S-PwL Controller
- Up to 10 off S-PwL Terminals
- 1 off S-PwL End of Line (EoL) terminator
- 1 off S-PwL Bridge to interface the PwL Controller with the Spacecraft Data Handling System



Single S-PwL Branch Overview

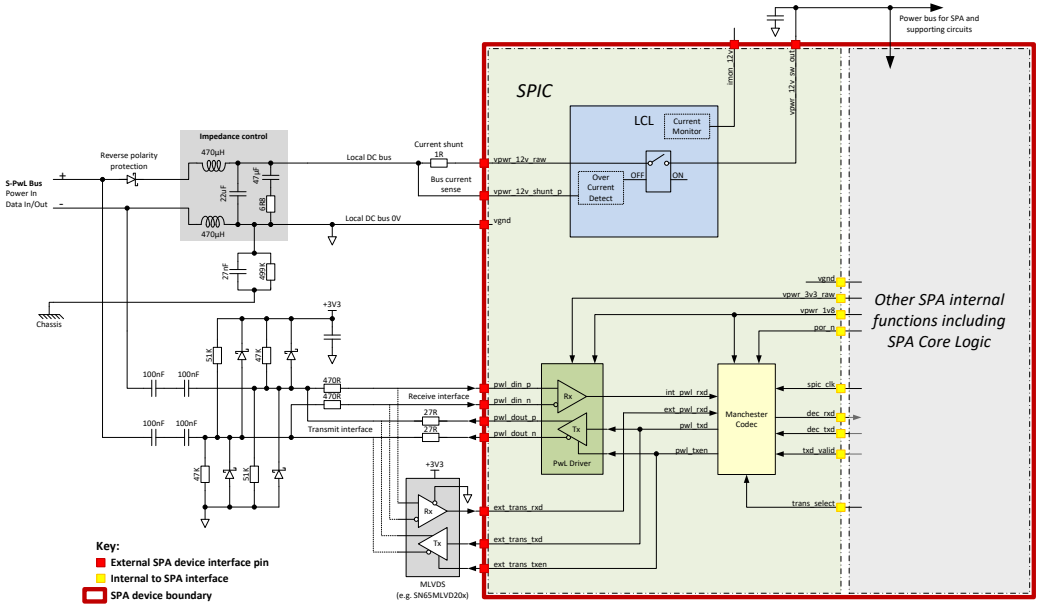
* This would constitute the basis of the future activity (SPwL Ecosystem) to be developed to validate the Space Powerlink Standard

Space Powerlink Interface Controller (SPIC)

The SPIC is an IP Core integrated into the Space-PowerLink ASIC (SPA).

The SPIC is the physical layer interface between the user designed functions within the ASIC and the S-PwL Bus.

- The SPIC is used as a bus interface for both ASIC configurations of an S-PwL Controller and the S-PwL Terminals
- Used within the Space PowerLink ASIC (SPA), for implementation of an S-PwL Controller and a Terminal.



S-PwL Bus Interface to SPIC functions

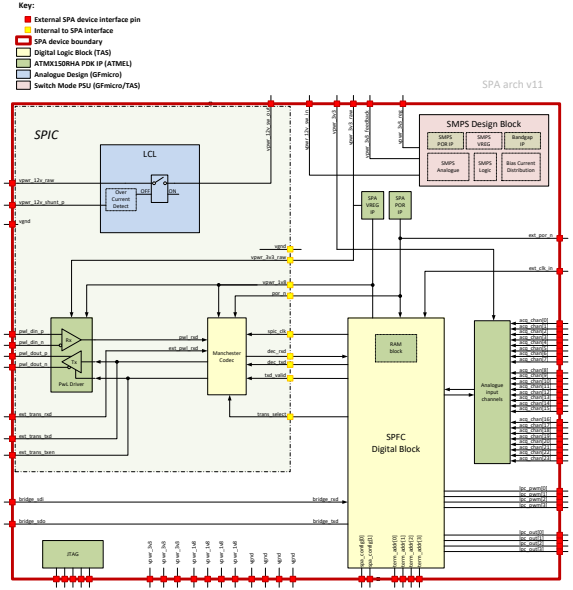
Space Powerlink Device

The Space PowerLink ASIC (SPA) is divided into two parts:

- S-PwL Interface Core module (SPIC)
- S-PwL Functional Core (SPFC)

The SPFC contains the following blocks:

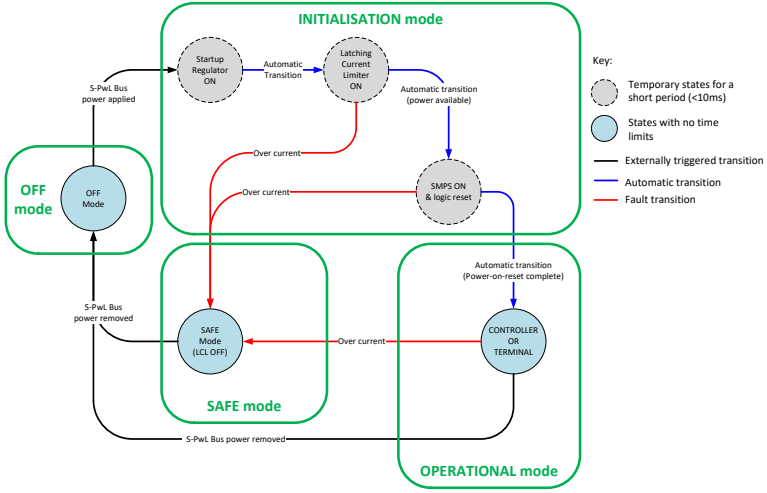
- Switched Mode Power Supply
- Voltage regulator
- Power On Reset
- Digital Block
- Analogue input channel block
- JTAG



SPIC and SPA functional blocks and interfaces with SPIC

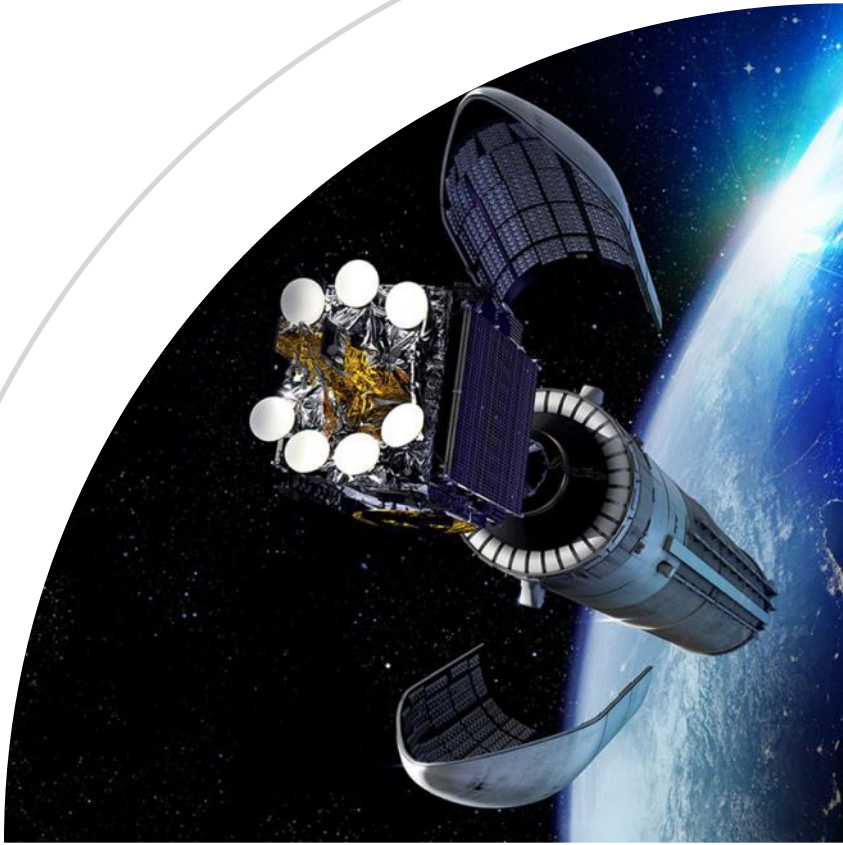
SPA Modes of Operation

Mode	Description
OFF	• Initially the SPA starts in the OFF Mode with no bus power.
INITIALISATION	• After the bus power is applied by the S-PwL PSU it enters the INITIALISATION Mode • The SPA stays in the INITIALISATION Mode until the bus has reached a certain level and the LCL switches ON • A Power On Reset function produces a global reset for a period to initialise all logic and allow time for the global clock to become established
OPERATIONAL	• After the power on reset is released the SPA enters the OPERATIONAL Mode • In the OPERATIONAL Mode the SPA is configured to operate either as a Controller or as a Terminal configuration • In OPERATIONAL Mode the SPA is functioning normally and S-PwL packets can be exchanged between the Controller and Terminals on the S-PwL bus. • If the bus power is removed from the S-PwL bus then the SPA enters the OFF mode.
SAFE	• If an LCL trip occurs the LCL latches into the OFF state and the SPA enters the SAFE mode. In this state the SMPS is OFF but the power is still present at the input to the LCL. The LCL will not reset to the ON state until the S-PwL bus power is cycled OFF and then ON again.



SPA mode diagram

SPIC – Detailed Design

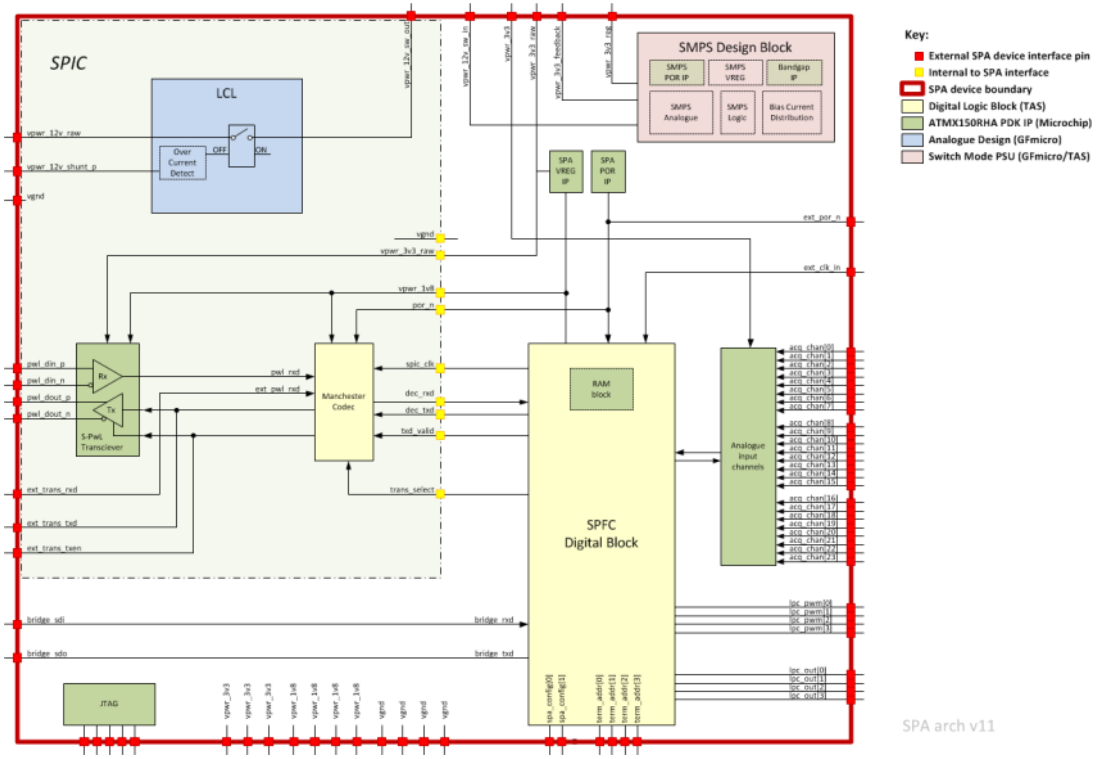


Main Features

Name	Space PowerLink ASIC (SPA)
Complexity	NA
Working Frequency	16MHz with sub-divided synchronous domains.
Technology	Microchip 150nm
Matrix	7 x 7mm (worst-case estimate)
Package	CQFP 208 (prototype)
Useful pins	87 including supplies, reset, test etc
Core Power Supply Voltage	1.8V. Note that the ASIC is designed to run from two supplies, 3V3 Analogue and 3V3 Digital.
Periphery Power Supply Voltage	3V3
Core Power Consumption	50mW (TBC) dominated by SMPS efficiency
Periphery Power Consumption	100mW (TBC) dominated by digital I/O load currents supplied to external devices
Test (full-scan, functional test)	JTAG

Note: To be updated at CDR and TRB

SPA functional architecture

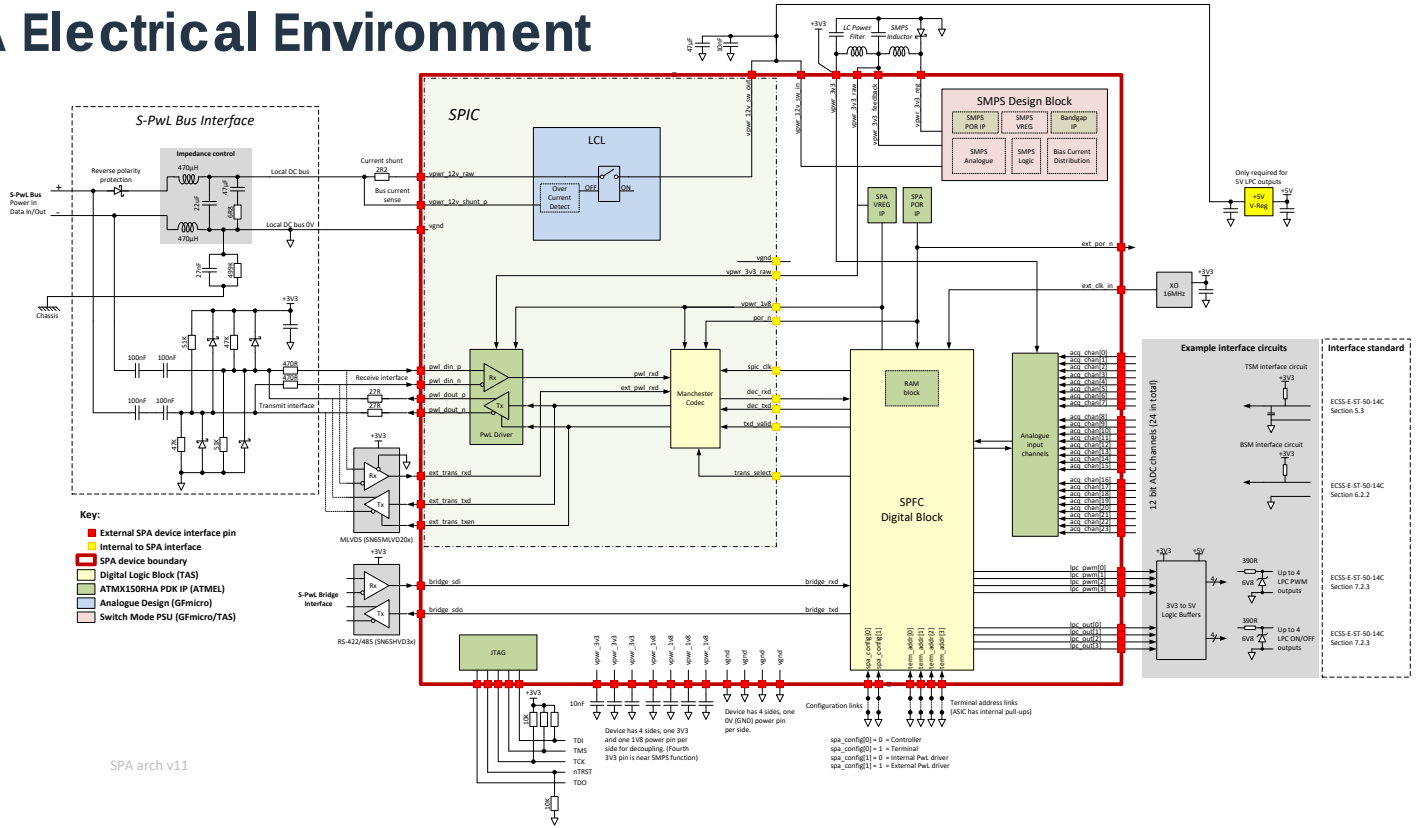


SPA arch v11

Date 12/05/2020

Ref. = Space Powerlink SET-PFD

SPA Electrical Environment



Date 12/05/2020

Ref. = Space Powerlink SET-PFD

Key ASIC Functions

SPIC containing:

- LCL IP providing over-current protection (Designed during Phase 1 by GF Micro)
- S-PwL Data Transceiver – Microchip PDK library element
- Manchester Encoder/Decoder (S-PwL Codec TASUK IP)

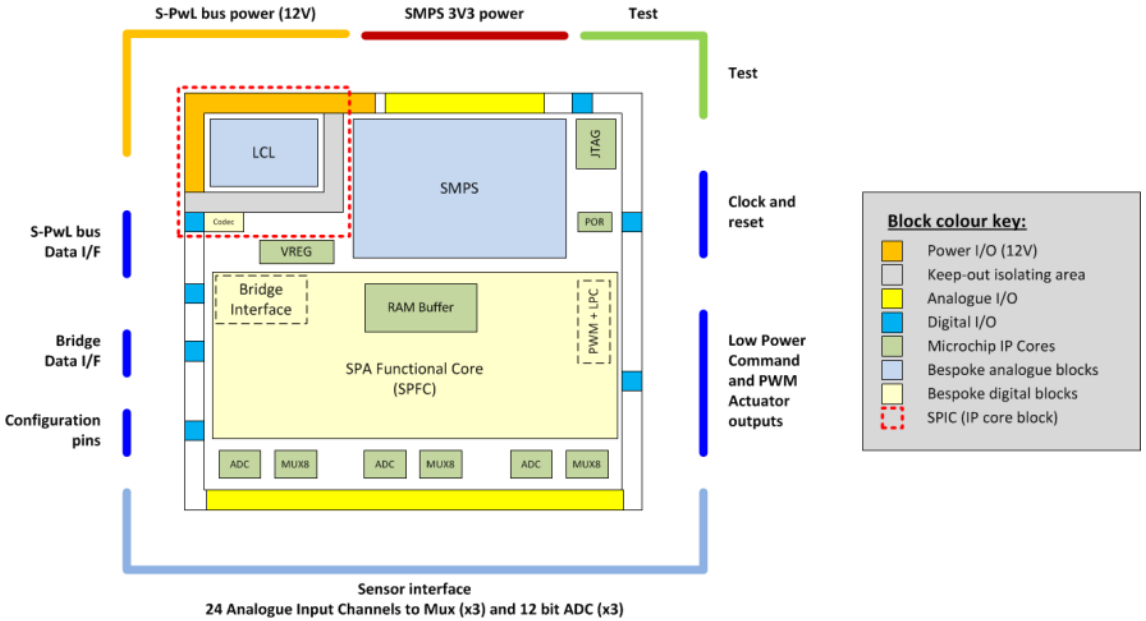
SPA Functional Core comprising:

- Switched Mode Power Supply (SMPS) (Designed by GF Micro)
- Voltage Regulator (VREG) (Microchip IP core)
- Power On Reset (POR) (Microchip IP core)
- S-PwL Functional Core (SPFC) (TASUK VHDL + Microchip memory IP core)
- 24 analogue Input Channels (Microchip ADC and multiplexer IP cores)
- Analogue inputs are digitally filtered
- 4 PWM outputs with 8 bit resolution
- 4 bi-level on/off outputs
- JTAG test interface (Microchip or GF Micro IP core)
- Separate 3.3V digital and 3.3V analogue power rails for noise isolation

Layout approach Floorplan

The driving requirements for the layout are:

- High and low voltage segregation
- Power and analogue segregation
- S-PwL bus interfaces positioned close together
- Analogue inputs positioned away from digital I/O and away from “noisy” power rails



Space Powerlink: Preliminary Standard

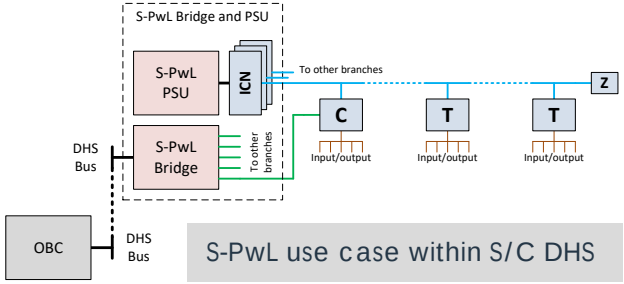
Space PowerLink Standard - summary

Document section breakdown and content based on:

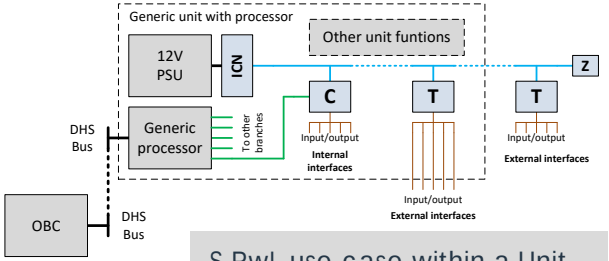
- SpaceWire standard
- Mil-STD 1553B standard

Content for both S-PwL and Bridge Interfaces:

- Overview – including spacecraft application context
- Use Cases
- Physical Level
- Power and Signal Level
- Character and Exchange Levels
- Packet Level including CRC
- Network Level
- System level behaviour
- Fault management and Error Handling

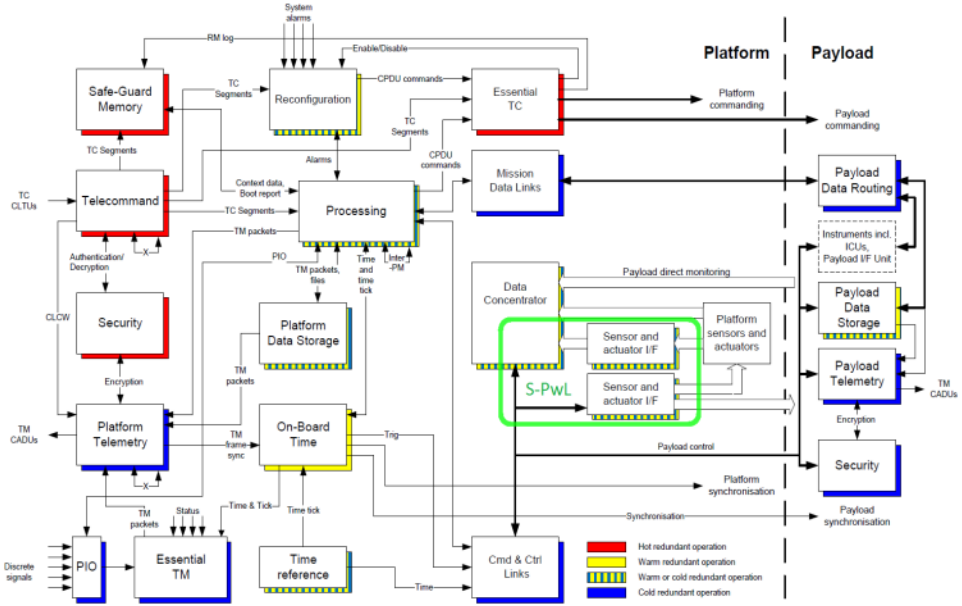


S-PwL use case within S/C DHS

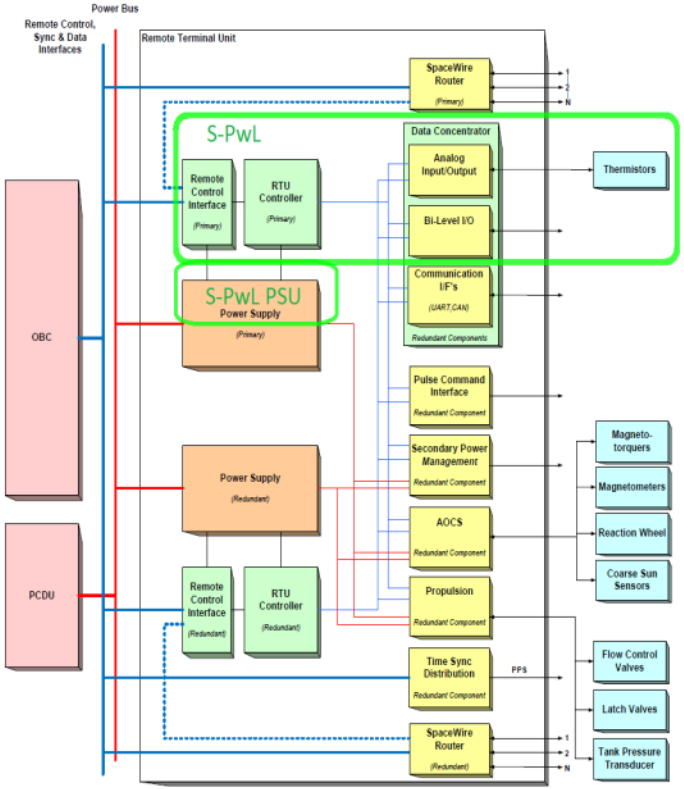


S-PwL use case within a Unit

S-PwL application in S/C context

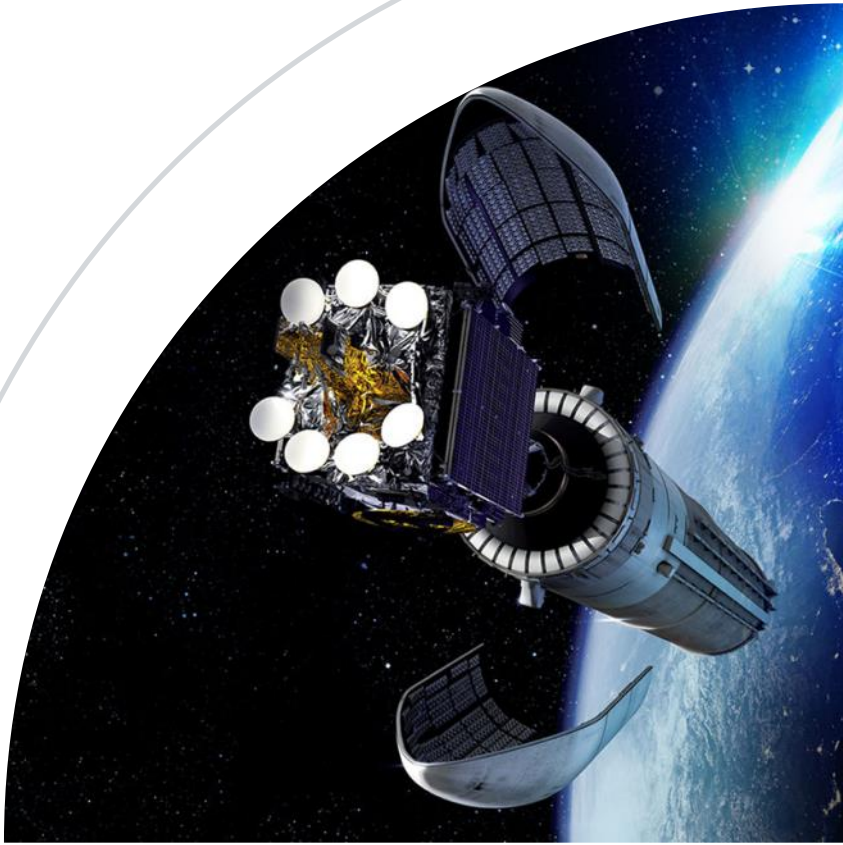


SAS-PwL context within SAVOIR



SAS-PwL context within S/C DHS

Conclusion & Next Steps



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Conclusion

Phase 1 of the Space Powerlink contract has been completed, with all objectives achieved, noting the following:

1. The formal architecture for the SPA has been optimised and associated requirements for the SPA and SPIC have been aligned accordingly.
2. ASIC foundry confirmed as Microchip ATMX150RHA IP Core and Library
3. The LCL, within the Interface Core, has been assessed and defined allowing the analogue design and verification to proceed
4. Digital block generated and verified
5. Block layout of the ASIC generated, and device verification outlined
6. Preliminary Space-Powerlink Standard generated
7. Current SPA design is based on preliminary datasheets for Microchip IP blocks
8. The overall SPA detailed design is complete with respect to the Phase 1 negotiated objectives and considered mature for Phase 2 initialisation

Questions

The Thales Alenia Space UK team would like to thank the European Space Agency for their support and assistance