Generation of a Testbed for the Validation of the TTEthernet Technology

TEC-ED & TEC-SW Final Presentation Days

13/05/2020

Generation of a Testbed for the Validation of the TTEthernet Technology

- *Budget:* 980 kEUR

- *Duration:* 24 Months

- *Prime:* Airbus DS Bremen

- *Main Objectives:*

  1. To design and develop a modular integrated and representative testbed intended to test TTE based End System;

  2. To Design and develop a TTE End System using COTS components that have counterpart in space grade where possible

Generation of a Testbed for the Validation of the TTEthernet Technology

3. The testbed will be able:

-To accommodate Hardware In the Loop (HIL)

-To test and verify according to the standard the determinism, synchronisation & fault tolerance mechanisms of third party ES models

-To Assess the end to end communication performances (e.g. precisions);

4. The End System

The design of the TTE End System boards will include interfaces like SPW, SPI or LAN to connect a wider variety of units (sensor, PCDU, RIU, thermal control system or a Mass Memory);

GSTP : Generation of a Testbed for the Validation of the TTEthernet Technology

Final Presentation

DEFENCE AND SPACE

Bremen, Dec. 16th 2019

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Agenda

This presentation is divided in three major sub-chapters:

- Chapter #1 : Hardware Development and Programming within GSTP

- Chapter #2 : Test Cases and Test Results within GSTP

- Chapter #3 : Summary and Way Forward

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Chapter #1

Chapter #1 : Hardware Development and Programming within GSTP

- Project Overview

- Test Architecture Concept

- TTE Testbed

- TTE Testbed Software

- Airbus Crate

- Airbus Crate SW (LEON 4)

- Airbus Crate IP (Ref ES)
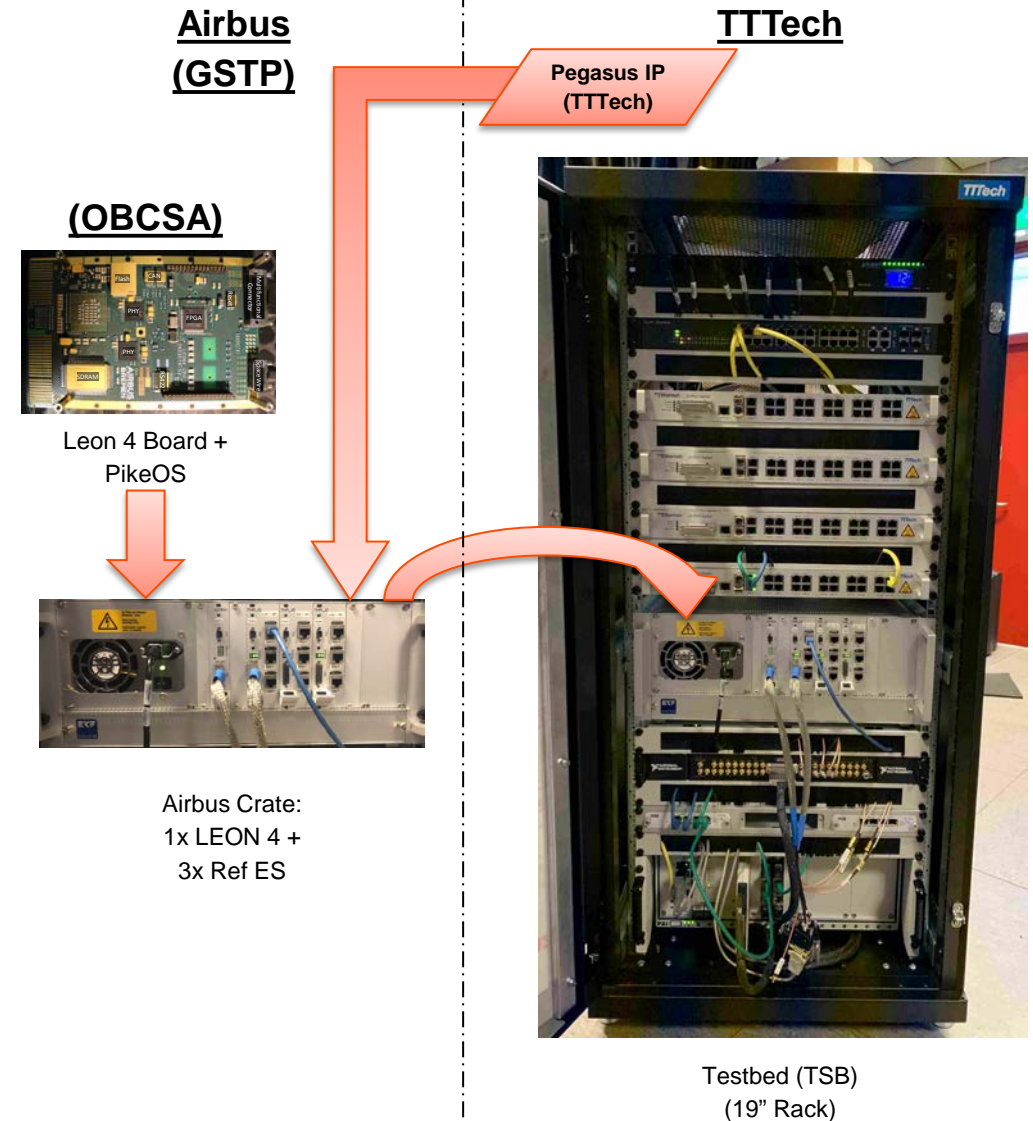
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Project Overview

GSTP : Generation of a Testbed for the Validation of the TTEthernet Technology

Contractor Number: 4000118781/16/NULF
Start: 11.11.2016
End: 15.11.2019
Prime: Airbus DS
Subcontractor: TTTech

Contribution: LEON 4 Board + PikeOS
Originator: OBCSA Project (DLR)

Project Scope :

• Maturation of TTE Technology
• Generate a Reference End System Card (Ref ES)
• Generate Testbed to stress TTE IP (Pegasus) in a Ref ES
• TTE speaking Thermal Sensor w/o LEON 4 host

Airbus (GSTP)

TTTech

Pegasus IP (TTTech)

(OBCSA)

Leon 4 Board + PikeOS

Airbus Crate:
1x LEON 4 +
3x Ref ES

Testbed (TSB)
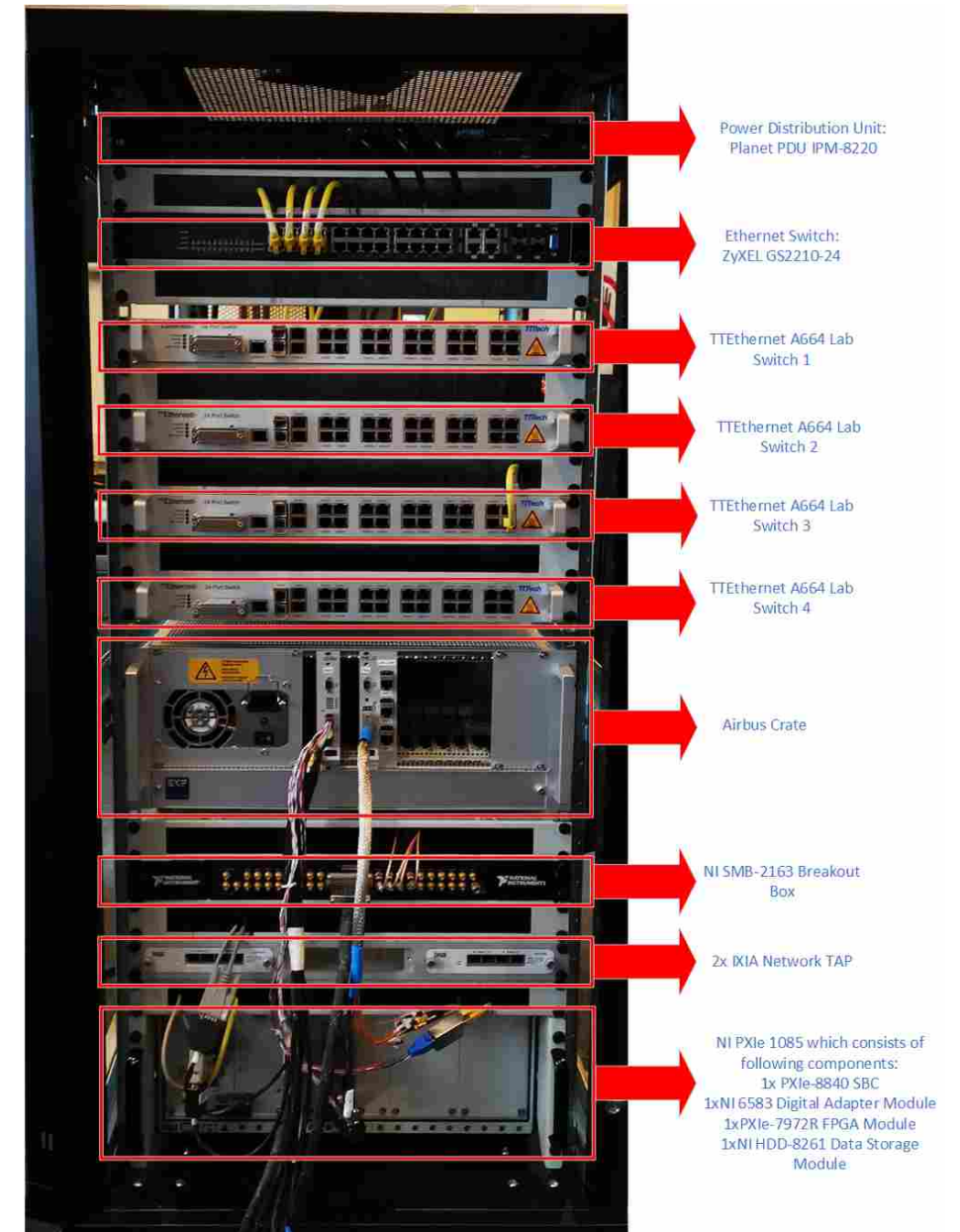(19" Rack)

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Test Architecture Concept

- Ref. End System (Ref ES):
  - 3x Virtex5 FPGA boards build the reference for TTE Protocol. TTE IP (Pegasus) has been integrated in the Ref ES
  - Ref ES+ TTE IP build the unit under test (UUT)

- LEON 4 Board (OBCSA):
  - Loaded with PikeOS (A653)
  - Includes the host function for the Ref ES/TTE IP Core
  - Builds the link between Testbed and UUT
  - Communicates via SPW / RMAP with Ref ES (backplane) and via RS232 with Testbed (TTTech)

- Temperature Sensor:
  - COTS temp sensor with SPI interface
  - Communicates to TTE IP Core directly (via LEON 3)

- Testbed (TSB):
  - Supervises all test (e.g. generate corrupt TTE traffic)
  - Controls TTE communication of Ref ES
  - Includes 4x TTE switches (not shown in figure)
  - Receives discrete status signals from Ref ES (4x DIO)
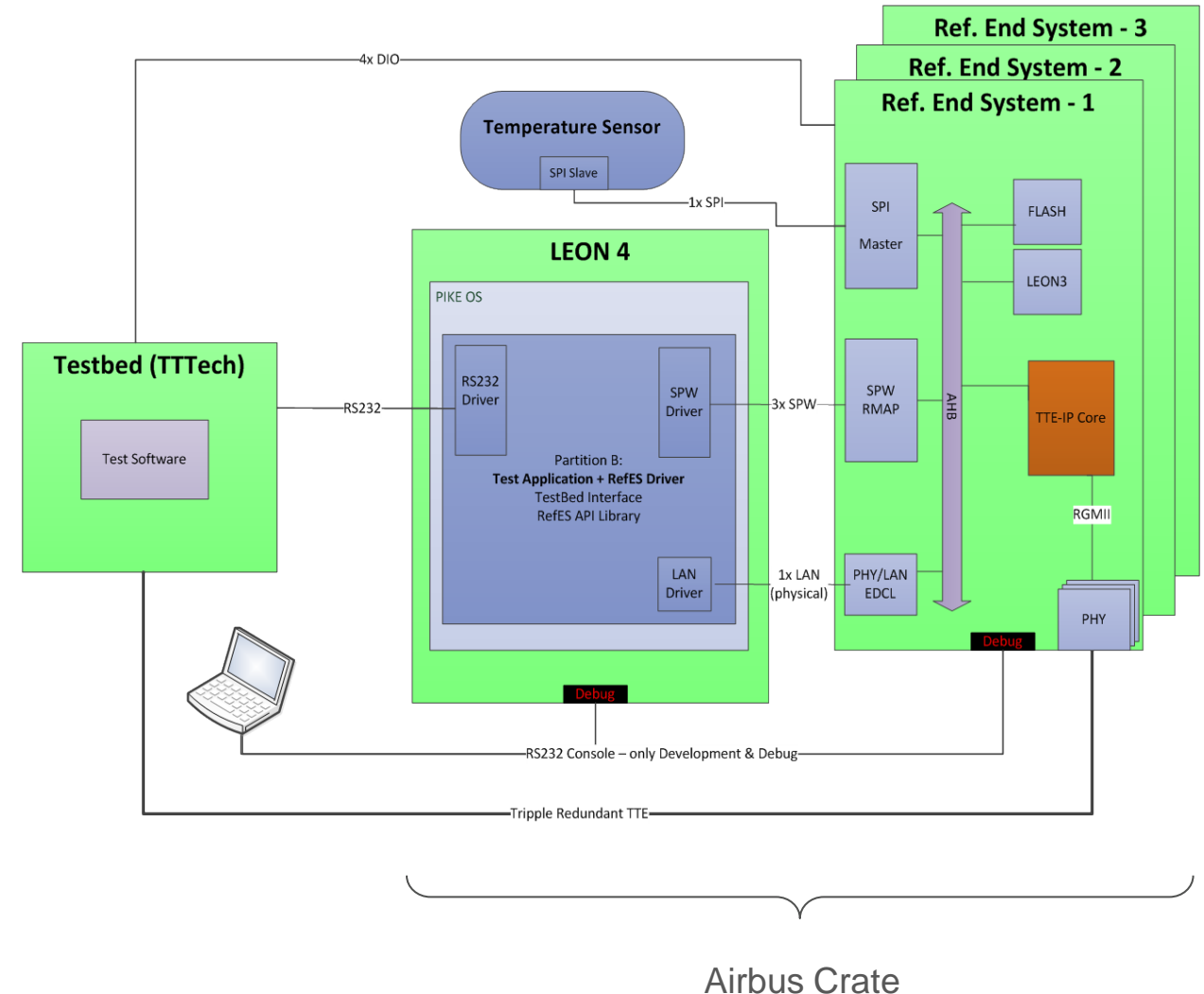
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TTE Testbed 1/2

19'' rack (Digitus DN-19-SRV-26U-B-G-1) which consists of :

- 1x Power Distribution Unit (Planet PDU IPM-8220)
- 1x Ethernet Switch (ZyXEL GS2210-24)
- 4x TTEthernet A664 Lab Switch
- 1x Airbus Crate
- 1x NI SMB-2163 Breakout Box
- 2x IXIA Network TAP
- 1x NI PXIe 1085 chassis

Power Distribution Unit:
Planet PDU IPM-8220

Ethernet Switch:
ZyXEL GS2210-24

TTEthernet A664 Lab Switch 1

TTEthernet A664 Lab Switch 2

TTEthernet A664 Lab Switch 3

TTEthernet A664 Lab Switch 4

Airbus Crate

NI SMB-2163 Breakout Box

2x IXIA Network TAP

NI PXIe 1085 which consists of following components:
1x PXIe-8840 SBC
1xNI 6583 Digital Adapter Module
1xPXIe-7972R FPGA Module
1xNI HDD-8261 Data Storage Module
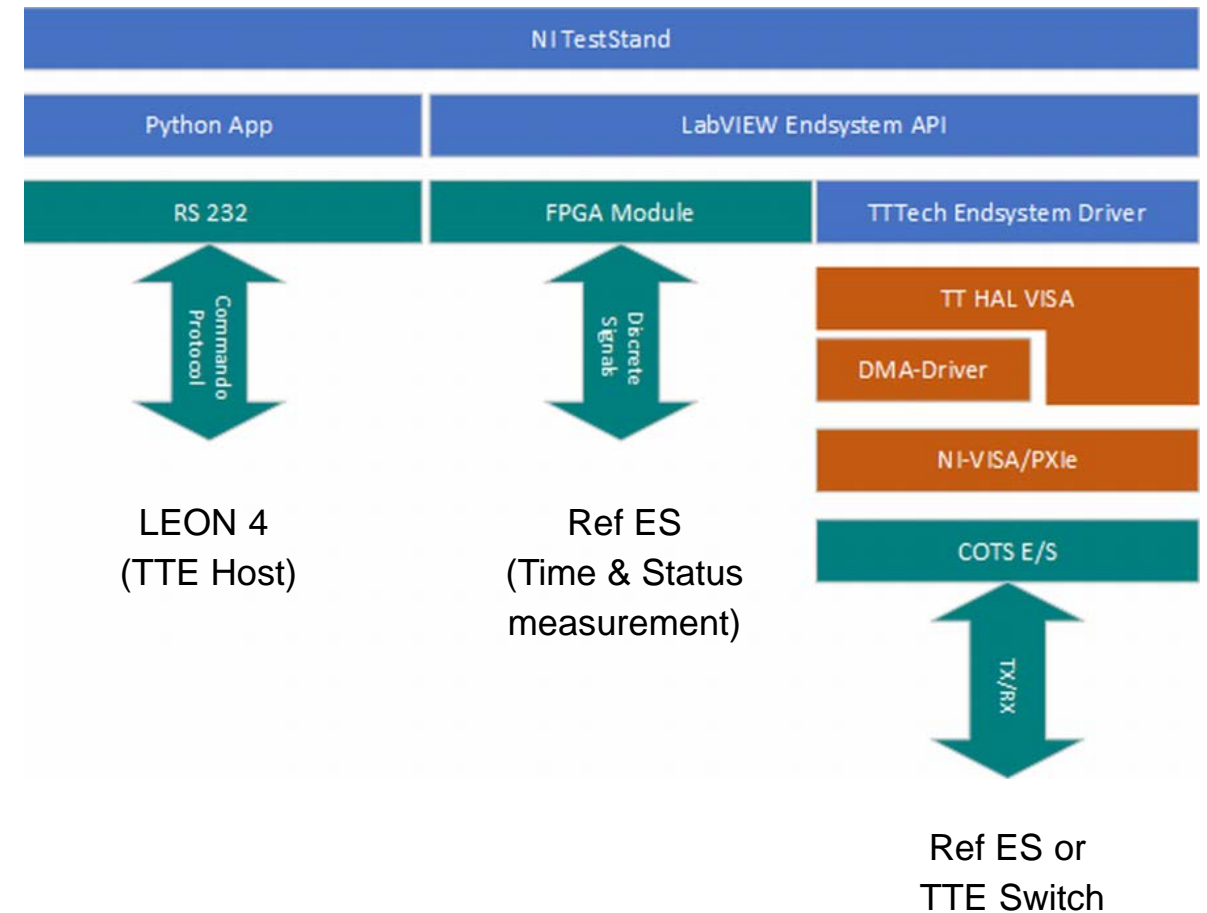
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TTE Testbed 2/2

1x NI PXIe 1085 chassis which consists of following modules:

- 1x NI PXIe-8840 SBC

- 1x NI 6583 Digital Adapter Module

- 1x NI PXIe-7972R FPGA Module

- 1x NI HDD-8261 Data Storage Module

- 2x 12610 TTE-End System A664 Lab (cPCIe , copper))

NI PXIe-8840 SBC

NI-SMB 2163

NI-PXIe 1085 chassis

NI 6583 Digital Adapter

PXIe-7972R FPGA Module

NI PXIe-1085

TTTech COTS cPCIe ES

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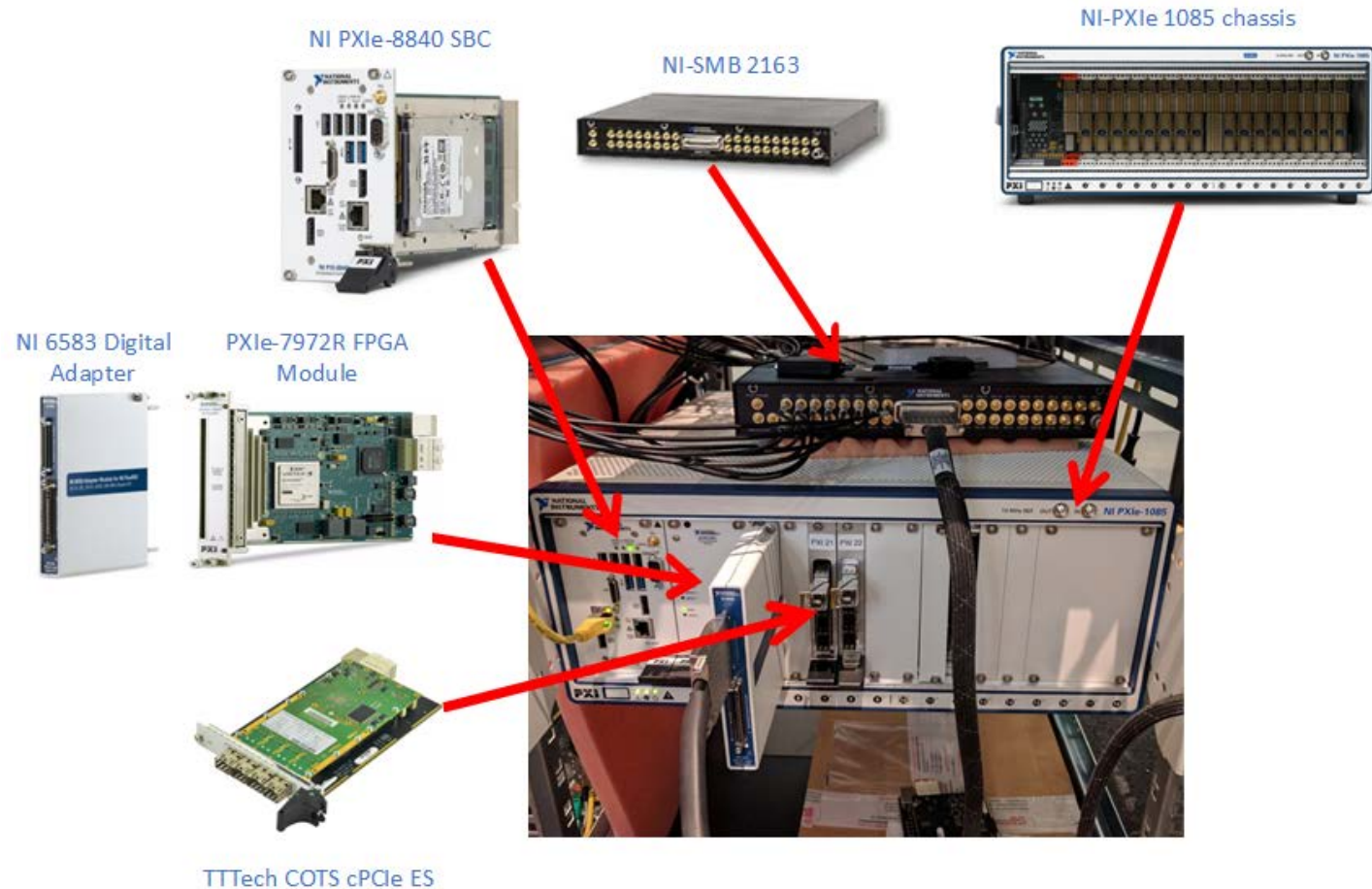
NI Crate SW (TTTech)

- Test control is done via Windows based PXIe-8840 SBC card with integrated NI TestStand

- Python App has been used to program the RS232 interface to LEON 4 processor

- LabVIEW has been used
  - to measure Ref ES synchronization status and timing
  - To generate TX/RX TTE traffic with COTS E/S (e.g. corrupted PCF)

- VISA (Virtual Instrument System Architecture) is a common API for instrument I/O, originally designed for laboratory automation buses.
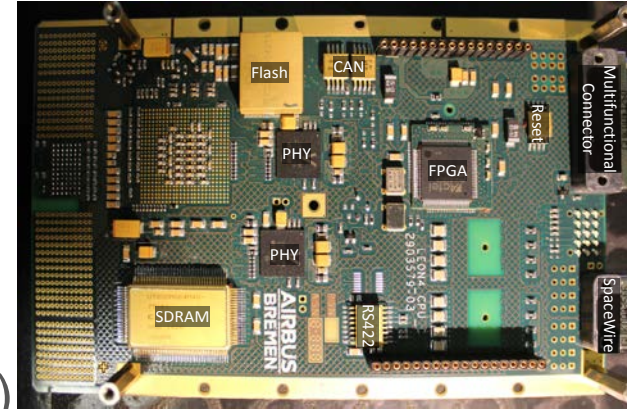
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Airbus Crate

HW Availability Airbus (Ref ES Crate):

- 1x Ref ES Crate (EKF, SRS-8421-Serial)
- 3x Ref ES FPGA boards (P/N: 2903580-02)
- 1x LEON 4 Processor Board (P/N: 2903579-0)
- 1x Thermal Sensor (MAX6675 v1.2)

– Screen / Keyboard were provided by ESA
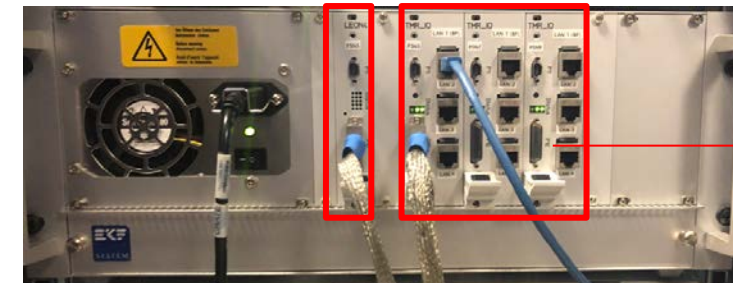– Remote Control of tests via LAN interface

LEON 4 Board

3x Reference End System
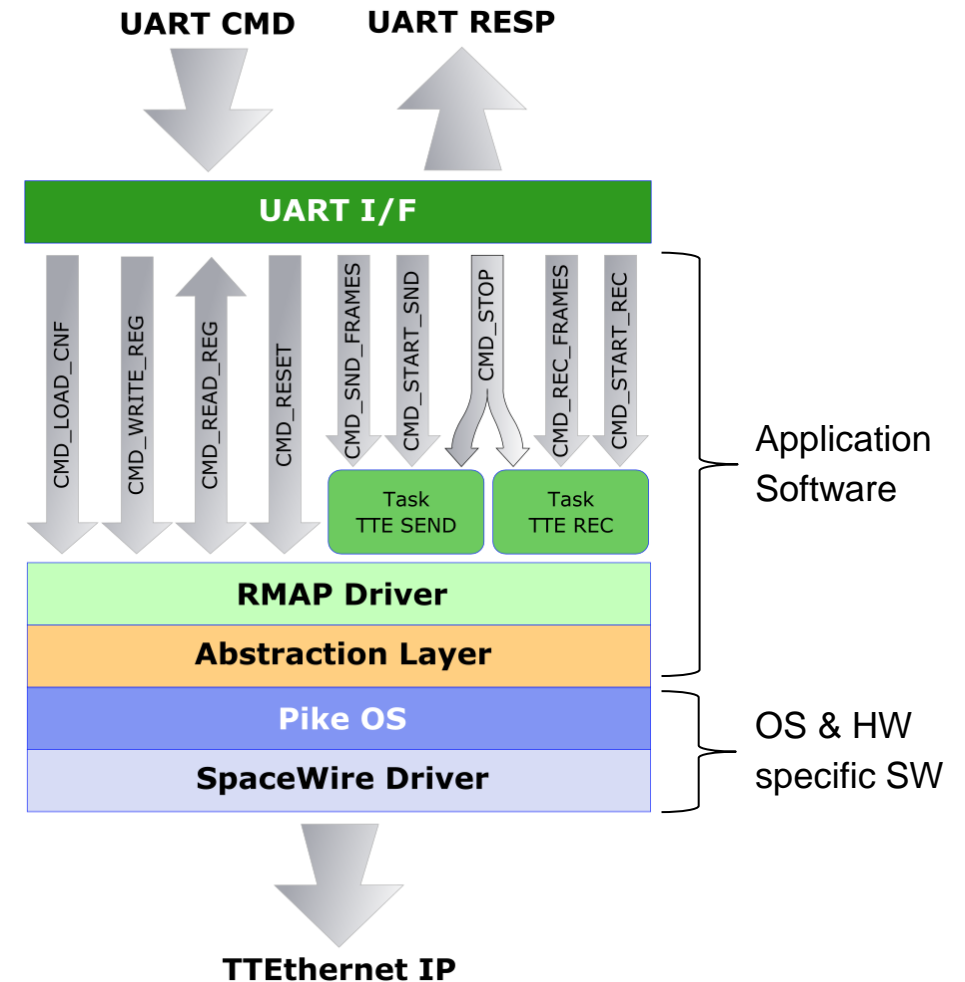
Thermal S.

Airbus Crate

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Airbus Crate SW (LEON 4)

PikeOS Operation System:

- PikeOS 4.2.3 "SPARC Integrator Suite Node-Locked Research License"
- PikeOS 4.2.3 Run-Time License
- Not released BSW/BSP (result from OBCSA)

GSTP Application Software:

- Includes the commands for control of Ref ES and to support test cases (e.g. "Task TTE Rec")
- Abstraction Layer has been introduced to reuse Application Software for different OS (i.e. VxWorks, RTEMS)

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Airbus Crate IP Core (Ref ES)

Ref ES IP Core consist of:

- GRLIB (UART, SPI etc…) from Cobham
- RMAP IP from ESA
- TTE IP Core from TTTech
- LEON 3 Processor (Cobham) + Traffic Initiator for Thermal Sensor (MAX6675 v1.2)
- Airbus VDHL Programming (e.g. MAC trigger)

GSTP uses PEGASUS instead of PHOENIX TTE IP (used in ORION)
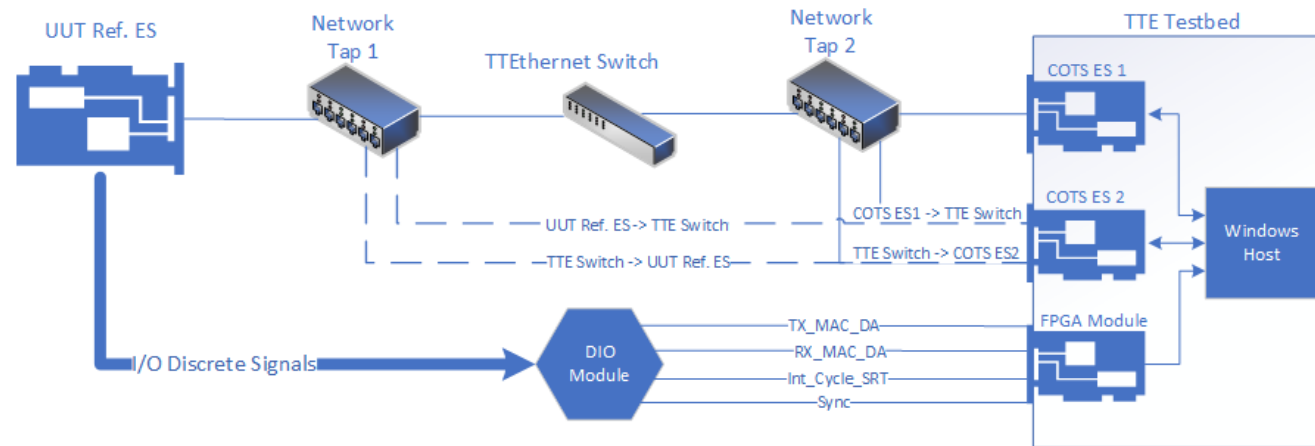
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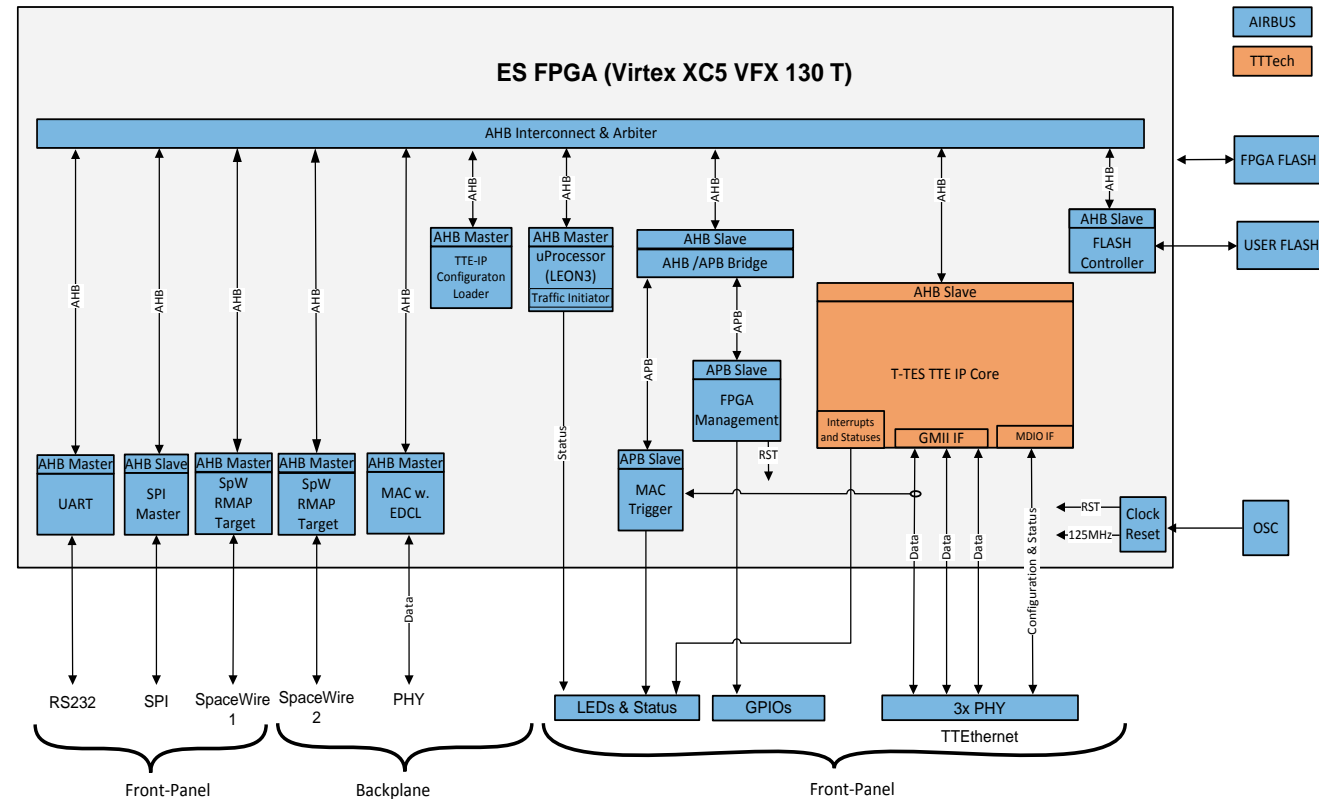
Chapter #2

Test Cases and Test Results within GSTP:

- Test Scope

- Test Architecture

- Synchronization Functionality Tests

- Precision Test

- Fault Injection During Synchronization

- Babbling Idiot

- Maximum Throughput

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Test Scope

- Test Scope:
  – Development of a Testbed for 3rd party TTEthernet End Systems
  – Implementation of 9 different test-cases to verify the correct integration of the TTTech End System Core IP in 3rd party Ref End System
  – Verification of the fundamental features of the TTEthernet Protocol

- Test-Cases: Goals
  – Stress the TTE End System IP
  – Validate that it behaves as intended on the Airbus developed Reference End System Hardware

Test Architecture

Component	Role In The Network
UUT Reference End System	Unit Under Test (TTEthernet End System card developed by Airbus D/S)
2x Network TAPs	Test Access Points to sniff the data exchanged between all of the components in all directions
TTEthernet Switch	Network switch which uses the TTEthernet protocol to communicate
2x COTS End System	TTTech's own TTEthernet End System which is used either to capture data from the network or to stress the UUT
DIO Module (Breakout Box)	Breakout box used to route the discrete signals from the UUT to the FPGA module in the TTE Testbed
FPGA Module	FPGA in the Testbed which is used to timestamp the signals originating from the UUT
Signal 1: TX_MAC_DA	Set to high (1us) whenever a frame with a specific (configurable) VL-ID is sent from the UUT
Signal 2: RX_MAC_DA	Set to high (1us) whenever a frame with a specific (configurable) VL-ID is received by the UUT
Signal 3: INT_CYCLE_SRT	Set to high (1us) whenever a new integration cycle begins
Signal 4: SYNC	Set to high when the UUT is in a synchronized state; Set to low otherwise

Synchronization Functionality Tests

Goals

- Synchronization is the pre-requisite for Time-Triggered communication between the network components

- Therefore, the goal of this test-cases is to verify that the UUT is able to correctly synchronize to the network during 3 phases:
  - At power-up (Initial Synchronization Test-case, i.e. Startup)
  - During runtime (Ongoing Synchronization Test-case)
  - After losing synchronization (Re-Synchronization Test-case)

Achievement

- With this test the TTE-Testbed is able to validate that the startup feature is executed correctly for all three cases:
  - Initial Synchronization Procedure
  - Ongoing Synchronization Procedure
  - Re-Synchronization Procedure

Measured Figures

Test-Case	Test Result	
Initial Synchronization Test-case	Startup Time*	653.82 us
	Startup Analysis	Validated by checking the exchanged frames during the protocol execution
Ongoing Synchronization Test-case	Ongoing Synchronization Analysis: Validated by checking the exchanged frames during the protocol execution	
Re-Synchronization Test-case	Re-Sync Time**	13.627 us
	Re-Sync Analysis	Validated by checking the exchanged frames during the protocol execution

* The time that passed until the configured End system reaches initial synchronization

** The time that passed until the configured End System re-synchronizes to the network

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Precision Test

Goals

- To verify that the Airbus End System correctly executes the Time-Triggered Ethernet schedule with respect to the clock synchronization algorithm

- To achieve this, the timing of two time-triggered messages (1 transmitted from the UUT and 1 received by the UUT) is measured and then compared with the scheduled values computed by the TTE-Tools

Achievement

- With this test the TTE-Testbed is able to validate that the newly developed End System card behaves and executes according to the configuration file that is generated by the TTE-Tools and sends (receives) the time-triggered frames at the correct (i.e. scheduled) moment in time

- If the difference between the measured value and the configured value is less than the 1 us precision, the test is considered passed

Measured Figures

Test-Case	Test Result	
Transmitting Side	Scheduled Sending Point in Time of the Message (relative to integration cycle start)	2,001120 ms
	Minimum Measured Sending Point in Time of the Message (relative to integration cycle start)*	2,001620 ms
	Maximum Measured Sending Point in Time of the Message (relative to integration cycle start)*	2,001787 ms
Receiving Side	Scheduled (configured) Receiving Window Start (relative to integration cycle start)	2,999574 ms
	Scheduled (configured) Receiving Window End (relative to integration cycle start)	3,04666 ms
	Minimum Measured Receiving Point in Time of the Message (relative to integration cycle start)	3,010233 ms
	Maximum Measured Receiving Point in Time of the Message (relative to integration cycle start)	3,010347 ms

* Empirical trigger values (1000 frames)

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Fault Injection During Synchronization

Goals

- To verify that the UUT behaves correctly when a synchronization master (SM) is missing from the network (A SM is a device which actively takes part during the synchronization process)

- To verify that the UUT behaves correctly if protocol control frames are periodically shifted in time (protocol control frames are the frames which are used to perform all synchronization processes)

- To verify that the UUT behaves correctly if protocol control frames are missing or have incorrect content

Achievement

- With this test the TTE-Testbed is able to validate that the Airbus End System either stays in sync, or drops out of sync depending on the configured settings and depending on the number of synchronization masters that are available in the network

Measured Figures

Test-Case		Test Result
Missing Synchronization Masters Test-case	Part 1: 2 SMs needed for synchronization	UUT looses sync after powering off one SM
	Part 2: 1 SM needed for synchronization	UUT does not lose sync after powering off one SM
PCFs Time Shift Test-case	UUT loses sync only if the time shift is higher than the configured network precision (10 us)	
Corrupt And Missing PCFs Test-case	UUT does not lose synchronization if PCFs are corrupt or sporadically missing	

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Babbling Idiot

Goal

- To validate that the UUT behaves correctly, i.e. according to the configuration, when it receives configured and unconfigured traffic or frames with incorrect checksum

Achievement

- With this test the TTE-Testbed is able to validate that the End System discards all the unconfigured traffic and the frames with incorrect checksum

Measured Figures

Test-Case	Test Result	
Unconfigured Critical Traffic (Rate Constrained + Time-Triggered)	Number of unconfigured critical-traffic frames transmitted to the UUT	4000
	Number of unconfigured critical-traffic frames discarded by the UUT	4000
Unconfigured Best-Effort Traffic	Number of unconfigured best-effort frames transmitted to the UUT	1000
	Number of unconfigured best-effort frames discarded by the UUT	1000
Frames with Incorrect Checksum (CRC)	Number of frames with incorrect checksum transmitted to the UUT	10
	Number of frames with incorrect checksum discarded by the UUT	10

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Maximum Throughput

Goal

- To measure throughput values which can be achieved by the UUT:
  - 5 Time-Triggered (TT) VLs in a 20 ms integration cycle
  - 5 Rate-Constrained (RC) VLs in a 20 ms integration cycle
  - 10 critical traffic VLs in a 20 ms integration cycle (5 TT + 5 RC)
  - Maximum throughput achieved by the UUT from the host interface in a Gigabit Setup
  - Maximum throughput achieved by the UUT when bypassing the host in a Gigabit Setup (TX & RX)

Achievement

- With this test the TTE-Testbed is able to validate that the End System is able to transmit traffic with highest possible throughput when it is not limited by software

Measured Figures

Test-Case	Measured Throughput
5 Time-Triggered VLs in a 20 ms integration cycle	3 Mbit/s
5 Rate-Constrained VLs in a 20 ms integration cycle	3 Mbit/s
10 Critical-Traffic VLs in a 20 ms integration cycle (5 TT + 5 RC)	6 Mbit/s
Maximum throughput achieved by the UUT from the host interface in a Gigabit setup	7 Mbit/s
Maximum throughput achieved by the UUT when bypassing the host in a Gigabit setup (TX) *	992 Mbit/s
Maximum throughput achieved by the UUT when bypassing the host in a Gigabit setup (RX) *	992 Mbit/s

* Burst of 10 frames

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Chapter #3

Summary and Way Forward

- Summary

- Increase Maturity of Existing SPINAS Prototype

- Develop a "Light IP" that fits To the future FPGA architectures

- Adapt existing LEON4 software design for cFS technology

- Development of a Network Analyzer + Marketing of TSB within space industry
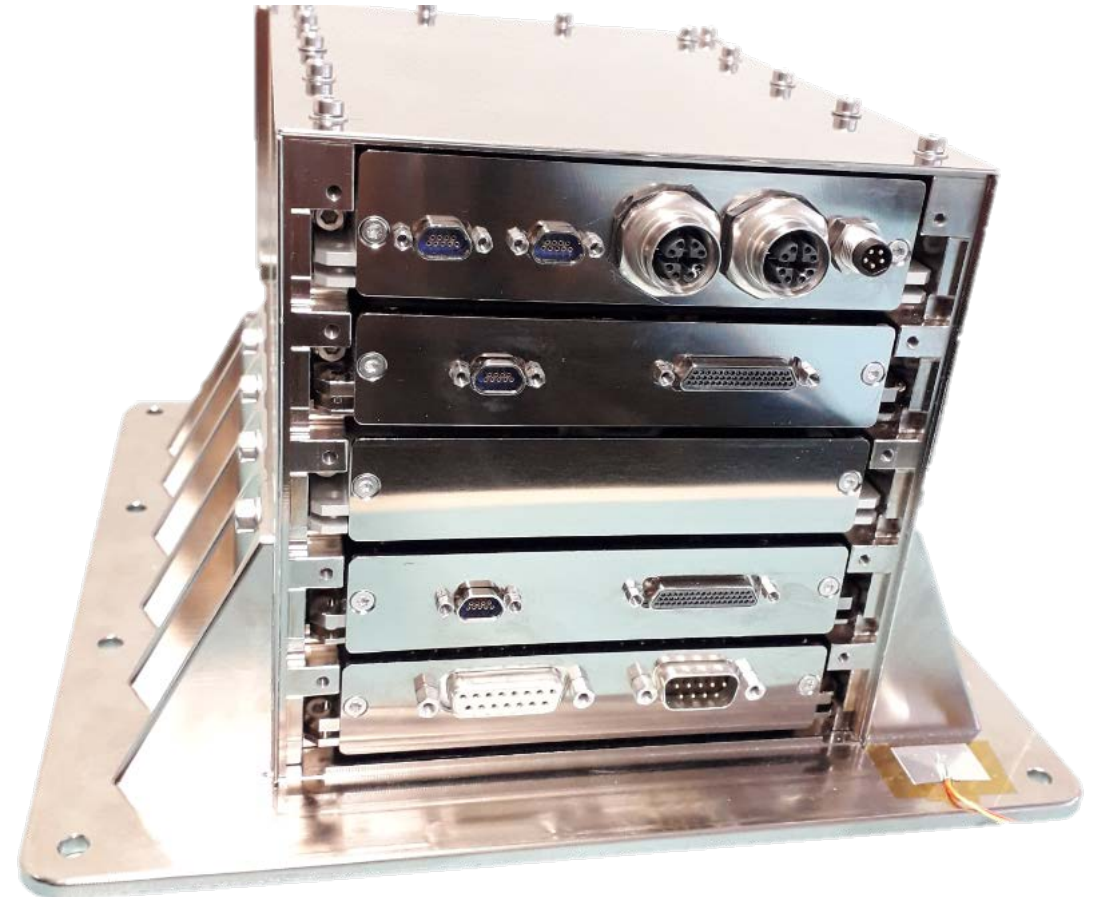
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Summary

- The selected Architecture has caused
  - additional Effort in terms of technical complexity
  - Management of OBCSA activities and GSTP activities

- The developed hardware architecture may be used for next generation of standard computer (SPINAS) in space

- Airbus demonstrated TTE functionality in SPINAS and started to extend functionality in terms of CFS (NASA DSG concept)

- Uncomplicated integration of Airbus and TTTech contribution (see Acceptance Test)

- No major surprises about the "Stress Tests". Reference End System behave as expected and build a "Reference" for future architectures

- Modular TSB architecture concept allows functional extension of actual architecture

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Increase Maturity of Existing SPINAS Prototype

Qualification of the future used operation system. It needs not to be PikeOS automatically

Industrialization of the Ref ES and LEON 4 manufacturing. Which company is able to manufacture space qualified boards (e.g. soldering qualification)?

Minor: Program PikeOS LAN driver that allows Front End _and_ Backplane LAN communication in parallel

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Develop a "Light IP" That Fits to the Future FPGA Architectures

- Adapt IP that is programmed for the Virtex5 FPGA family (AXI interface)!

- Airbus believes that FPGA TTE solution should exist in parallel to the TTTech ASIC approach
  - FPGA solution becomes interesting if beside TTE other FPGA functionality is needed
  - ASIC solution could be interesting if single board approach is preferred (S - NIC card , MPCV)

- In future the CPU solution could be the way forward (see right figure)

- Other open market time triggered bus solutions should be investigated

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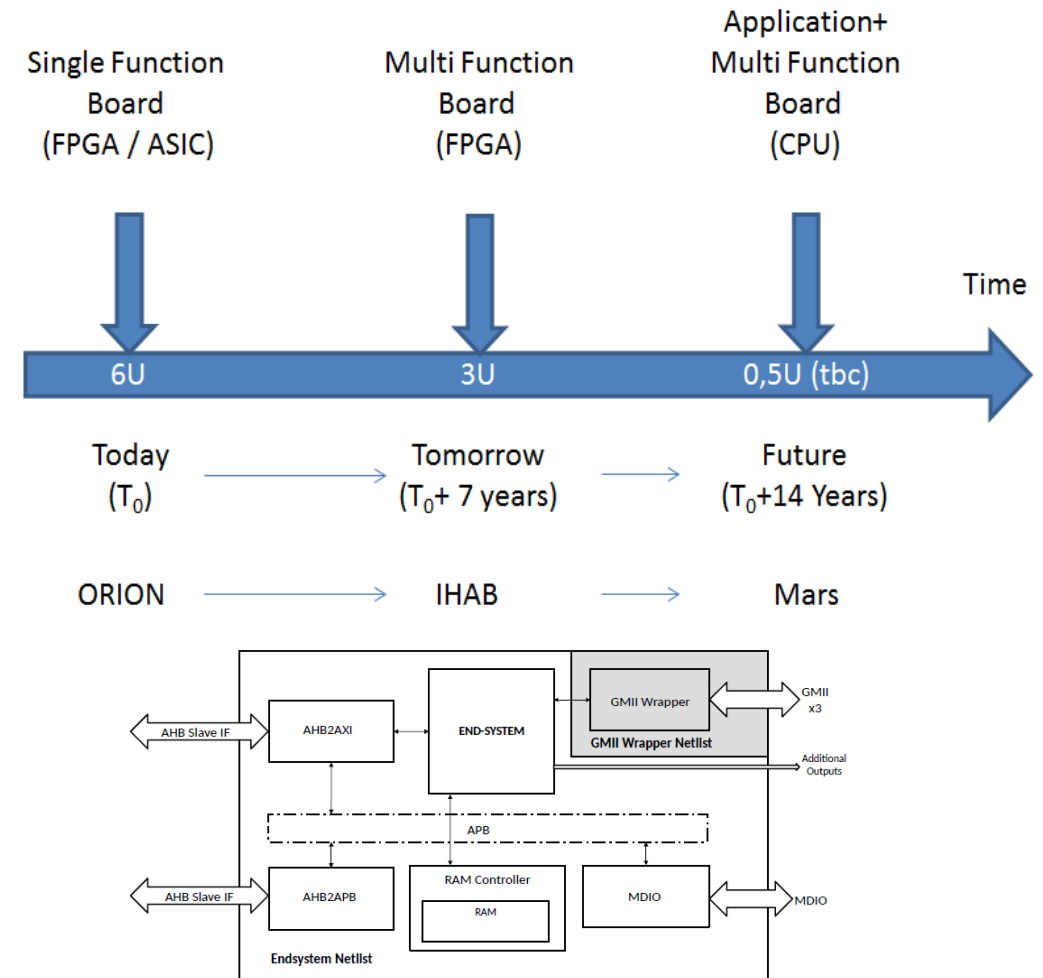
Adapt existing LEON4 software design for cFS technology

From NASA Web Page:
"The core Flight System (cFS) is a platform and project independent reusable software framework and set of reusable software applications."

"The cFS architecture has been proven to:
Reduce time to deploy high quality flight software
Reduce project schedule and cost uncertainty
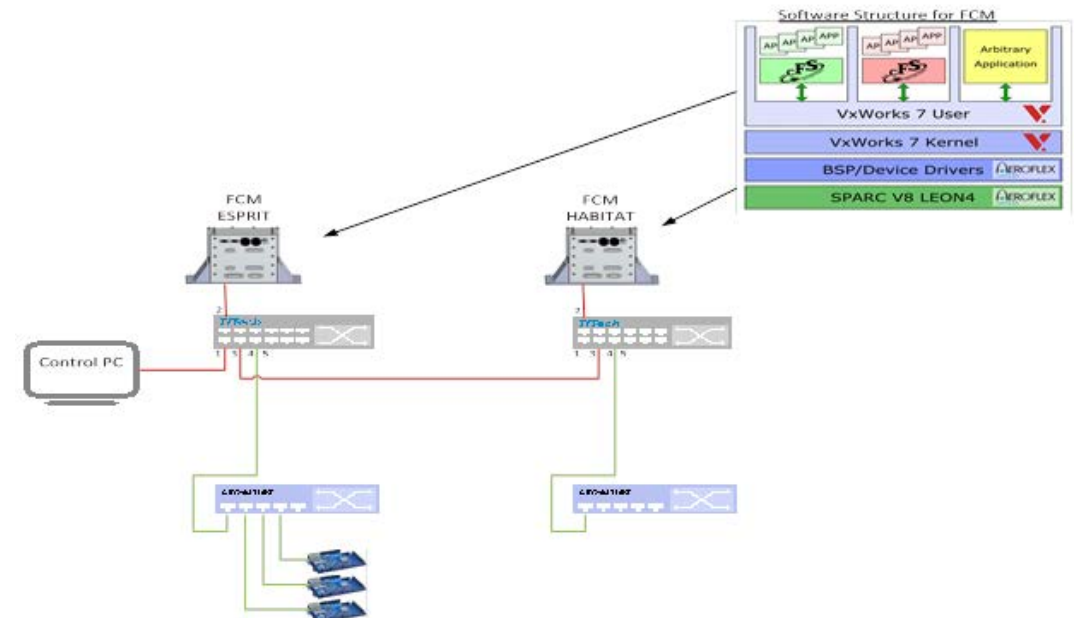*Facilitate formalized software reuse*
Enable collaboration across organizations
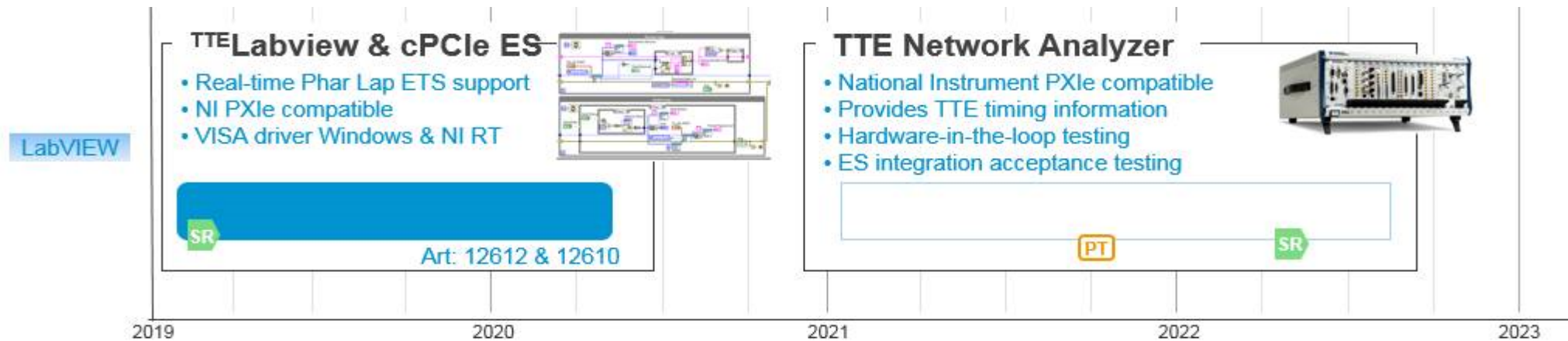*Simplify flight software sustaining engineering*
Provide a platform for advanced concepts and prototyping
Provide common standards and tools across Goddard's missions and NASA wide"

Maturate cFS technology. Realize TTE bus technology with cFS

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Development of a Network Analyzer + Marketing of TSB within space industry

TTTech is envisioning potential exploitation as network analyzing tool. This requires further market research and product definition

Testbed could evolve into a full-blown TTE compliance tester once the related ECSS standard is published. This is not in the focus of TTTech though but the company would be happy to support any third party wanting to develop such a tester in the framework of an ESA contract

Thank you

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