~ Sli.do Q&A ~
Generation of a testbed for the validation of the TTEthernet technology

Why did you choose PikeOS?

The original motivation was to demonstrate partitioning OS with state-of-the-art processor boards. Thereby Airbus draw upon experiences made during the A400M project. The colleague has worked a couple of years on the SW for the Load Master Station. The controller uses PikeOS as well.

A final trade-off which OS should be used on Leon 4 has not been done. Beside PikeOS Airbus could collect experiences with RTEMS and VxWorks as well.

Is the operating system abstraction layer you mentioned custom or which one did you integrate?

The abstraction layer has been developed by Airbus explicitly for the LEON4 design. For each OS as well for each HW another abstraction layer would be needed.

We introduce the abstraction layer the first time. The motivation was not to rewrite the application software for the Deep Space Gateway demonstration again (VxWorks)

How many resources (roughly) of the Virtex-5 does the TTEthernet IP core require?

In our DDF following figures were given:

Resources	Resources XQ5FX130	Current Design
LUT	81920	48979
%	100%	60%
Register	81920	31896
%	100%	39%
IO	840	270
%	100%	33%
BRAM (kbit)	10728	1114
%	100%	11%

Which LEON4 device was used? GR740?

For the realization of the GSTP project a specific new HW design has been made.

To work in parallel some of the software designers have worked on GR740 for coding relevant software.

To purchase such a test bed, would one contact Airbus or TTTech?

Both ways are possible if the design is not changed.

If you wish modifications on Airbus Crate and its UUT then I would contract Airbus.

If you want modifications on the testbed functionality I would contract TTTech.

Would the current version of the TTTech IP core fit into an RTG4 FPGA?

In the moment Airbus does not see any reason not to integrate the TTE IP into the RTG4. However Airbus has no experiences.

TTTech commits that a TTE IP integration on RTG4 is feasible.

Was mapping of TTE IP onto BRAVE FPGA considered/done by ADS?

GSTP did not consider this as option.

When the project has been started (2016!) a discussion between RTG4 and Virtex5 took place. Thereby Airbus decided to proceed with Virtex5 because of the better maturity level (better tools).

If the project is started again the decision would not be so clear!