Hardened DDR2/3 PHY development

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The DDR PHY provides connectivity between a DDR Memory Controller and the DDR2 or DDR3 memory devices. This DDR PHY is compliant with both JESD79-2E and JESD79-3F specifications providing the Industry Standard DFI interface to the Memory Controller (MC).

The PHY design has been targeted in C65SPACE hardened CMOS process of ST Microelectronics. It is compatible with wirebond interconnection scheme as well as the flip chip one.

The implemented PHY has the following features:

- Supports both DDR 2 & DDR 3 memory devices.
- Compatible with T-branch & Fly-by topologies.
- Supports minimum data rate of 666 Mbps per data line.
- Support for 1 or 2 memory channels.
- Each memory channel is independent with configurable width up to 64 bits, in increments of 8 bits.
- Up to 8 ranks (chip selects) per memory channel.
- Supports DLL off operation.
- Supports dynamic On-Die Termination.
- Supports x4, x8, x16 device configuration.
- Supports DFI 2.1.1 [RD13] interface between Memory Controller (MC) and the PHY.
- Supports 1:1 frequency ratio interface between MC and DFI.
- Supports Gate, Read and Write Leveling schemes.
- Supports automated or manual ZQ Calibration.
- Supports a loopback mode for high speed test.
- Full control of the accompanied IO Buffers.

The full development flow for both front-end and back-end parts have been executed. The size of the obtained GDS for the final IP is 2811um by 650um (without the pads).

DDR IO buffers/pads have been implemented as hardened in both wirebond and flip-chip flavour in order to be used as required.