

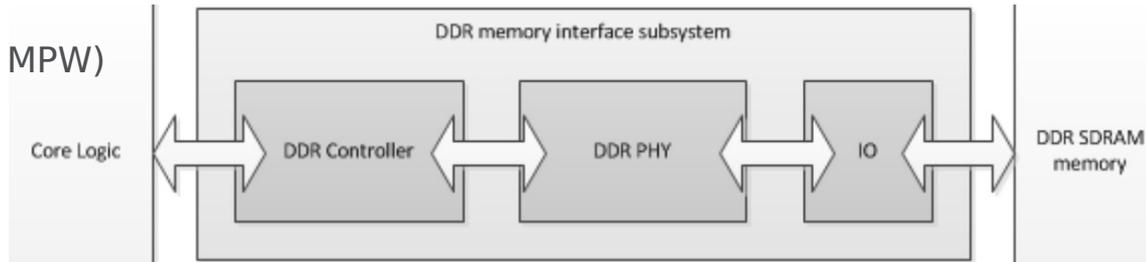
DDR Interface for Space DSM

TEC-ED & TEC-SW Final Presentation Days

2020-05-13

DDR Interface for Space DSM

- *Budget:* 900000 (600 ECI-4 + 300 TRP), reduced to 745000
- *Prime/Sub:* Cobham Gaisler AB, Sweden (SE) / Integrated Systems Development S.A., Greece (GR)
- *Duration:* 4.5 years (planned 2 years)
- Test chip discarded (non-availability of MPW)
- IPs are available



- *Main Objectives:*

- 1) Develop, prototype and test a DDR2/3 solution for ST-Microelectronics C65Space;
- 2) 3 components: DDR-Controller (FTADDR), Physical Layer (PHY), SSTL IO buffers (IO);
- 3) VHDL synthesisable cores available on ESA IP portfolio (for ESA activities) or contractors;
https://www.esa.int/Enabling_Support/Space_Engineering_Technology/Microelectronics/Fault_Tolerant_DDR_Controller_FTADDR
- 4) C65Space technology specific parts available from ISD or ST only.

Rad-hard DDR2/3 Physical Interface (PHY) and I/Os in C65SPACE

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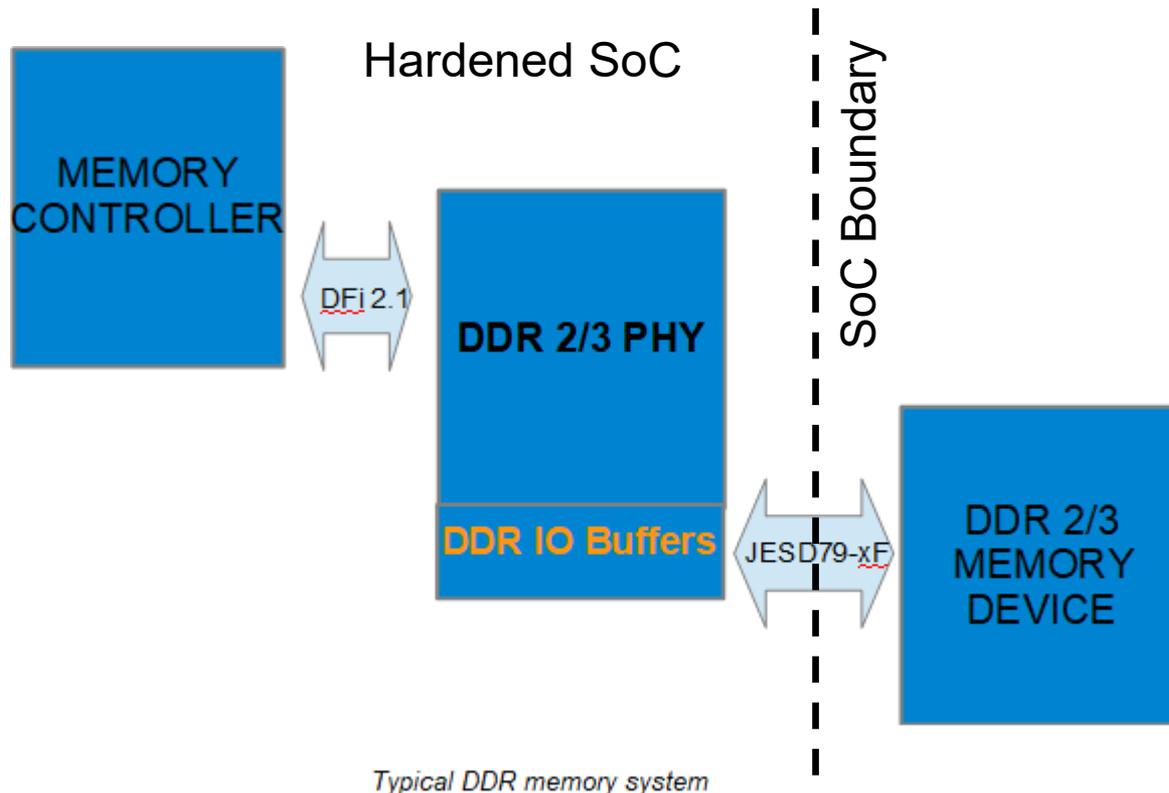
Context

- This development has been performed under ESA contract and the main outcome is the PHY IP and the associated I/O buffers, in classical wire-bond configuration, targeted in the hardened 65nm CMOS platform of ST Microelectronics.
 - In parallel, under the same contract a memory controller has been developed by Gobham Gaisler.

- In a second step, under CNES contract, the IPs have been re-engineered in order to become flip-chip compatible in the hardened 65nm CMOS platform of ST Microelectronics.

At a glance

- The PHY IP provides connectivity between a DDR2/3 Memory Controller and DDR2/3 memory devices.
 - Interfacing any Memory Controller DFI 2.1 and 2.2 compatible
 - Interfacing DDR2/3 memory devices according to JESD79-2E and JESD79-3F standards



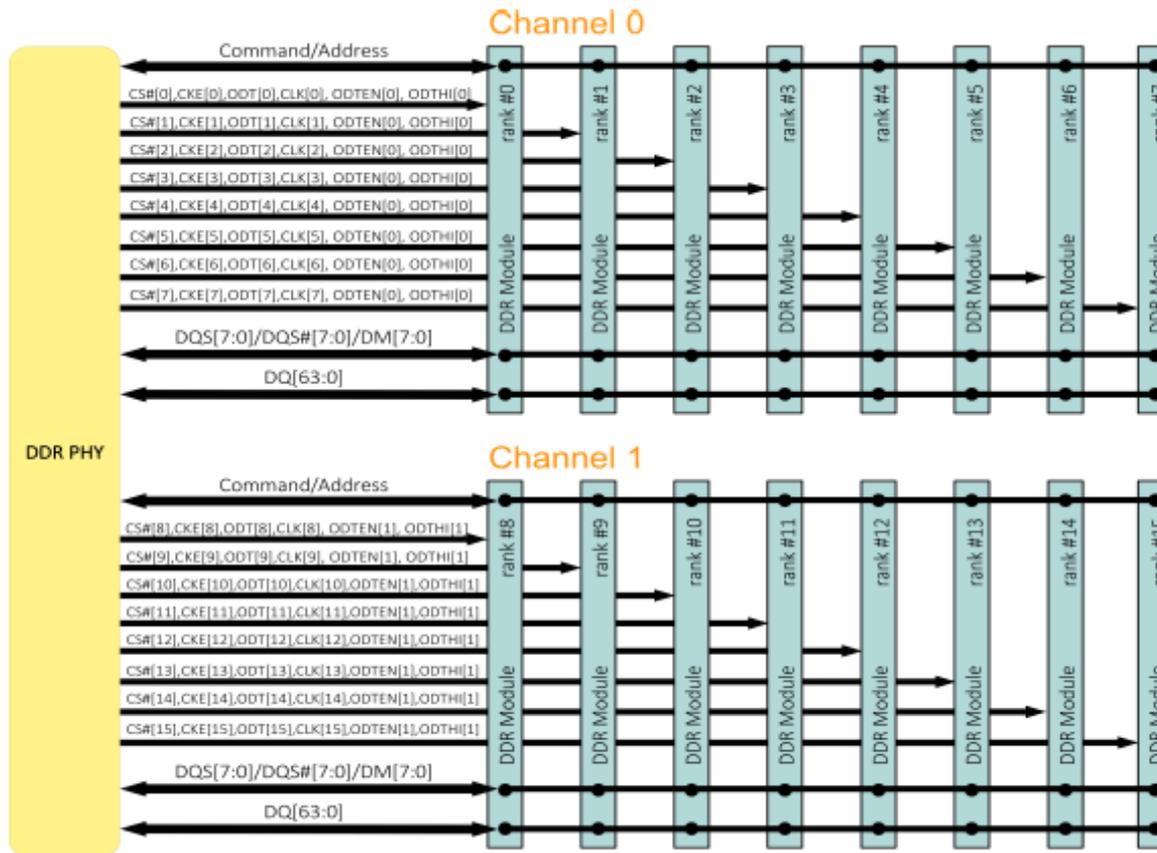
Typical DDR memory system

Key Features

- Supports both DDR 2 & DDR 3 memory devices
- Configurations:
 - 2 channels
 - Up to 8 byte lanes per channel – 8 chip select
 - Supports the two channels concurrently or individually
 - Each channel is independent with configurable width up to 64b, in increments of 8b.
- Supported data rates DDR2:
 - @200Mhz 26.5gbps/channel (with 8 byte lanes)
 - @400Mhz 53gbps/channel (with 8 byte lanes)
- Supported data rates DDR3:
 - @333Mhz 46gbps/channel (with 8 byte lanes)
 - @400Mhz 53gbps/channel (with 8 byte lanes)
- Supports DLL-off operation and dynamic On-Die Termination
- Supports loopback mode for high speed test.
- Compatible with T-branch & Fly-by topologies for clock distribution
- Supports DFI 2.1/2.2 interface between memory controller and the PHY.
- Supports 1:1 frequency ratio interface between memory controller and PHY.
- Supports Gate, Read and Write Leveling schemes.

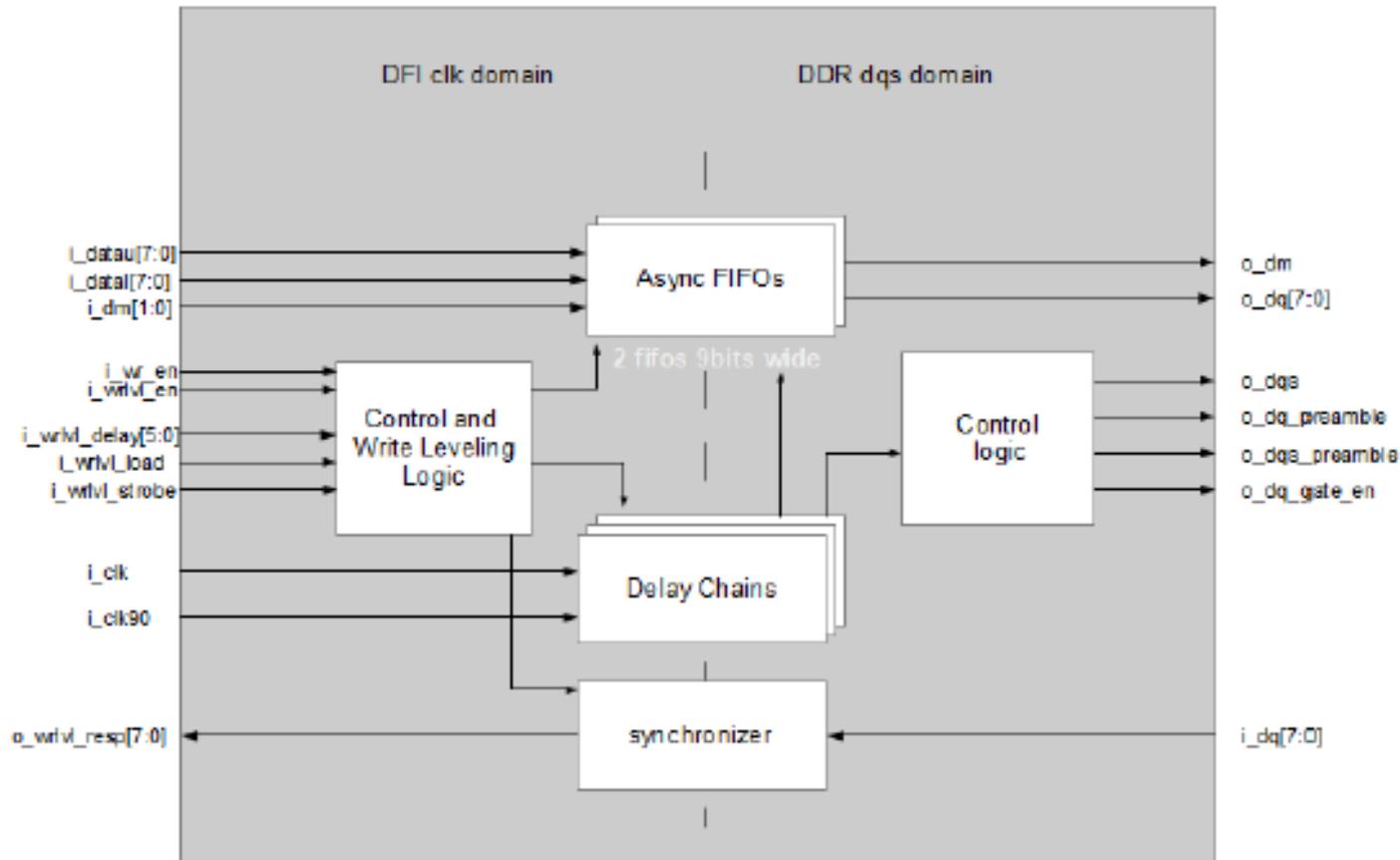
Memory Topology

- PHY is capable to support multiple memory channels, as shown below.



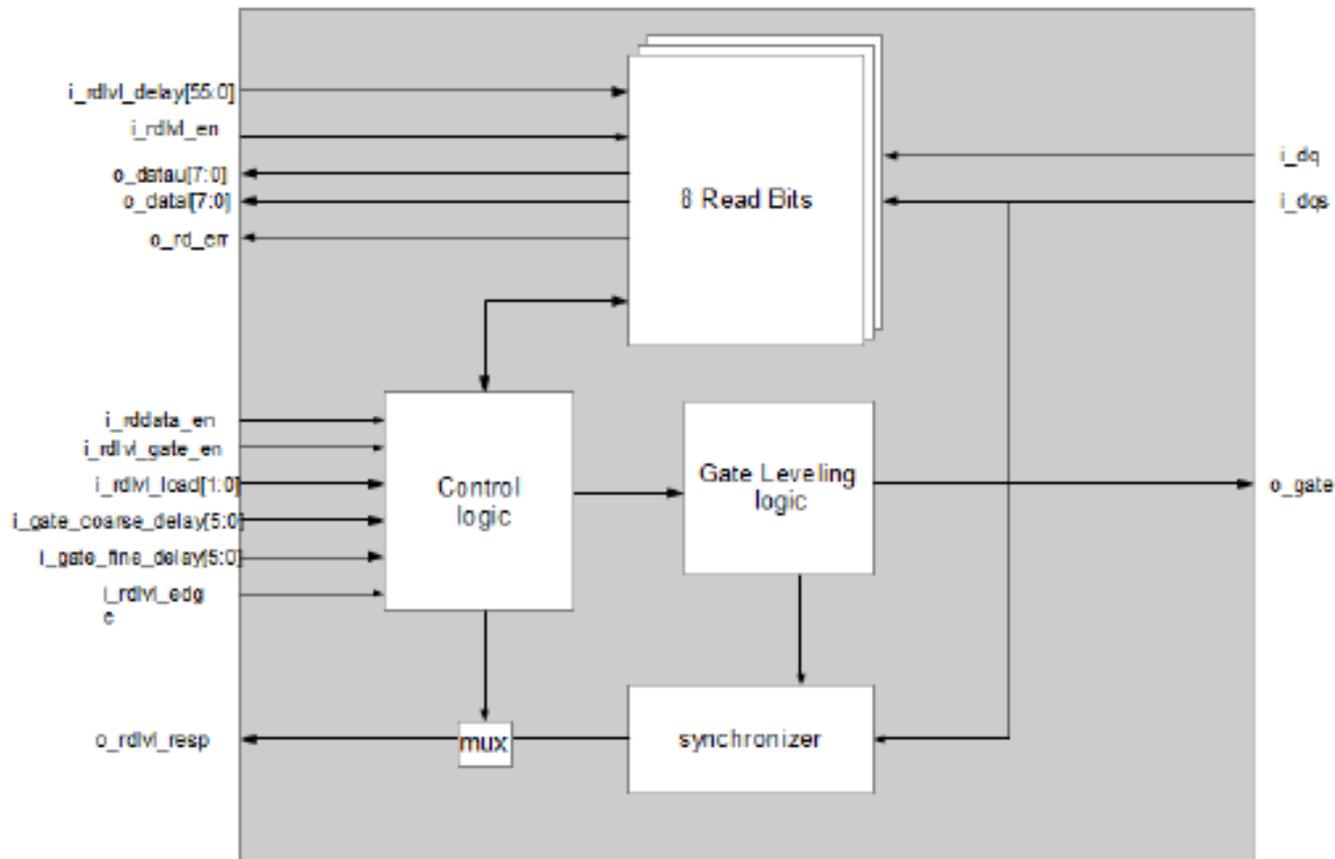
Write Data Path

- This block handles all write transactions from the PHY to the memory device(s) as well as the write leveling procedure.



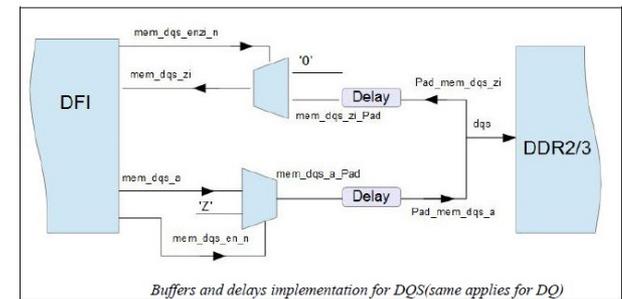
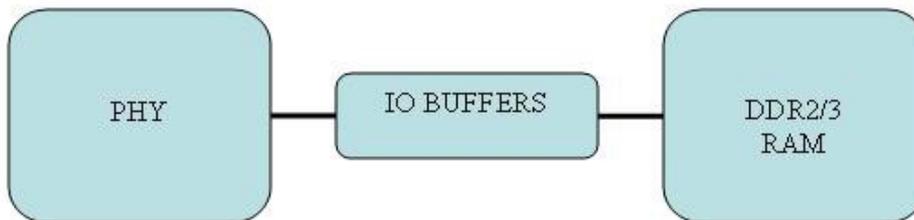
Read Data Path

- This block is responsible for reading data from the memory, using data strobe as clock input and feeding them to the memory controller through the DFI interface. It also contains all the logic needed for read leveling.



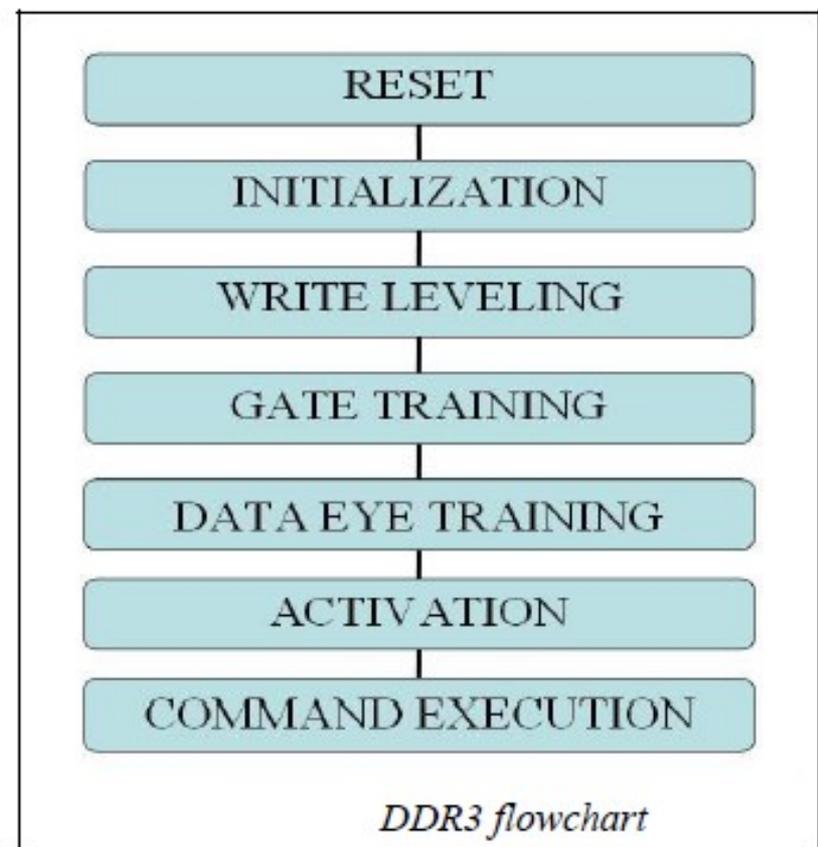
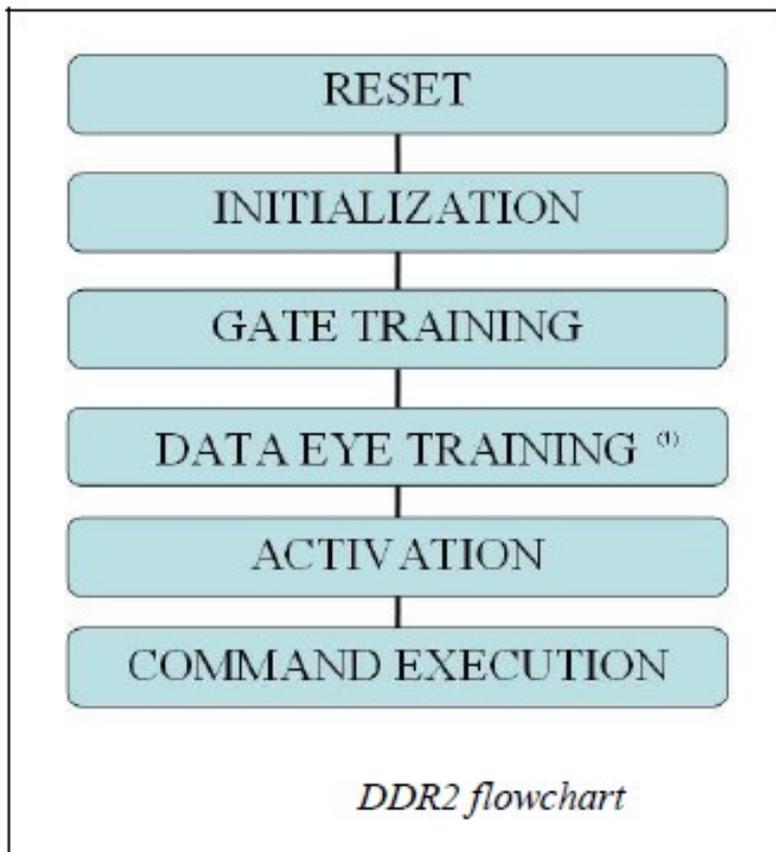
Verification Process (1/2)

- In order to better simulate the behavior of PHY, the following architecture was used for the verification process.
- A DDR2/3 prototype from Micron SA corporation was selected as the needed model for DDR2/3 RAM.
- In the test benches, an average delay of 1.4ns was introduced in the signal in order to emulate a realistic application involving DDR2/3 memories (mainly due to the PCB).



Verification Process (2/2)

- In the following flowcharts, the operations that take place in the test benches are illustrated:



RTL to Gate Flow

- Synthesis
 - hardening by using Skyrob and worst case library (worst case process, 1.1V, 125C ambient temperature, degraded after 20y of operation)
 - set of constraints was used for achieving the desired behavior
 - hierarchical approach (ddc for submodule, used as dont_touch in upper level)
- Formal Equivalence Check
 - process succeeded
- Static Timing Analysis
 - Functional scenario only
 - process considered as acceptable (remaining violated paths analyzed and could be corrected during PnR)
- Gate-level Verification
 - simulations run with netlist+sdf files (best/worst case)
 - PHY: all tests are passed
 - DDR2 200/333/400 MHz
 - DDR3 333/400MHz

Gate to Layout Flow (1/2)

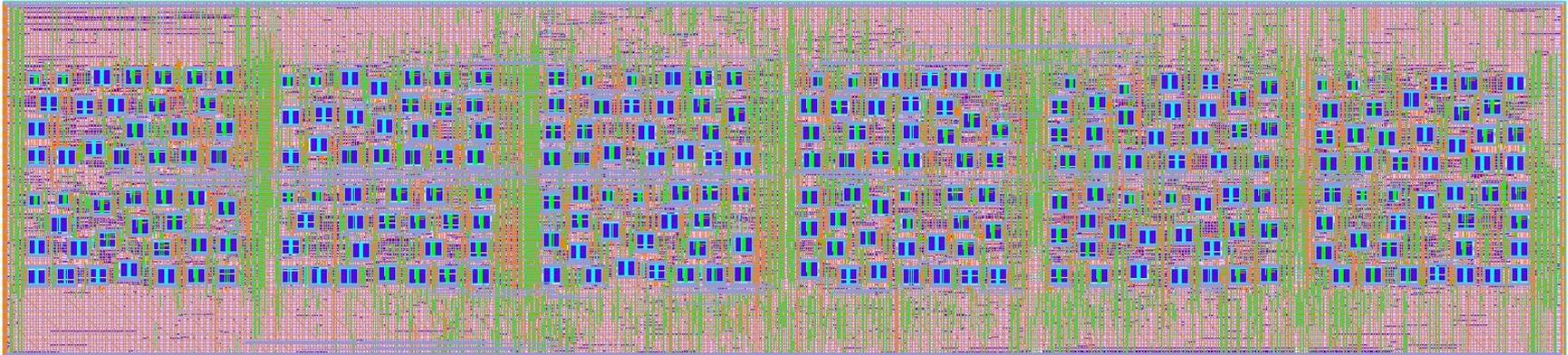
- Overall approach
 - Hierarchical process (analog design-like to ensure regularity in the final layout)
- Place and Route:
 - Floorplan
 - IO and cell placement
 - Special net routing
 - Clock tree synthesis
 - In-place optimizations
 - Global and detailed routing
- Hardening
 - Hardened design rules
 - Deep n-well mask
- Formal Equivalence Check
 - Ensure the equivalence of final design versus RTL
 - Process succeeded

Gate to Layout Flow (2/2)

- Static Timing Analysis
 - Process run for best and worst case conditions
 - PHY: results ok, timing violation acceptable
- Post-layout Verification
 - SDF files from Primetime used (best/worst case)
 - PHY: all the tests are passed
 - DDR2 200/333/400 MHz
 - DDR3 333/400MHz
- Sign-off tests
 - Calibre DRC (design rule check) with certain justified rules waived
 - Calibre DRC antenna checks
 - Calibre LVS (layout versus schematic)
 - All the issues are solved
 - Final GDS files are delivered

12byte Lane PHY Layout View

- 2811um x 650um (w/o I/Os)



Hardened I/O Library Features

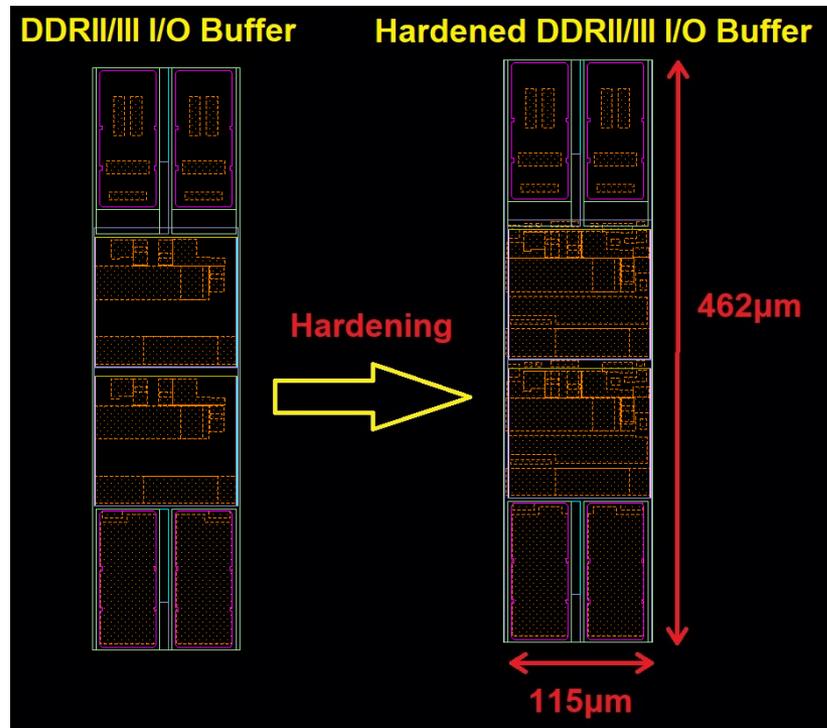
- SSTL I/Os
- 1.5V and 1.8V signaling
- Work either with 1.8V supply as interface with DDR2 applications or at 1.5V with DDR3 applications
- Cold spare (no power sequence requirement for core and I/O supplies)
- Pseudo-differential input for data and fully differential for strobe
- Scannable tri-state output
- Active impedance and slew controlled output drivers (via the compensation cell)
- Antenna diode protection on core side input
- I/O cells in tri-state when I/O power is up and core power is down.
- ODT (On Die Termination) functionality, in order to integrate the parallel resistor inside the die and improve signal integrity (depending if it is input or output).

Hardened I/O Library Cells

- Starting from a non-hardened version of the library validated on consumer electronics products
- The cells are:
 - I/O strobe
 - Bi-directional data
 - Output only data (i.e. for the address)
 - Core power supply
 - Reference Voltage (stable reference voltage for differential pair)
 - Compensation cell (compensate process and temperature drifts)
- Double row cells

Buffer Hardening

- Added deep n-well mask under all active devices.
- Applied all space rules to all cells (continuous guard around DNW, continuous n-well strap on the edges of DNW and more).



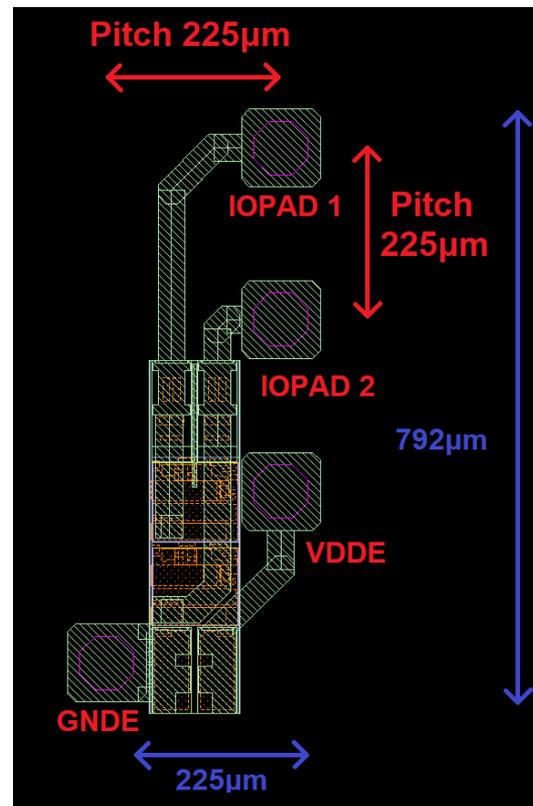
WireBond Hardened I/O

- Pad openings $108\mu\text{m} \times 44\mu\text{m}$ (including probing area).
- Each I/O Buffer has 2 pads for connection of I/O ring power supplies (VDDE, GNDE)



Flip-Chip Hardened I/O

- Bump openings $70\mu\text{m} \times 70\mu\text{m}$.
- The bumps are placed only in array of $225\mu\text{m}$.
- Each I/O Buffer has 2 pads for connection of I/O ring power supplies (VDDE, GNDE)



Current Status

- The IP and the I/O buffer are ready to be used both in classical wire bond and flip-chip flavors

The next step

- Identify the right opportunity for validating the PHY and the I/O buffers on a 65nm MPW
- Validate the IP in a product to be targeted in the 65nm node
- Modify the PHY IP (under CNES contract):
 - In order to support certain features requested by ISD/ST customers
 - Support also DDR4 devices.
 - Port the IP to the 28nm CMOS platform
 - Validate the IP in a 28nm MPW
- Integrate the IP in products (e.g. HPDP v2.0, etc) targeted on the 28nm node

Thank you!