~ Sli.do Q&A ~
Hardened DDR2/3 PHY development

What about availability and licensing terms of this IP core? Will it be available e.g. at least for ESA funded activities?

Certainly the licensing is possible. Any customer interested to use the IP core (in the framework of ESA funded projects as well as other projects), is advised to get in touch with ISD SA. In turn ISD will arrange all the formalities with ST Microelectronics as required.

Comment from ESA: The DDR controller IP developed in the frame of this activity (FTADDR) is already available in the ESA IP portfolio:

https://www.esa.int/Enabling_Support/Space_Engineering_Technology/Microelectronics/Fault_Tolerant_DDR_Controller_FTADDR

The RTL synthesisable version of the PHY could be made available by ESA on request for ESA activities. However, ESA can not provide the hard-macro or any ST-Microelectronics technology views and can not guarantee that the RTL would lead to satisfying results. For the hard-macro, users should indeed contact ISD. The SSTL buffers can also be made available by ST-Microelectronics on request.

Have you validated the design with a test vehicle? Or only by simulations and timing analyses so far?

So far the IP and the I/Os have not be validated in an MPW – it is our target to do so in the near future. In any case, the test bench used and the whole validation flow is such that give us very high certainty about the maturity of the IP.

Have you tested or verified the PHY with other existing DDR2/3 memory controllers?

Yes – it has been tested successfully with two different controllers. Unfortunately, we cannot provide further information on this topic.

Will the new hardened new IOs (WB and FC) be available for future ASIC development using STMicroelectronics C65SPACE library? How?

Certainly the licensing is possible. Any customer interested to use the I/Os (in the framework of ESA funded projects as well as other projects), is advised to get in touch with ISD SA.

Can the DDR4 be supported in 65nm, or you need to migrate to 28nm?

As of today, the 65nm implementation does not support DDR4 devices. It is possible to extend the PHY capabilities in order to interface DDR4 devices as well, however the fastest clock will not be over 400MHz. So far none of our customers requested to extend the 65nm implementation in order to address also DDR4 devices.

Does the PHY have any specific support to avoid SEFIs in external DRAM devices? Can you provide recommendations on how to handle this?

This is mainly handled by the controller. The PHY is able to execute almost any potential algorithm instrumented by the controller in order to address SEFIs in external memories.