# ***ESA IP core extensions for LEON2FT: a new FPU with configurable (half/full/double) precision, and SWAR (SIMD Within A Register) instruction extensions***

The presentation will describe a new floating-point unit and new integer ALU for LEON2FT, together with new arithmetic instructions that have been implemented in LEON2FT. The new integer ALU, named SWAR unit, implements SIMD-within-a-register (SWAR) operations that are beneficial for speeding-up GNSS/SDR as well as cryptographic and image processing workloads. The FPU, named daiFPU, can be configured to a number of flavours, for example one fully compatible with the Meiko FPU, and others that support just selected operations in one of double, single or half precisions, their combinations (e.g. single+half) and packed formats (e.g. half+half). The daiFPU comes with the required support in llvm and SoftFloat. These arithmetic extensions increase the potential of LEON2FT for current and future on-board data processing. Besides architectural features the talk will present performance figures for a GNSS tracking loop accelerated with the SWAR operations, and for a number of floating-point benchmarks computed using various configurations of the daiFPU.