RTEMS EDISOFT for ARM Cortex R5 with Asymmetrical Multiprocessing

The RTEMS R5 project provides an RTEMS port for the Zynq 102 board (Ultrascale+). This port has an ARM Cortex-R5 processor capable of running in a redundant lock-step mode in which two cores are running the same code or in a dual-core core, in which each core runs on its own. Using the new build system developed under the RTEMS GCC project, this project updated both RTEMS source code and the RTEMS Improvement test suite with this new architecture. A final report was produced containing the description of the changes made, as well as how to use the new RTEMS on the target platform.

It is possible to run RTEMS Improvement using the 2-core mode, in which the application contains a single executable with a RTEMS Configuration for each of the cores. That is, the application defines the maximum number of threads, semaphores, etc., for each of the cores. While the current version works in Asymmetrical Multiprocessing (AMP), it requires only a single executable, making it a starting point to allow (limited) communication between the cores to take maximum advantage of the multi-core capabilities of this (and more powerful) CPU. Furthermore, an enhanced death report functionality was added to increase the debugging capabilities where a full dump of the RTEMS structures and CPU context is made to a user defined buffer.