

# GR740 – Next Generation MicroProcessor Flight Models

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TEC-ED & TEC-SW Final Presentation Day

01 June 2021



# GR740 – NGMP Phase 3: Flight Models

- Budget: 1900 k€ = 950k co-funding, 740k GSTP, 210k EOP
- Duration: 3.5 years (planned 2.5 years)
- Prime: Cobham Gaisler (SE)
- Supplier: ST Microelectronics (FR)
- Main Objectives:
  1. Flight Silicon Manufacturing (design from Phase 2)
  2. Flight Silicon Validation (functional, radiation)
  3. Space Qualification (QML-V with delta-ESCC evaluation)

# NGMP Programme: schedule & budget

|    | Activity Name   | Contract #           | Progr.   | Start   | End     | kEUR | Description   |
|----|---|----------------------|----------|---------|---------|------|---|
| HW | GINA  | 18533/04/NL/JD, COO3 | TRP      | 7/2005  | 5/2006  | 170  | Pre-Study (quad-core LEON3, FPGA breadboard)  |
|    | NGMP Phase 1  | 22279/09/NL/JK       | TRP      | 7/2009  | 12/2010 | 800  | VHDL design until PDR, FPGA prototyping   |
|    | NGFP  | 18533/04/NL/JD, COO5 | TRP      | 5/2011  | 5/2013  | 190  | Functional prototypes in eASIC Nextreme2 (45 nm)  |
|    | NGMP Phase 1 completion   | 22279/09/NL/JK, CCN2 | TRP      | 8/2014  | 8/2015  | 315  | Detailed design and layout in ST65  |
|    | NGMP Phase 2  | 113922/15/NL/LF      | TRP      | 4/2015  | 12/2016 | 1100 | Prototypes in ST65, validation, rad-test  |
|    | NGMP Phase 3  | 4000122419/17/NL/LF  | GSTP/EOP | 11/2017 | 6/2021  | 1900 | FM qualification (50% co-funded = 950 k€)   |
| SW | RTEMS-SMP   | 4000108560/13/NL/JK  | TRP      | 2013    | 3/2015  | 300  | RTEMS for NGMP, parallel contract with Gaisler  |
|    | RTEMS-SMP   | 4000108771/13/NL/JK  | TRP      | 2013    | 4/2015  | 300  | RTEMS for NGMP, parallel contract with Spacebel   |
|    | RTEMS Qualification   |                      | GSTP     | 2019    | ?/2021  | 700  | In progress<br>(Edisoft, Embedded-Brains, Lero, Jena Optronics)   |
|    | Benchmark for multicore processor   | 4000102623           | INFRA    | 2010 ?  | 12/2012 | 90   | Barcelona Supercomputing Centre (BSC)   |
|    | System Impact of Distributed Multicore Systems  | 4200023100           | TRP      | 2010 ?  | 12/2012 | 290  | SIDMS = Hypervisor development, Astrium F, FentISS  |
|    | AIR hypervisor emulator<br>(source code and binary level)   | AO/1-7722/13/NL/LvH  | TRP      | 06/2014 | 12/2015 | 300  | Binary mode integrates ESOC emu 2.0 as LEON instruction set emulator. Consortium GMV (prime), Rapita, BSC |
|    | "Architectural solution for the timing predictability of the next generation multi-core processors" | 102880               | NPI      | 2011    | 2015    | 90   | Barcelona Supercomputing Centre, NPI Javier Jalle   |
|    | Cache structure optimisation for better RT performance  | 109680/13/NL/HK      | TAS/TRP  | 2013    | 2014    | 10   | Barcelona Supercomputing Centre   |
|    | Total   |                      |          |         |         | 6555 |   |

2009 – 2021 = 12 years, a long time, but...

- 2011 – 2014 : 3.5 years waiting for readiness and access to technology
- 2016 – 2017 : 1 year waiting for funding for qualification and packaging supplier “resigned”
- 2018 – 2019 : 1 year extra to establish and consolidate new assembly flow



# GR740 – NGMP Acknowledgement

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  - ST Microelectronics
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  - Contracts and administration
  - Management and fund-raising
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