SpaceFibre Interface Chip (TRP)

TEC-ED & TEC-SW Final Presentation Day

01 June 2021

SpaceFibre Interface Chip

- Budget: 600 K€
- Duration: 51 months
- Prime: STAR-Dundee (+ Airbus DS, RUAG, ISD)
- Main Objectives:
  1. To design a SpaceFibre interface chip in HDL
  2. To verify the chip design in simulation and to validate it on FPGA
  3. To ensure easy migration to ASIC technology (C65SPACE)