Demonstration of SpaceFibre Technology Usage for Image Processing Applications

Activity: Polish Industry Incentive Scheme

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Abstract:

The main objective of the Demonstration of SpaceFibre Technology Usage for Image Processing Applications project (abbreviated as SpaceFibre Image Compression - "SFIC") has been to demonstrate a parallel operation of several instances of CCSDS-121 and CCSDS-123 compatible multispectral image compression IP cores on high-performance FPGA evaluation board. This lossless data compression algorithms' operation has been demonstrated by using data transmission speeds up to 2.5 Gbps net data rate fed through the SpaceFibre (SpFi) interface.

Another important goal for the demonstrator has been to show the capabilities of the SpFi as a high-speed interface used to transmit hyperspectral images to the CCSDS-121 and CCSDS-123 compression cores.

It has been required to be able to use either standalone CCSDS-123 IP core or the combination of both CCSDS-123 (working as a pre-processor) and CCSDS-121 IP cores (creating so called SHyLoC) to compress hyperspectral images corresponding to two different datasets: AVIRIS and LANDSAT.

The requirements for this project have been prepared by the TAS-E engineering team, having large experience in on-board data processing and image compression related projects.

Achievement of above objectives has been demonstrated by development, integration and tests of the SFIC Breadboard Model (SFIC BB). The SFIC BB has been built around the following hardware elements:

- RTG4-based development kit from Microsemi,
- Star Dundee FMC expansion card that incorporates four SpaceWire and two SpaceFibre interfaces.

The RTG4 FPGA is the central component of the electronics.

Tests have been orchestrated using COSMOS suite from Ball Aerospace and written in Ruby.

Within this project TRL 4 has been achieved.