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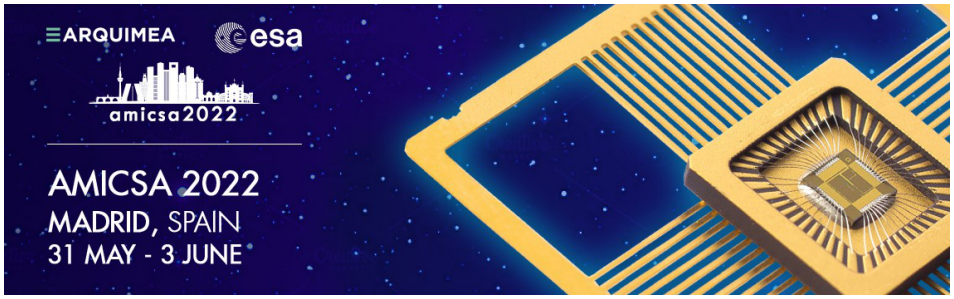

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Custom cell-, circuit-, and system design of ICs for space applications / 1

NIRCA MkII – IR Image Sensor Readout and Controller ASIC

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NIRCA MkII is the second-generation ASIC from IDEAS for readout from infrared (IR) image sensors, e.g., HgCdTe/MCT-based focal plane arrays (FPA). The ASIC aims at reducing the size, weight, power and cost (SWaP-C) of infrared sensor readout systems by integrating the necessary functions and performance on a single ASIC. The NIRCA MkII is a radiation-tolerant integrated circuit (IC) system-on-chip with operating temperature between -40℃ and +85℃. Figure 1 shows the block diagram and interfaces. The ASIC includes 16 video channels, each with a 1× to 8× programmable gain amplifier (PGA) and a pipeline ADC with 14-bit and 16-bit output options running at 12 Msps. Analog input offset is adjustable in the analog domain with fine-tuning of gain and offset in the digital domain. Digitized sensor data is output on a 9×480-Mbps high-speed serial LVDS interface (TX<0:8>). The ASIC provides a digital interface (DIN/DOUT) for controlling the sensor, and analog reference voltages (AOUT) for biasing the sensor.
NIRCA MkII is programmed via an SPI interface. After a program has been loaded into the internal ECC RAM the internal sequencer can execute a variety of tasks, e.g., waveform generation, ADC sampling control, configuration and control of both internal analog and digital modules. At this conference, we will present the results of the validation campaign.
The NIRCA MkII ASIC is developed under the ESA project Control ASIC for Earth Observation Infrared Detector. The project has been funded by the European Space Agency (ESA), the Norwegian Space Agency (NSA) and IDEAS.

Other / 2

Radiation Hardened 6.25 Gbps Serializer-Deserializer IP in 65nm Technology (GENESIS)

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A radiation hardened high speed serializer-deserializer (SerDes) IP for aerospace applications is presented. It is developed in TSMC 65nm technology, using the DARE65 rad-hard digital library. The maximum speed will be 6.25 Gbps and the power dissipation will be lower than 300mW per channel.

Integration of high-speed SERDES macros in a complex ASIC requires full-custom, application specific mega-modules (or multi-channel modules). These modules must be complete with I/O interfaces, power routing and appropriate noise isolation techniques. The existence of different applications and varying electrical specifications of different standards makes the iterative process involved

in traditional mega-module design both cumbersome and cost-prohibitive. This issue is even worse for aerospace ASICs where the low number of parts needed for the application leads to low budgets for new ASIC developments. A SERDES IP which can be easily integrated in other ASICs is the right approach for low volume rad hard ASIC developments where high-speed transmission capabilities are required.

The IP will be compatible with different speeds ranging from 6.25Gbps down to 1Gbps. Speed is achieved using five techniques: (1) a driver circuit that supports programmable preemphasis to deal with cable distortion, (2) a complex adaptive equalization, based in Feed Forward/Decision Feedback (FFE /DFE) equalizers that compensate for various loss profiles of the channel; (3) an Automatic Gain Control and Continuous Time Linear Equalization (CTLE) to compensate the channel attenuation and distortion, (4) a low-jitter clock-and-data recovery (CDR) circuit that enables multiple data rates with corresponding clock generation; (5) various testability features including different type of loop-backs, PRBS generation/checking and (6) Single Channel Stacking to create multichannel systems by joining together single channel IPs. These techniques enable compatibility of the architecture with multiple ASIC requirements- speed, data rate, different cable length/quality and number of channels - without any redesign on the SerDes macro.

The receiver front-end plays a critical role in determining the operating speed and loss-compensation capabilities of the transceiver. Transmitting NRZ data at 6.25Gb/s over a cable/backplane, even at short distances results in significant inter-symbol interference dictating the use of preemphasis in TX and receiver-equalization techniques. The adaptive equalizer forms the front end of the RX that compensates for > 12 dB of loss at 3GHz for all process conditions. This equalizer uses the incoming data and "learns" the best way to compensate for the distortion before the data is recovered. Although preemphasis partially compensates for the loss in the physical link, the RX equalization capability is maximized to achieve a Bit Error Rate (BER) of at least 10-12 in GEO orbit.

Market and customers are pushing the boundaries to increase the data rate, in the range of tenths of Gbps. This is very challenging because it will imply a new set of different techniques like TX Feed Forward Equalizers, speculative RX equalizers, sub rate clock generation and possibly PAM4 codification, together with the use of smaller and faster fabrication nodes, which are more expensive and more difficult to design with.

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Space Applications for analogue and mixed-Signal ICs / 3

Performances of LIROC with SiPM: a Rad-Hard Front-End ASIC for Space LIDAR

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LIDAR is a distance and speed measurement device using reflection characteristics of emitted light. In space applications, time-tagging LIDAR allows scanning planet surface before landing missions,

formation flights by measuring distances between spacecrafts or atmospheric backscatter measurements. The main requirements for the read-out electronics are trifold: single-photon time-tagging capabilities for long range measurements, timing resolution better than LIDAR system (SiPM intrinsic resolution, laser pulse-width, etc.) and minimized dead time.

LIROC is a 64-channel front-end R&D ASIC designed to read silicon photomultipliers delivering charges in the range 50 fC - 10 pC. The ASIC is composed of a 1 GHz RF preamplifier followed by a fast discriminator and low swing LVDS fast driver with a power consumption of 3 mW per channel. The circuit exhibits also a fast return to baseline thanks to its tunable pole zero cancellation circuit prior to the preamplifier. The ASIC also embeds channel-wise DAC for SiPM overvoltage adjustment. Designed in TSMC 130nm, LIROC can furthermore withstand radiation environments up to multi-MRad radiation levels. LIROC configuration can be programmed using an I2C interface that has been triplicated for SEU tolerance.

LIROC has been extensively characterized: first, a pulser has been used to inject an equivalent charge using a detector-like capacitance connected to the channel under test, second measurements have been performed with multiple SiPM devices using a LASER testbench. The ASIC has a Single Photon Timing Resolution of 3.9 ± 0.4 ps RMS when coupled to a detector-emulated capacitor of 100 pF (with an injected charge of 160 fC obtained with a 200 ps transition time voltage step through a 10 pF capacitance). When coupled to SiPM, LIROC time resolution is therefore limited by SiPM intrinsic performances, as state-of-the-art devices have around 70 ps FWHM time resolution (expressed as FWHM to take into account the tail of the Time-Of-Arrival distribution due to delayed photon conversion). LIROC has also shown excellent double-peak separation with 100% efficiency for double pulses separated above 3 ns, which is consistent with photocounting capability of up to 300 MHz. LIROC allows also time-walk correction and input charge estimation thanks to Time-Over-Threshold/discriminator width measurements. Results from LASER testbench will be detailed and compared with simulation.

LIROC architecture will be described, as well as foreseen spatial LIDAR with CERN PicoTDC enabling sub-centimeter resolution with picosecond TDC precision. This project results from the work of the collaboration between WEEROC and OMEGA and has received funding from the ATTRACT project funded by the EC under Grant Agreement 777222.

Custom cell-, circuit-, and system design of ICs for space applications / **4**

A Signal Processing ASIC for Synthetic Aperture Based EO Instruments

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The astrometric systems Very Large-Scale Baseline Interferometer and currently under development Event Horizon Imager uses the Aperture Synthesis principle to track and measure cosmic phenomena. The main advantage of such an Aperture Synthesis approach is that the image is recreated from a physically distributed set of receivers, which are fewer than the number of points in the reconstructed image. Such an approach minimizes the system's weight but degrades the signal-to-noise ratio and increases the calculation complexity. From a signal processing point of view, Aperture Synthesis is a method of reconstructing an image (not necessarily in visual range, but rather of any electromagnetic spectrum) utilizing interferometry and Fourier transform. The reconstructed image contains the intensity or "brightness" of some object if the received data contains information about the object. The latter data is contained in the phase domain in contrast to the amplitude domain of the astrometric signal. The single-lag cross-correlation of the received signals gives a phase map in the frequency domain after some integration period. This single-lag cross-correlation is usually performed with incoming signals as they are produced. Thus, the cross-correlation performing devices need to process the incoming signals seamlessly.
A signal-processing ASIC for Synthetic Aperture Based EO (XCA) Instruments has been developed to seamlessly cross-correlate two sets of 64 digital 2-bit signals. XCA performs single-lag cross-correlation during preset integration time from 1.5ns to 50.33ms. The 32-bit cross-correlation results are stored in a 64x64 cell-matrix, and these results are serialized through an 8-bit bus synchronized by either an external or internal clock.

Each of 128 inputs can receive digital signals at a 2.667Gb/s dual data rate. Transition voltage (VTT) can be set from 0.4V to 1.25V, and each input can sink up to 9mA. Each of these inputs is terminated by (50, 100, 200, 400, HiZ) Ω termination. XCA can interface with HSTL, SSTL, etc., at high speeds. Any of the inputs are aligned against the 1.334GHz clock by alignment block, which also serves as part of the line communication test harness. The input signal protocol is a simple pilot signal and 2-bit stream sequence. The pilot signal is used to test input communication validity and fix bit alignment due to unforeseen design and operation conditions.
XCA has an inbuilt Digital Control Unit, which controls various aspects of XCA operation. The user can control the specific operation modes through the I2C interface.
The internal digital control and primary function can be tested by Built-in-Self Test. The internal XCA algorithm determines the correctness of the operation of Cross-Correlator ASIC. BIST is controlled through I2C and can be run at any non-operation moment.
The Cross-Correlator ASIC has been radiation-hardened by applying SOI (Global Foundries 22nm FD-SOI) technology, differential pair-based schematics, triple redundancy control, interdigitation, guard ring isolation at the cell level. Cross-correlator ASIC has been designed for temperature ranges from -40℃ to 125℃ and ±10% power supply range.
Applications. Primary application – EHI interferometer delay to spatial distribution conversion. Secondary applications: various DSP algorithms which utilize temporal integration, radar systems.
Keywords. Cross-correlator, RadHard, I2C, DSP, SOI, Delay map, Radar, HSTL, SSTL, BIST, 22nm, FD-SOI.

Custom cell-, circuit-, and system design of ICs for space applications / **5**

Rad-hard Microcontroller with Open Access ISA for Space Applications

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The application field of small satellites develops rapidly over the last years. It is expected that the number of satellites until 2029 will exceed 57000. This opens new perspectives and application possibilities, including replacement of old satellites and more complex processing needs for tasks such as satellite constellation and swarm formation.
For various applications within the satellites the microcontrollers are needed. This includes control domain, with propulsion systems, various robotics applications, motor & mechanisms, DC/DC conversion, or thermal regulation. Another application domain is represented also by scientific instrumentation for control of various sensing devices. Microcontrollers market is already having a number of very good and mature solutions, including products from Cobham Gaisler, Atmel, and several US suppliers (Vorago, Texas Instruments).
One trend in general hardware development is the open hardware approach which rapidly started to develop in the last years. One of the major concepts is the use of open access instruction set architectures (ISA), where the main example is the rapid growth of RISC-V approaches. This trend requires also changes in the space domain.
This development is part of the EU project MORAL, targeting development of microcontroller IC with a 130nm standard CMOS technology, and corresponding development software. MORAL approach exactly addresses this need with the target to develop a completely European, ITAR-free µcontroller for space applications. MORAL approach is based on the novel PEAKTOP architecture (incl. novel open access ISA), and includes formally-verified C-compiler, RTOS and toolchain, and

corresponding demonstrator board.
The microcontroller contains, in addition to the regular execution pipeline, also floating-point unit, memory protection unit, as well as DSP support. The integrated SRAM, based on rad-hard ELT transistors and extended with ECC for SEU correction, should support initially 256 KB, with the perspective of further memory space increase. The microcontroller includes a number of interfaces relevant for space applications, including CAN, UART, SPI, SpaceWire, I2C, MIL-STD-1553 etc. It is important to emphasize also the integration of rad-hard A/D and D/A converters with 12-bit resolution. The former is a SAR-based ADC, while the latter is a resistor-string DAC. The schematic of MORAL design is provided in the attached figure.
The key aspect of MORAL development is the radiation hardening methodology which is consequently implemented at different abstraction layers. Concerning the analog IPs, the hardening has been achieved acting on architecture, circuit and layout sides. For the DAC, the choice of a topology based on poly-resistors (insensitive to radiation) is coupled with proper MOS sizing. Extended use of ELT shapes and guard-rings are common to both. For the ADC, MIM capacitances (insensitive to radiation) and over-design have been adopted. Moreover, digital control section serving analog functions is implemented with proven rad-hard digital library.
At the level of complex digital sequential cells, the TMR (triple modular redundancy) methodology has been applied for filtering SEUs while timing filters address SETs. SETs in control logic are addressed by specific combinational cells, pre-tested for SET sensitivity. SET mitigation is achieved either at circuit level (reducing the number of p-channel and n-channel transistors not directly connected to power supply and ground) and layout level (making leverage on enhanced guard rings also used for SEL mitigation). Extensive use of ELT geometry guarantees TID resiliency well over 100 Krad (Si) making the final SoC suitable for the major part of LEO and GEO missions. At system level, the error accumulation is addressed by use of error correcting codes and scrubbing in memory.
The project started in 2020, and until now significant developments have been performed. The complete RTL processor core has been developed and verified in extensive simulations. The complete RTL platform is also mapped to an FPGA, which is used for co-verification. As for the analog IPs, the DAC have been successfully characterized in lab operation environment. The final integration and back-end design is ongoing. The target process is SG13RH technology from IHP, that is currently under ESA evaluation. The technology has been commercially qualified and used in many products, and radiation hardness features have been verified within successfully finished DLR project. Based on such background we are aiming for 100 Krad (Si) TID hardness, as well as to be SEL-free up to at least 60 MeV·cm2/mg (Si) and with SEU sensitivity > 30 MeV·cm2/mg (Si).
At the software side, CompCert, a formally verified C compiler, was successfully ported to the PEAKTOP architecture. Through its formal verification, CompCert is free of miscompilation and allows the use of code optimizations, even for safety- and mission-critical applications. This ensures the effective use of limited hardware resources. Furthermore, formal verification of software is a major advantage over typical proven-in-use arguments, which are not applicable if the target audience is not a mass-market.
Serving as an operating system, a new separation kernel has been developed to run on the PEAKTOP CPU. The challenging frame conditions, and strong security and safety standards, are combined with an extremely small footprint, to match the embedded memory limitations.
After successful production the produced IC will be functionally verified, but also initial reliability tests will be performed. In parallel we are working on the demonstration board which will include also application demonstration.
PEAKTOP microcontroller platform introduces novel ISA concept and aims to result in competitive mixed-signal solution for space applications. The advanced development stage of digital & analog IPs, as well as system software, provide us with great confidence for successful exploitation of final project results.

Custom cell-, circuit-, and system design of ICs for space applications / 6

Radiation Hardened by Design SONOS embedded Non-Volatile Memory in 180nm

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In this article we report about a design of new mixed-signal eNVM IP in XFAB 180nm technology with HV and SONOS (silicon–oxide–nitride–oxide–silicon) options and hardened against radiation effects. The purpose is to create a non-volatile memory (eNVM) solution for space applications. The design is in final completion stage and test vehicle building is due to be sent to manufacturing shortly afterwards.
The main specifications of the IP are memory size 256x64 of 32-bit words, clock frequency 16MHz (+/-10%), power supply 1.8V/3.3V, area 21.15mm2.
The IP consists of three main parts: digital controller, full custom memory core and high voltage control with third-party charge pump IP (provided by XFAB).
This IP is in scope of DARE180XH platform, in XFAB's xh018 technology.
The mission profile does not imply to use HV operations like program and erase. So, the design boundaries were dictated by the mission requirements. That is why radiation hardening design efforts were concentrated on data safety in read operations.
To address the overall data integrity threats, ECC with data path scrubbing and scrambling/descrambling were implemented. Variable-speed read operation and triple read options were made available for the user to increase confidence in read safety. Degradation caused by TID effects and general aging is mitigated by limited self-calibration techniques.
Further immunity of the analogue circuitry against TID and latchup is preserved by layout design. For that purpose, special DRC were implemented. To improve read operations in harsh environment, especially at the end of life, configurable sense amplifiers were developed.
For testability and functional safety, DFT approach was used.
The digital memory controller was synthesized from RTL and was mapped to a radiation hardened standard cell library with DICE flops and specially designed combinational cells for clock and reset signals SET hardening. Furthermore, all analogue and digital IP blocks were systematically scanned for SET sensitive nodes using an in-house tool and special testbenches. SET filters were added on all critical control signals to improve SEE behaviour.
The test vehicle containing this IP is expected to be taped out in Q2 2022. The characterization, irradiation and reliability tests are planned to use the test vehicle. Space-grade radiation hardened memory is expected to be ready for production in 2023.

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Radiation-hardened technologies for analogue ICs / 7

Accomplishing PROMISE, PROgrammable MIxed Signal ASIC Electronics Framework

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PROMISE project, started at the beginning of 2020, has lived by now more than 2 years of harsh but exciting times of successful microelectronics developments. It has crossed by now the equator of its lifetime. During this time most of the IPs have pass a successful CDR, and the CDR of the Pilot Circuit ASIC, integrating all the IPs, is expected by April this year.

PROMISE stands for PROgrammable MIxed Signal Electronics. It's tailored to bring a flexible mixed-signal ASIC architecture design ecosystem built on a portfolio of silicon qualified hardened IP blocks to the space community. Moreover, the project is intended to provide a flexible mixed-signal ASIC manufacturing and qualification ecosystem, and will provide a full European design environment for new IPs and mid-range ASIC for space applications.

PROMISE is based on a modular architecture built on the DARE180X/XFAB XH018 0.18 micron Mixed Signal HV CMOS Technology that allows the end users to target both simple and complex applications of Mixed-Signal ASICs such as signal conditioning and acquisition, motion control, signal processing, signal synthesis and others. This architecture pivots around a central eFPGA module that provides extra flexibility during the lifetime of the mixed-signal ASIC.

PROMISE has designed an IP library oriented towards the fast design of mixed-signal ASICs by the suitable aggregation of pre-validated modules with the minimum added specific circuitry. It enables mixed-signal ASIC and ASSP approach. IP reuse will ensure a shortest and secured schedule and de-risk the design hardening for mixed-signal ASIC/ASSP.

During the conference, the details of the current status of the PROMISE project will be presented, along the planned Electrical and Radiation Testing to be performed after Pilot Circuit ASIC Manufacturing.

Radiation tests of analogue and mixed-signal ICs / 8

Validation, Characterization and Irradiation Testing of the DARE65T Platform

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The DARE65T platform is an analog/mixed signal RAD-hard platform based on TSMC 65nm RF/LP technology. It includes an extensive variety of library cells like standard cells, IO, Single and Double Port RAM, PLL, ADC and DAC, bringing the first advanced node sibling to the DARE platform family.
This paper introduces a test vehicle, developed to validate functionality, perform electrical characterization and ultimately perform irradiation testing (SEE and TID) to confirm the radiation hardening techniques applied during the library design phase.
The test vehicle contains test circuits to allow for analysis of TID effects on standard technology devices, and circuits for validation, characterization and irradiation testing of the library cells, both in SEE and TID.
Electrical validation and characterization includes the parameter measurement of every device and library cell. For TID, parameter drift up to 300kRAD was measured before, during and after the campaign while the supply current of many individual power domains was monitored accurately, according to ESCC standard TID specifications. In SEE, heavy ion particle strike effects were monitored for all library cells to confirm critical threshold and cross-section figures over a range up to 65MeV·cm2/mg for SET and SEU effects, and up to 75MeV·cm2/mg for SEL effects, complying with ESCC SEE standard specifications. Also here, individual power domains were monitored accurately.
To get a detailed understanding of SEE impact on the standard cells, specific test structures were developed that allow for 10ms periodic sampling and capturing radiation effects, reducing the risk of multiple heavy ions affecting the same cell to less than 5% while reaching a total fluence of at least 1e7 particles/cm2. In total 98 standard cell variations were selected (gate length 60 and 70nm, Vt threshold LVT/SVT/HVT and drive strength up to x16) each reaching up to 1000µm2 sensitive area,

to guarantee sufficient statistical relevance on the final test data. These circuits allow for counting the number and measure the duration of SEE effects. For each of the analog/mixed signal library cells a dedicated test circuit was designed to detect SEE effects. These cells and circuits were instantiated 1 or 2 times only, as their sensitive area is much smaller with respect to the physical area, so SEE analysis was restricted to specific parameters only.
The die was assembled in a CPGA-256 package, which is among the highest pin count standard packages generally available. Nevertheless, as the number of digital control and monitoring pins to all test structures and library cells goes far over 1000, a pin multiplexing strategy was implemented with a radiation hardened SPI interface. A regular production tester was employed to operate the digital pins through the SPI interface every 10ms.
In parallel, it stimulates and measures the analog signal and supply pins directly connected to all analog blocks. Oscilloscopes were used to acquire waveforms of various analog interfaces and to detect SET pulses propagating from silicon to PCB.
In total over SEE 90 runs were performed for 3 samples, 6 LET levels and 5 test cases in the course of 3 days.
The acquired test data for validation, characterization and irradiation are currently being analyzed and test results, along with final platform specifications, will be available by the end of April.

Custom cell-, circuit-, and system design of ICs for space applications / 9

Bringing Proven PoC to Space Grade Ka Band Capable Improved Sampler for Direct Microwave Sampling in Software Defined Radio Context

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see the article in the attached file

Analogue intellectual property and re-usability of analogue circuits in space / 10

Radiation Hardened Versatile 14-bit SAR ADC

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This ADC is composed of mainly 2 blocks:
• An 8:2 analog mux combined with an auto zeroed-amplifier (0dB, 6dB and 12dB).
• A 500kS/s ADC with an internal voltage reference generator (external capacitor free) configurable in differential or single-ended mode 11-bit SAR ADC or in 14-bit SAR ADC (in such configuration the sampling rate is limited to 300kS/s).

All the digital is hardened against SET, SEU and SEL:
• Only radiation-hardened flip-flops (HIT) are used.
• Data out bits are SET-free by means of a Muller-C filter.
• Clock paths hardened by drive strength.
• Signals driving the switches connecting the capacitors to the voltage reference are not SET free up to 60 MeV*cm2/mg. However, any SET on these signals will be filtered thanks to the limited analog bandwidth of the capacitor bank.

The 14-bit pseudo-SAR ADC is essentially an 11-bit classical SAR ADC (already existing component from the DARE180U library) combined with a 3 bits sub-DAC. The main SAR ADC (11 bit) uses a unit cap of 12.5fF and has 2 capacitor banks of about 25pF (2048 unit cap). The intrinsic matching of

these capa banks is well above the 11 bit of the original ADC and allows us to reach an accuracy of 14 bit. To add these 3 extra bits on the existing 11 bit SAR ADC there are several possibilities:
- Increase the number of unit caps from 2048 till 16384, but it will create a very big sampling capacitor (2 times 200pF) and furthermore we lose the benefit to reuse a silicon-proven ADC (major change of the layout and the schematic).
- Implement a second capa bank of 8 unit cap connected to the main capa bank of 2048 unit cap thanks to a bridge cap. But in that case the ratio between the 2 capa bank (8/2048) is not optimal and will lead to a loss of accuracy.
- Add a sub-DAC with binary-weighted downscaling of the unit cap. It is difficult to create a smaller capacitor than the unit capacitor and keep a good matching. But as the SAR ADC is based on charge sharing, another solution is to use the unit cap of 12.5fF and to store on it smaller voltage (Q=V*C). This can be easily performed by creating sub-voltage references: the original voltage reference VREFP/VREFN is extended by adding 7 extra intermediate voltages.

On top of that, some extra capacitors (heaving each the same value as the unit cap) have been added in the sub-DAC to have the possibility to add a pseudo-random offset to the sampled signal and to perform at the end a Diethering. The Diethering is intended to reduce the mid-code INL discontinuity.

The comparator has been also slightly redesigned to reduce his equivalent input noise to a 14-bit level.

The capacitor matrix and their switches are insensitive to SEU (i.e. permanent capacitor charge error) except the3 switches on the capacitor bank side connected to the comparator. Indeed, if during the conversion a charge is injected when the switches connecting the capacitors to the voltage references are on, this charge is stored on the capacitor bank. But these switches represent a very small cross-section and will lead to many data corruption

Implementation of Radiation Hardening on analogue circuits at cell-, circuit- and system-design level / 11

First Silicon Enabling Rad-Hard Non-Volatile Memory in 22nm Technology for Space Applications

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In this article, we report the design of new analog and digital IP in 22nm FDSOI and against radiation effects (DARE). The purpose is to enable a magnetic non-volatile random-access memory (MRAM) for space. A test vehicle has been taped out. It contains a range of analog IP for powering and clocking the test chip and to provide safe power up and down sequences. These blocks are integrated into a monolithic power management unit (PMU) macro instantiated at digital top level. The digital part is synthesized from RTL and mapped to an 8-track radiation hardened standard cell library with DICE flops and specially designed combinational cells for clock and reset tree. The chip communicates to the world using a new hardened IO cell library for 1.8V and 3.3V. A fuse box provided by the foundry is used to store trim and config data.

Radiation tests of analogue and mixed-signal ICs / 12

Detailed SET Ionized Charge and Pulse Duration Measurement of a 65 nm CMOS Technology

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This paper presents the measurement results of Single-Event Transients (SET) in a commercial 65nm CMOS technology. The heavy-ion test campaign measured both total SET ionized charge and SET pulse duration. In this test chip, single transistors of different types and dimensions were implemented as victim devices. SET variation due to different supply voltages also was investigated. The detailed measurement principle and circuits are described in [1].

The test chips were irradiated with heavy ions at the Heavy Ion Facility (HIF) in UCLouvain, Belgium. Nickel and Xenon are used in this test with different incidence angles (0o and 45o) to obtain a different effective LET. Two chips were tested at room temperature and exhibited consistent results. During the test, over 20000 SET events were observed on each chip.

SET ionized charge measurement

The SET charge collection of 65 nm technology follows the prediction. For example, the PMOS devices exhibit a smaller collected charge than the NMOS devices. DNW devices collect more than 30% less charge than non-DNW devices. The longer channel length of the devices results in a more charge collection and a higher sensitive area. However, some of the results are not as expected. Conventionally, the drain area is considered the SET-sensitive region of the transistor. From the measurement results, the unit device cross-section is larger than the expected unit device drain area. Specifically, the gate and even source area need to be taken into account.

SET pulse duration measurement

When the LET is high enough to produce a pulse to trigger the measurement circuit, the measurement results form a bell shape on the pulse duration vs. occurrences plot. A higher effective LET heavy ion can cause a higher most-frequent duration (mean value), a wider duration distribution range (variation), and the total number of occurrences. Besides, a longer channel can cause a more extended duration since the total transistor area is increased. When comparing the sensitive area of the non-DNW devices with the DNW devices, unexpected results are founded. DNW devices show a larger unit device cross section compared to non-DNW devices. It indicates that the DNW makes the victim devices more sensitive at high effective LET situations in pulse duration measurements. This phenomenon can be caused by the potential rise in the p-well followed by the injection of electrons into the p-well from the source.

More detailed information can be founded in [2].

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Other / **13**

DARE22 Test Vehicle Design for a 22nm FDSOI process

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This paper presents the test vehicle (TV) of the rad-hard library developed at IMEC, referenced with the acronym DARE22G, that reflects the "Design Against Radiation Effects in 22nm". Thanks to this test vehicle, the functional validation, the electrical performance, and the radiation hardening and sensitivity (SEE and TID effects) of the DARE22G library and a commercial DPRAM will be performed.
The TV includes; 1) digital core cells, mainly 228 combinatorial logic cells, 48 clock gating, 5 radiation-hard (DICE) and 12 standard sequential flipflops. 2) IO cells, including bidirectional digital IOs, and LVDS. 3) a TID sensor with an adaptive back-bias generator, 4) voltage and current references, 5) a 3GHz ultra-low jitter Phase-Locked Loop. 6) 1 GHz ring oscillators. 7) a commercial DPRAM. 8) a radiation-hard SPI (Serial Peripheral Interface) controller and control/monitor registers have been integrated to this TV, in order to control the testing of all the previous blocks.

Multiple instances of the digital core cells and DPRAMs are necessary to achieve enough sensitive area for the SEE testing. This has been respected for all the victims under the test, except for the radiation-hard flipflops. In fact, to fit inside the available area for this TV (15mm2), the sensitive area of these flipflops has been divided by two, and only 5 relevant flavors of the 12 available have been selected. However, the radiation exposition time for these DICE flip-flops will be doubled with respect to the statistical relevance.
Many structures have been designed to allow the SEE testing of the different blocks. For instance, the combinatorial logic cells have been split in many parallel short chains with maximum 24 cells, to limit the pulse broadening effect. A specific block called Combiner, is designed to merge these parallel chains into one node (making data handling more manageable). Beside the SET detection of the combinatorial logic cells, the duration of these events will also be estimated.
The 1Ghz ring oscillators are intended to evaluate the delay variation of the logic gates versus TID. But also, to calibrate the delays used for the estimation of the SET duration.
Beside the SET detection for the clock gating cells, the propagation of such events between victims can also be detected. The SEU hardening of the commercial DPRAMs, and the sequential flip-flops will be tested by a comparison of the contents of these cells before and after irradiation.
Fast comparators have been designed to allow the SET detection of the voltage references. IO receiver cells are equipped with SET-detecting latches; IO transmitter cells are connected in analog loopback mode to two receiver cells with SET-detecting latches, to distinguish between RX and TX SET effects.
Using the TID sensor, the adaptive back-bias generator automatically compensates for any TID effects by trimming the back-bias voltage to a level where the digital circuitry performance can be maintained.
The 3GHz PLL has been designed to guarantee a jitter lower than 300fs. To be able to measure such low jitter with a standard 256 CPGA package, a dedicate buffer with a specific IOs ring has been designed.
Acknowledgement:
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Analogue intellectual property and re-usability of analogue circuits in space / 15

Rad-Hard Mixed-Signal IP-cores in a Fully Depleted Silicon-On-Insulator 22nm Technology

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The 22FDX technology from Global Foundries is a commercial cutting-edge manufacturing process for integrated circuits. This process combines a characteristic minimum gate length of 22 nm and a FD-SOI (Fully Depleted Silicon-On-Insulator) multi-layered structure. These technological features allow adaptative body bias, ultra-low voltage supply and ultra-low leakage, that benefit, from an electrical circuit application point of view, power-efficient RF signaling, high-performance computing, and robust MRAMs (Magneto-resistive Random-Access Memory). Therefore, this technology is extremely suitable to overcome the current product solutions used in high-speed and low-power AMS (Analogue and Mixed-Signal) applications. Particularly, the SOI technological feature guarantees immunity against single event latch-up.

Although the 22FDX technology is noteworthy, it also presents several challenges for AMS applications. The ultra-low voltage supply leaves reduced space for analogue signals. Additionally, the inter-device variability of the threshold voltage due to short channel effects voids some design assumptions used in classic circuit structures. Moreover, for AMS Space applications, ionizing radiation affects the threshold voltage of the FET (Filed-Effect Transistor) devices and degrades the performance of linear circuits. In return, the high operational speed of the technology devices increases the time resolution. Consequently, novel circuital solutions are required to cover the same higher-level functionality.

Our ongoing research, in the frame of the EFESOS project, is focused on the development of several rad-hard AMS IP-cores suitable for their integration in complex SoC (System-on-Chip) products for Space applications. For the time being, the design of a high-speed (2 Gsps) medium resolution (10-bit, 5-ENOB) DAC (Digital-to-Analogue Converter) and a high-speed data transmitter (10 Gbps, 1E-12 BER) IP-cores has been accomplished. Furthermore, the design of a high-speed (2 Gsps) medium resolution (10-bit, 9-ENOB) ADC (Analogue-to-Digital Converter) IP-core is ongoing. Although verified by simulation (or partially verified in the case of the ADC), none of these designs have been electrically tested yet. In any case, there are still not similar European solutions available in the market based in the 22FDX technology and proven under radiation.

The DAC has a current steering segmented architecture, taking the best of the binary-weighted and thermometrical approaches for the current source implementation: on one hand, binary weighted current sources occupy smaller area and are easier to control; on the other hand, thermometrical current sources bring lower DNL (Differential non-Linearity), greater dynamic performance, and monotonicity. Therefore, the combination of both topologies brings a good balance among dynamic performance, power consumption, and area. The 10-bit digital input is binary coded. The six MSBs (Most Significant Bits) drive the thermometric segment by means of two binary-to-thermometric decoders: the most significant three control the row decoder, and the least significant three the column decoder. In fact, the 63 unary elements of this segment are arranged physically and logically in a matrix configuration to optimize area. The four LSBs (Least Significant Bits) are synchronized with the six MSBs with a delay equalizer, so that the binary-weighted current sources are aligned in time with the unary ones.

The data transmitter converts low-speed (up to 625MHz) words (16-bit) into a high-speed single bit stream up to 10 Gbps. Transmitted data can be encoded in an 8b/10b scheme. A high-speed clock (up to 5 GHz) is obtained by multiplying the input clock (up to 625MHz) and used to synchronize the data transmission. The data are serialised using a DDR (Double Data Rate) high-speed shift register and then sent to the communication channel using a CML (Current-Mode Logic) high-speed driver with 50Ω output impedance. In addition, the transmitter allows signal pre-emphasis to mitigate the effect of the channel high frequency attenuation. The pre-emphasis levels are configurable to adapt the transmission to different channels.

The ADC digitize a high-frequency analogue signal (up to 1.4 GHz) with a 10-bit resolution. It is implemented with an 8-stage pipelined architecture. Each of the initial seven stages is composed by a ping-pong residue amplifier and a 1.5-bit ADSC (Analogue-to Digital Sub-Converter). The seven MSBs of the ADC output are obtained from the redundant digital information generated by these initial stages. The three LSBs are directly obtained from the final stage, which is implemented as a 3-bit flash ADSC with a one-hot digital output after bubble correction. A digital core aligns the data

of the different stages and corrects detected errors. All the composing parts of the ADC operate at 2 GHz.

Space Applications for analogue and mixed-Signal ICs / 16

100/1000Mbps Space-Qualified PHY for TTEthernet Data Network in Gateway

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Ethernet is becoming more common in spacecraft to enable hardwired communication speed, support higher data rates, and facilitate interoperability between satellites and other spacecraft. As Ethernet in space applications continues to expand, Microchip Technology has introduced a space-qualified Ethernet transceiver.

In the presentation, Microchip will introduce the VSC8541RT, European radiation tolerant Gigabit Ethernet PHY developed in collaboration with the CNES. Microchip will explain the qualification and radiation activities held during the qualification of the product and a review of the ceramic and plastic quality flow will be detailed.

TTTech Aerospace develops TTEthernet network platform devices to enable the design of fault-tolerant and reliable network system architectures for deep space missions. TTTech will present the usage and validation of Space Qualified PHY in a reference TTEthernet design (SONIC) for Gateway.

With Rad Tolerant space qualified Ethernet Gbit PHY implemented in a TTEthernet Equipment reference design, Microchip and TTTech are providing a full system implementation which demonstrates the performances of the Ethernet Physical Layer device. This reference design is a good starting point to enable any TTEthernet system development for space applications like Lunar Gateway communication interface.

Radiation tests of analogue and mixed-signal ICs / 17

Flexible Test System for Single Event Effect (SEE) Characterization of Digital and Mixed-Signal Integrated Circuits

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This paper presents a flexible Single Event Effect (SEE) test system designed to detect and record Single Event Upsets (SEU), Single Event Transients (SET), Single Event Functional Interrupts (SEFI) and Single Event Latch-ups (SEL) that may arise in digital and mixed-signal ICs from irradiation by heavy ions. The test system is based on a digital core synthesized on an FPGA, a Cortex-M3 Armv7-M microcontroller and miscellaneous circuitry devoted to providing the required supply voltages,

process SEL phenomena, generate and process input/output test signals and monitor key voltage levels.

Space Applications for analogue and mixed-Signal ICs / **18**

A Mixed-Signal, Single Event Upset Tolerant Analog Front-End IC for Redundant Electromechanical Actuator Applications.

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Abstract

A highly integrated, mixed signal IC implements most functions needed for acquisition and for control synchronization in redundant electromechanical actuator applications currently targeting aviation/launch/low Earth orbit. The IC is implemented using circuit and system design techniques to be immune to single events affecting internal circuits and/or communications interfaces. Actuator system design is highly simplified, and system reliability is increased by dramatically reducing the number of components v.s. traditional approach.

Introduction

Electronics for electromechanical actuators usually extend from the sensors for position/velocity to be controlled (usually L/RVDT or resolver) to driving the currents in the windings of an electrical motor and brake solenoid. Typically, besides position, other sensor data related to safe operation of the actuator is needed (e.g. temperature at several points, torque/pressure, currents, voltages etc.). This data is fed to a control algorithm that is executed via software on an MCU or via DSP and state machines if running in an FPGA fabric. Control outputs in the form of PWMs are fed via gate drivers and power devices to the motor/brake. In this type of control, usually, a synchronous sampling scheme is needed to reduce system interactions.

While high-safety, high-reliability electro-mechanical actuator design normally involves a redundant scheme it also requires quite a large amount of IC and discrete devices to cover all functions (see Figure 1). Therefore, there is a need to integrate as many of these functions as possible to reduce size/mass and increase reliability at system level.

A Fully Integrated Analog Front-End IC for Electromechanical Actuators 1

A fully integrated analog front-end shall cover all acquisition functions and support synchronous sampling while implementing a SEU immune interface to the MCU/FPGA processing. Additionally, the IC shall have a simple power scheme while still interfacing with some of the sensors' larger voltage. Early in the design process the decision was made to not integrate gate drivers and power devices to drive the motor windings to allow the usage of same AFE with different actuator power/voltage level combinations. Also, the level shifting/isolation needed for current and DC line voltage sense is not included in the IC as it is application dependent.

The following is a summary of the functions that are integrated in this circuit (see Figure 2 - AFE block diagram):
• Redundant LVDT/resolver driver with primary voltage sense
• Redundant LVDT/resolver 2 x secondary sense supporting 5/6 wire sensor connections
• Multiple PT100/PT1K channels supporting 2/3/4 wire sensor connections
• Multiple 4-20mA loop sensor interfaces (high side power switch with protection and low side current sense) for other sensors
• Redundant motor DC line voltage sense channels
• Multiple motor winding current sense channels
• Internal DC regulators to support single 10-30V input supply
• Internal register file for ADC conversion results and subsystem status using triple redundant storage

• Fully programmable set of PWM generators that are synchronous with the overall channel acquisition.
• Redundant SEU immune SPI/UART communication interface to host with hardware single error correction / double error detection.
• Internal fault checkers and redundant fault signaling.

This IC implements an extended set of fault-checking for inputs impedances, internal supplies compliance and measurement data range thus detecting open /shorts or parametric faults internally or by using host-level software drivers. Additionally, the AFE sports two dissimilar reference voltage blocks with a cross-checker to detect parametric drift. This way reference value drifts and ADC parametric errors can be detected during normal operation while acquiring data.

For SEU immunity, the higher accuracy channels (LVDT and current sense) are implemented with delta sigma modulators followed by SEU immune decimation filters while the other channels can be fed to one of the two redundant 10-bit SAR ADCs that use triple redundant comparators for the successive approximation decision.

Digital communication (SPI or UART) to the host integrates a single error correction, double error detection hardware encoding to avoid executing incorrect writes from the host and allow for single bit correction of acquisition data received by the host. This is more efficient than the host to operate majority/redundant read/write cycles.

LVDT sensing

The position sensing is done using two independent channels usable as fully independent or as redundant driver / sense. The LVDT drivers can be independently programmed for frequency and waveform and are implemented using a PWM based direct digital synthesis topology with external LC filters. Usually the user will program a sinusoidal waveform and will run a slow amplitude regulation software loop that will update periodically the DDS tables used to synthesize the output waveforms. Overall the circuit can drive up-to 10V RMS sinewave. Two differential voltage acquisition channels are used to sense the DDS generated waveform on the LVDT primaries.

The LVDT secondary channels (2+2) are fed via voltage dividers and some external filtering to per-channel sigma delta modulators. Internally each secondary channel samples a fixed number of samples per LVDT driver period and calculates the true RMS value as the square root of the sum of squares of acquired samples. This is done by a TMR based logic DSP block that implements a first decimation filter, a squarer, an averaging filter with a second decimation and a square root calculation. The RMS value for each of the two secondary channels (A and B) is available as a register value to be read by the host. The actual position calculation is finalized by the host to calculate the relative position as (A-B)/(A+B). Additionally, the host should implement the system level mechanical calibration for position.

The overall position measurement error at system level for one LVDT channel is 1.2E-4xMR and the RMS noise of each sample is below 6.1e-5xMR (where MR is the input measurement range).

The error checkers for LVDT drivers and for sense are able to detect open/short on primary or secondary channels and common mode driver faults for the secondary windings.

Applications

Typical application of LX4580 is a Permanent Magnet Synchronous Motor (PMSM) linear actuator with redundant drive and sense electronics. The full paper will show details of PMSM field-oriented control implemented in software closing the loop with LX4580 and a software-based version of LX4580 synchronization for multi-phase power driver alignment.

Conclusions and Future Work

A highly integrated mixed signal IC with SEU tolerance by design was presented together with results in applications involving electromechanical actuators for aviation/launch and low Earth orbit. Among other blocks it integrates 9 delta-sigma ADCs and 2 SAR ADCs and a single input supply power management scheme allowing to power both internal electronics and all sensors. Position accuracy in system is better than 13 bits and RMS noise is below 1 LSB of 14 bits. Radiation and reliability tests still need to be carried out, preliminary LASER tests predict good SEL immunity, ratiometric measurements and self-calibration for all critical channels should provide good support for total dose performance.

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Custom cell-, circuit-, and system design of ICs for space applications / 19

GaN half-bridge integrated circuits for power converters

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First GaN Half-bridges were developed and tested in the frame of SloGaN VLAIO project. The aim was to achieve integration of high voltage & high current transistors with low voltage control & gate drive devices.

Second step is a full feature 3..8A 200V integrated GaN IC Half-bridge been developed under an ESA GSTP program. Figure 1 shows the run1 (=prototype) of IC.

As a step forward, we are looking forward to develop an high current low voltage point of load converter based on GaN integrated half-bridges and new magnetic components. This PoL converter aims at delivering 75 Amp. current at low voltage output (down to 0.7V) in order to supply high complexity integrated circuits like FPGA or processors.

Implementation of Radiation Hardening on analogue circuits at cell-, circuit- and system-design level / 20

Radiation Hardened DDR3 Physical Interface (PHY and IOs) in Flip-Chip C65SPACE Process

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The aim of this communication is to present the hardening approach that has been followed towards the realisation of a hardened DDR3 PHY when targeted on the C65SPACE platform of ST Microelectronics. The implementation concerns the flip-chip version of the IP. The key points that will be presented are: i) the key requirements the PHY IP should meet, ii) the PHY architecture, iii) the RTL to gate flow that has been executed for the digital part of the PHY with emphasis on the hardening precautions, iv) the gate to layout flow that has been executed for the digital part of the design with emphasis on the hardening of the delay elements, v) the modification of the commercial I/O buffers in order to become hardened while maintaining the I/O pitch as small as possible, vi) the modification of the hardened I/O buffers in order to become flip-chip and vii) the hardening rules that have been followed during the top-level IP integration.
This development has been supported initially by an ESA contract and the flip-chip version of it by a CNES contract.

Development Standards for A/MS Integrated Circuits / **21**

Standards Development - Keeping up with advances in analog, mixed signal and other microcircuits

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Back in 2005 NASA published an analog-to-digital converters (ADC) guideline document. It was widely used for the selection of flightworthy ADC devices for use in space flight applications. Since then, the number of available converter products has really proliferated, with many choices available, in the categories of resolution, power, speed, radiation, packaging, and a combination thereof. The application spectrum has widened as well. This presentation will describe the efforts underway where the NASA Electronic Parts Assurance Group (NEPAG), which ESA partners with, has worked with DLA (Defense Logistics Agency), JC-13 (the manufacturers of government products), and CE-12 (the users of active devices) committees to ensure current military/aerospace standards address these challenges, one example being the insertion of new technology, the Class Y initiative.

Class Y represents advancements in packaging technology, increasing functional density, and increasing operating frequency. These are ceramic-based single-die systems-on-a-chip (SoCs) with non-hermetic flip-chip construction, in high pin count ceramic column grid array (CGA) packages. These products use tiny base electrode metal (BME) capacitors for signal integrity and vented packages for thermal management (e.g., Xilinx Virtex-4 FPGAs). To address the manufacturability, test, quality, and reliability issues unique to new non-traditional assembly/package technologies intended for space applications, we introduced a new concept called Package Integrity Demonstration Test Plan (PIDTP), which provided flexibility to manufacturers in building the products the best way they knew how. This initiative resulted in a major overhaul of the performance specification for microcircuits, MIL-PRF-38535, particularly with respect to requirements for flip-chip, underfill, CSAM, column grid arrays, etc. Revision K reflecting these changes was released in December 2013. The front runner Class Y suppliers are offering functions such as processors, ASICs, and very high-speed A/D converters.

Despite severe disruptions caused by COVID-19, we were able to continue the standards activities in the last two years using virtual formats. The recent progress made in extending the standards coverage to other parts of the technology/application spectrum will also be described: the addition of organic Class Y into the draft of MIL-PRF-38535, revision M; a QMLP task group developing requirements for rad hard / rad tolerant plastic encapsulated microcircuits; a new task group taking off with the goal to develop requirements for 2.5D/3D devices; and others.

Radiation-hardened technologies for analogue ICs / **22**

SAMRH707 Unique Radiation-hardened MCU including a TID robust non-volatile memory

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For several decades, Microchip provides one of the industry's most comprehensive space product portfolio of radiation-hardened and radiation-tolerant solutions that includes high-performance MCUs, MPUs, FPGAs, memories, communication interfaces, frequency and timing solutions, mixed-signal ICs, custom power supplies, diodes, transistors, RF components and more. With product development activities and qualified supply chain in Europe, Microchip France is key contributor to the European space ecosystem delivering European and ESCC qualified solutions.

Spacecraft and satellites are expanding in complexity to provide commercial and military operators with robust new communication and data capabilities, greater reliability, and faster speeds, while the operators continuously seek to reduce cost, size and weight. In this environment, lowering system development costs while enabling greater capabilities and space system integration are ever more critical.

The introduction of Arm technologies for space applications opens-up new perspectives by enabling the use of the same ecosystem well in place in the consumer and industrial sectors. The SAMRH707 is the second Microchip Arm Cortex M7-based rad-hard microprocessor available today on the market. It offers developers the simplicity of a single-core processor and the performance of an advanced architecture without having to implement heavy mitigation techniques as is required for non-space components.

Integration of digital-to-analog converters, analog-to-digital converters, and on-chip non-volatile memory together with a powerful processor core is a key requirement for addressing new challenges in aerospace applications. With the SAMRH707, Microchip provides easy-to-use capabilities in cost-effective, radiation hardened MCUs. Built to support up to 128kBytes of non-volatile code in its on-chip flash, the SAMRH707 is capable to run as a standalone computer without any need for external memories. Thanks to its embedded 128kBytes flash memory and more than 700kbytes of SRAM, the SAMRH707 enables a high level of integration embedding a >100 DMIPS processor unit with digital signal processing (DSP) capabilities, combined with space connectivity interfaces such as SpaceWire, MIL-STD-1553 and CAN FD, along with analog functions such as a 12-bit Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC), in a small footprint designed for high-level radiation performance, extreme temperatures and high reliability

The SAMRH707 can be seen as a new step ahead in the integration of the system directly on a single chip with the integration of the Non-Volatile Memory in addition to the standard peripherals. This leads to optimization of the BOM cost by removing external memory requirements from a board, enables reaching much performant memory access speed, minimizing the power consumption of the system…

The Flash memory embedded in the SAMRH707 product relies on a conventional eFlash with stacked floating gate. Requiring high voltage for programing and erasing, such flash is quite sensitive to TID, thus limiting the capability to increase the product performances up to 100krad(Si) and higher with the NVM activated.

During the last 2 years, Microchip has developed different strategies to improve the cumulated dose level of the Flash embedded in the SAMRH707. This presentation will expose the different technics applied for the TID hardening of the NVM in reading mode.

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ESA Mission Classification and project adoption of new micro-electronics development

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ESA has been working on the development of a system for risk assessment and management that would deliver a classification for a particular mission or application depending on its nature (risk acceptance). As a result, a critical review of some Engineering and Product Assurance standards and methodologies is currently underway. This presentation will address the progress achieved by the time of AMICSA 2022, with a special focus on the development of microelectronic products for space systems. The presentation will provide as well an update on European specifications and qualification methodologies which are acceptable for ESA projects.

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SLIME : a radhard, clockless, I2C slave for space application.

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SLIME (Serial Latchup-free I2c 1Mhz link for the x-ifu Electronics) is a radhard and clockless I2C digital module implemented in a radiation-hardened library based on the BiCMOS SiGe ST_130nm.
This module will be used in the Warm Front End Electronics of the X-ray Integral Field Unit for the Athena space mission.
Due to the sensitivity of the instrument, the module must have low noise and low power consumption. It relies entirely on the I2C clock for its operation, and must operate at a frequency of up to 1MHz. It uses a standard cell library which was modified for greater resistance to radiation, and must remain latchup-free at a linear energy transfer of up to 60Mev*cm^2/mg. It must also remain entirely functional with a TID of 20 krad or more.

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Implementation and Evaluation of Sum-Int ADC IP-core on NanoXplore FPGA

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The Summa-Integration analog to digital conversion principle is used for decades in PiKRON's company designed liquid chromatography spectrophotometric detectors as well as for winding currents sensing in permanent magnets synchronous motors and stepper motors control units. The principle has been implemented into a NanoXplore FPGA device on NX1H35AS-EK evaluation kit equipped by an analog front-end bread board in the frame of the GSTP De-Risk funded project.
The provided open-source/open-hardware design files which allows to synthesis of the converter control logic for multiple resolutions and sample rates according to actual target applications requirements. The analog front end KiCAD data are provided as well (see the project GIT repository https://gitlab.com/pikron/projects/sumintadc).
The original simple design used on customer or industrial grade FPGAs was able to realize resolution about 14 bits by only single external operational amplifier per channel. In the combination with precise (chopper stabilized) amplifiers, analog switches and comparator resolution better than 20 bits has been obtained in the past.
Very limited portfolio of analog components (operation amplifiers, analog switches, precise voltage refernces) with space qualification was major obstacle during the porting to space grade components and radiation-tolerant NanoXplore FPGAs. It complicated design of the analog front-end and change of the input bias and offset currents contributed to conversion characteristics shift and slope changes over temperature tested range -40 to 85℃ more than expected. As the most promising has been found Texas Instruments chip equivalent to their OPA4H014-SEP operational amplifier introduced into their space portfolio at the end of the 2021 year.
The PiKRON company designed system has been evaluated at Laboratory of Precise Measurement of Electrical Quantities (METLAB) of Czech Technical University in Prague, FEE. The complete setup for static characterization with two Keysight 3458A voltmeters, Keysight B2912A source meter and climate chamber ClimaEvent C/180/70/3 has been orchestrated over GPIB from PC unit with CTU developed automation scripts using open Phython components. The Stanford Research Systems DS 360 generator has been used in addition for dynamic characterization. The full 8 channel modulator datastream has been delivered from NanoXplore FPGA to Xilinx Zynq 7000 bases MZ_APO kit which captured and precomputed modulator data stream on PC system TCP request and sent response with data back to the central Python based control system.
The achieved results confirms that design provides enhance of resolution when moving average from n samples is used which is directly proportional to the number of samples (i.e. 1/n noise suppression) up to the limit caused probably by analog reference switch and FPGA clock jitter in range of 25 ps. The expected linearity has been achieved but temperature stability requires further design phase. The secondary/experiment goal to design high-resolution Sum-Int ADC conversion frot-end based on space qualified components was not successful at the first trial. The found problems and components limits will be presented as well.

The actual PiKRON's Sum-Int ADC technique has been introduced in the paper:
PÍŠA, Pavel; PORAZIL, Petr. Σ-Integration Analog to Digital Converter, Idea, Implementation and Results. IFAC Proceedings Volumes, 2005, 38.1: 85-90., Congress of the International Federation of Automatic Control. 16th IFAC World Congress: article online https://www.sciencedirect.com/science/article/pii/S1474

Other / **27**

TAS Belgium RadHard ASICS (DPC and HSC) : Space applications – Maturity and Innovation

Authors: Alain Van Esbeen[1]; Marc Fossion[1]; Christophe DELEPAUT[2]; Arturo Fernandez[3]; Richard Jansen[4]; Thierry van Humbeeck[1]

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Since more than a decade, Thales Alenia Space in Belgium is investing in a growing portfolio of Rad-Hard ASICs with the Digital Programmable Controller as a flagship paving the way to other ASICs. The brand new High Speed Controller, the" Swiss Knife for DCDC converters", contains an innovative regulation , the Peak & Valley Current Control (PVCC)

In the frame of a growing Rad Hard ASIC portfolio, a new branch of activities is now focused on GaN integrated circuit for power (Please refer to another dedicated AMICSA presentation from M. Fossion et al. , these 3 technologies (high bandwidth analog regulation + digital power management + GaN-ICs), constitute a key chipset leading to a complete breakthrough in dc-dc converters.
These key developments are made possible thanks to Multidomain skills in TAS B, an efficient network of innovative partners, a fruitful collaboration with ESA experts and a strong support from Belgian Delegation.

Other / **28**

TBD

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TBD

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TBD

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New ECSS standards for ASIC engineering and product quality assurance

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Two new ECSS standards,

- ECSS-E-ST-20-40 "ASIC, FPGA and IP Core engineering"
- ECSS-Q-ST-60-02C Rev.1 "ASIC, FPGA and IP Core product assurance"

are expected to be released this Q3-2022 after implementing any final proposals for changes collected during a Public Review expected to end this summer.
Engineering and product assurance requirements will be applicable to developments of analog and mixed-signal ASICs and to analog IP Cores developed for space projects or under space technology programmes.

The talk will summarize the major differences with respect to the old, and still valid ECSS-Q-ST-60-02C “ASIC and FPGA development” (2008). Emphasis will be made to highlighting analog-specific items and new elements as a normative pre-tailoring of the requirements according the “criticality category” of the device.

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