A Signal Processing ASIC for Synthetic Aperture Based EO Instruments

Authors

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Abstract

The astrometric systems Very Large-Scale Baseline Interferometer and currently under development Event Horizon Imager uses the Aperture Synthesis principle to track and measure cosmic phenomena. The main advantage of such an Aperture Synthesis approach is that the image is recreated from a physically distributed set of receivers, which are fewer than the number of points in the reconstructed image. Such an approach minimizes the system’s weight but degrades the signal-to-noise ratio and increases the calculation complexity. From a signal processing point of view, Aperture Synthesis is a method of reconstructing an image (not necessarily in visual range, but rather of any electromagnetic spectrum) utilizing interferometry and Fourier transform. The reconstructed image contains the intensity or “brightness” of some object if the received data contains information about the object. The latter data is contained in the phase domain in contrast to the amplitude domain of the astrometric signal. The single-lag cross-correlation of the received signals gives a phase map in the frequency domain after some integration period. This single-lag cross-correlation is usually performed with incoming signals as they are produced. Thus, the cross-correlation performing devices need to process the incoming signals seamlessly.

A signal-processing ASIC for Synthetic Aperture Based EO (XCA) Instruments has been developed to seamlessly cross-correlate two sets of 64 digital 2-bit signals. XCA performs single-lag cross-correlation during preset integration time from 1.5ns to 50.33ms. The 32-bit cross-correlation results are stored in a 64x64 cell-matrix, and these results are serialized through an 8-bit bus synchronized by either an external or internal clock.

Each of 128 inputs can receive digital signals at a 2.667Gb/s dual data rate. Transition voltage (VTT) can be set from 0.4V to 1.25V, and each input can sink up to 9mA. Each of these inputs is

terminated by (50, 100, 200, 400, HiZ) Ω termination. XCA can interface with HSTL, SSTL, etc., at high speeds. Any of the inputs are aligned against the 1.334GHz clock by alignment block, which also serves as part of the line communication test harness. The input signal protocol is a simple pilot signal and 2-bit stream sequence. The pilot signal is used to test input communication validity and fix bit alignment due to unforeseen design and operation conditions.

XCA has an inbuilt Digital Control Unit, which controls various aspects of XCA operation. The user can control the specific operation modes through the I^2C interface.

The internal digital control and primary function can be tested by Built-in-Self Test. The internal XCA algorithm determines the correctness of the operation of Cross-Correlator ASIC. BIST is controlled through I^2C and can be run at any non-operation moment.

The Cross-Correlator ASIC has been radiation-hardened by applying SOI (Global Foundries 22nm FD-SOI) technology, differential pair-based schematics, triple redundancy control, interdigitation, guard ring isolation at the cell level. Cross-correlator ASIC has been designed for temperature ranges from -40°C to 125°C and ±10% power supply range.

Applications. Primary application – EHI interferometer delay to spatial distribution conversion. Secondary applications: various DSP algorithms which utilize temporal integration, radar systems.

Keywords. Cross-correlator, RadHard, I^2C, DSP, SOI, Delay map, Radar, HSTL, SSTL, BIST, 22nm, FD-SOI.