A Signal Processing ASIC for Synthetic Aperture Based EO Instruments

Paukstaitis Vaidas, Ignas Martisius, Vidas Abraitis

UAB "Si Femto" (Ltd.)

vaidas@sifemto.com, ignas@sifemto.com, vidas@sifemto.com

Abstract

A signal-processing ASIC for synthetic Aperature Based Instruments has been developed for Global Foundries 22nm FD-SOI fabrication process. This article discusses the implemented architecture, developments and requirements, as well as a simple model of a synthetic aperture to generate input and output signals. The architecture of the XCA consisting of two groups of 64 2.667Gb/s input signals, built-in self-test, cross-correlation cells matrix, readout circuitry, and digital control unit is presented. The operation of the XCA is controlled through the I²C interface. The XCA is capable of seamless 2-bit cross-correlation of 2 signals from 2 input groups. High-speed digital interfaces can support multiple digital standards. The XCA function verification method and simulation results of the function at typical case are presented. The power consumption over the temperature [-40, 125] °C, ±10% power supply variation, and corner variation reaches 560mW for the standard cell-based design part, and 3W for custom-created high-speed digital interfaces. The XCA is implemented on Global Foundries 22nm FD-SOI fabrication process, thus the expected SEL immunity is 20MeV cm²/mg and TID - 1MRad.

Keywords. Cross-correlator, RadHard, I²C, DSP, SOI, Delay map, Radar, HSTL, SSTL, BIST, 22nm, FD-SOI.

Introduction

Astrometric systems, namely Very Large-Scale Baseline Interferometer and the currently under development Event Horizon Imager use the Aperture Synthesis principle to track and measure cosmic phenomena. The main advantage of such an Aperture Synthesis approach is that the image is recreated from a physically distributed set of receivers, which are fewer than the number of points in the reconstructed image. Such an approach minimizes the system's weight but degrades the signal-to-noise ratio and increases the calculation complexity. From a signal processing point of view, Aperture Synthesis is a method of reconstructing an image (not necessarily in visual range, but rather of any electromagnetic spectrum) utilizing interferometry and Fourier transform. The reconstructed image contains the intensity or "brightness" of observavble object. The latter information is contained in the phase domain in contrast to the amplitude domain of the astrometric signal. The single-lag cross-correlation of the received signals results in a matrix with a phase map in the frequency domain. This single-lag cross-correlation allows to process incoming signals in real-time and the cross-correlation performing devices are expected to read out the delay map matrices seamlessly.

One of the current ASIC-based cross-correlator developments is a 1-bit cross-correlator. Such a system has a signal-to-noise reduction of 0.64 compared to the infinite case [1]. Also, the targeted instruments of this ASIC does not require an increased number of cross-cross-correlation lags [1]. The clock and data are submitted to the cross-correlating cells by utilizing pipelining method i.e., each cell amplifies clock and data and forwards them to the next cross-correlating cell in some routing fashion. This tends to eliminate clock-data skew and increase performance. The full system is comprised of digitizers on separate ASIC to minimize cross talk between digital and analogue digitizers. Such a digitizer and cross-correlator system could operate at a clock signal of 3.5GHz for special and 2GHz for nominal power supply cases [1]. The final cross-correlation value is 30-bits and 24-bits are read out through serial-parallel-interface (SPI). The power consumption presented is 0.13 mW/channel/GHz.

Cross-correlation Function and ASIC

Figure 1a) shows the distant signal emitter radiating the harmonic signal. This signal reaches the receivers (antennas) which are distributed evenly by d distance. The two sets of 64 receivers are ordered perpendicularly to each other and their cross point is oriented towards the distant signal emitter. The harmonic signal arrives at each antenna at different times and the radial delay is depicted as wavefronts (WF).

The spatial distribution is reconstructed by calculating the single-lag cross-correlation of every possible combination of 2 signals from each group. The result would be a 64-by-64 matrix of cross-correlation values (Figure 1b). Such a matrix is called a delay map. Note, Figure 1b) is for illustrative purposes and presents the delay map in pseudo-colour code. The similar delay map is given into phase part of Fast-Fourier Transform (FFT) input.

The output of FFT is the reconstructed spatial distribution. The single spot is shown in Figure 1c) because the example surmised a single distant point signal emitter. Figure 1c) is also for illustrative purposes and the maximum value of 32 is the result

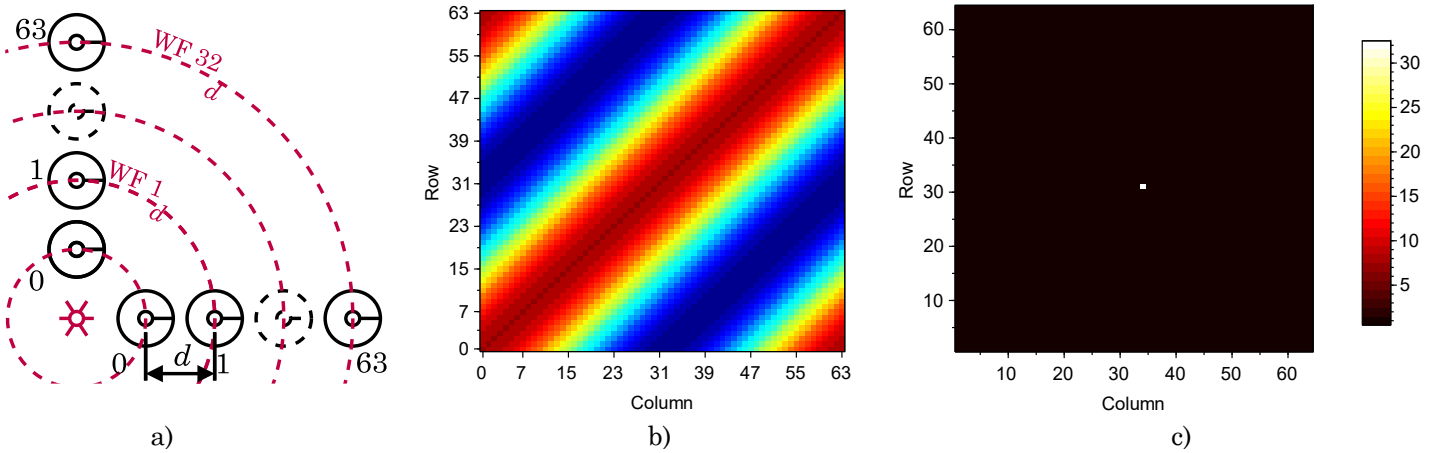

Figure 1. Signal receiver positions (a), Delay Map after cross-correlation (b), reconstructed distant signal (c)

of normalization. The sinewave signals of constant delay difference are applied as test signals during XCA simulation and are expected to be like the Figure 1b) result.

The cross-correlation itself can be realized by one of the two possible flows:

1) collect each receiver's data, transform by FFT, and multiply FFT result,
2) supply each receiver's data in real-time to the cross-correlator device assembled from multiply-accumulate cells.

Method (1) requires the samples to be stored in memory first, then computing the FFT and multiplying the resulting sequences. This method is preferred on ground-based instruments, because high amounts of memory are available. Method (2) does not require high data rate transfres and is able to reconstruct spatial distribution with small amounts of data. This is preferred for space-based applications because of memory weight reduction and radiation tolerance. It is also more radiation resistant since cross-correlation is an averaging operation.

The current Event Horizon Imager project is a non-geostationary space-space interferometer, and is an example of where the cross-correlator system is used. Black hole observations would use circular or polar orbits, observing frequencies up to ~690GHz [2]. This is a concept system that assumes that the cross-correlation of the data streams from two satellites is conducted onboard in real-time within a delay window compatible with on-the-fly relative positioning of sufficient accuracy. Also, cross-correlation is used to reach a sufficiently low rate for data transfer to the ground, where the actual fringe fitting would take place.

The high bandwidth and real-time requirements for EHI can be realized by a cross-correlator system where multiple cross-correlation ASICs are used in parallel. 10GHz bandwidth should require 4 2.5GHz ASICs working in parallel. As previously stated, geostationary cross-correlators may not require multi-lag cross-correlations. The developed ASIC should either hold the previous data in its internal memory or get the data from an outside memory device to support multi lag cross-correlations. Internal memory increases ASIC size, power, noise, and radiation risk compared to specialized radiation-hardened external memory. It is of special interest because cross-correlator memory may need to keep 10Gsamples per channel. Such requirements dictate transmission line based data bus reading conditions. The 50Ω transmission lines and termination connect signal source and cross-correlator directly when a single ASIC is used, and HiZ when multiple ASICs are used in PCB assemblies terminating at the end of the transmission line. Moreover, the provision of real and test signals (during testing of the ASIC) is a concern. Thus, either a specialized multiple ASIC product line should be developed, or the developed ASIC should reuse the current standards and space-qualified integrated circuits. It is good practice to build an ASIC which supports high-speed digital interfaces such as HSTL, SSTL, and LVDS. Keeping in mind that CMOS interfacing can also be done with supply voltages as low as 0.8V, the interface should receive signals at a 0.4V transition voltage level. Such an approach increases the application to other fields. However, there is a risk that high-speed multiple transition voltages cannot be supported sufficiently for all frequencies and interfacing standards.

The second cross-correlation calculation method has been selected as the base of the XCA. This method is less risky to implement since it does not require dedicated memory, the delay difference map is directly calculated. The EHI project requirements outline the cross-correlator ASIC's ability to read data through a digital interface. The cross-correlator ASIC's architecture has been created to read the digital signals through digital interfces, cross-correlate 64 2-bit signals from one group with 64 2-bit signals from another group and to readout resulting delay difference map seamlessly.

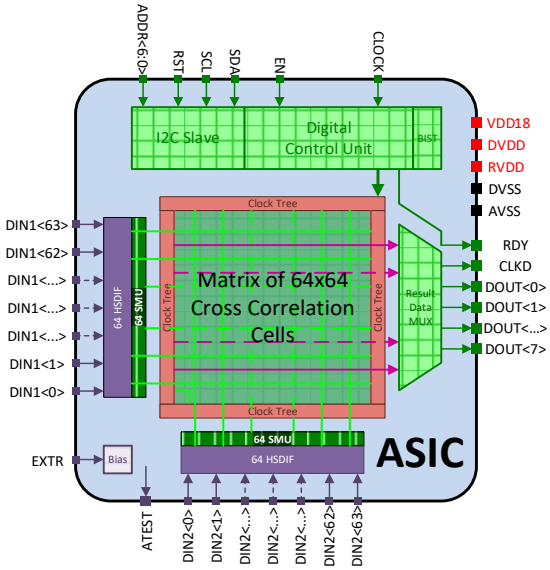

Figure 2. Functional Diagram of XCA

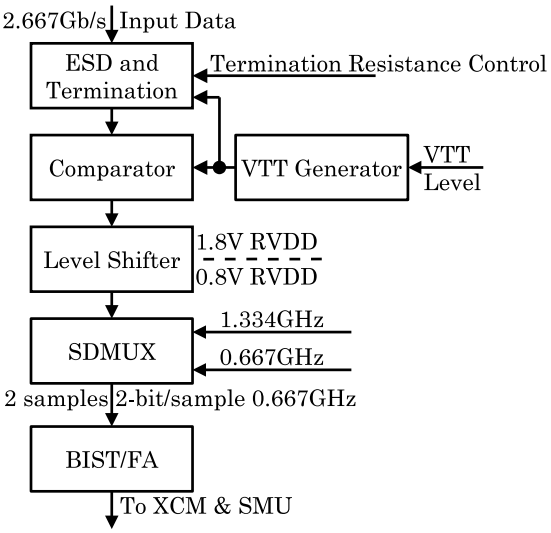

Figure 3. HSDIF Structural Diagram

XCA Architecture

The Signal Processing ASIC (XCA) for Synthetic Aperture Based Instruments has been developed to cross-correlate DIN1<63:0> with DIN2<63:0> signals (Figure 2~~Figure 2~~). They are received by the high-speed digital interfaces (HSDIF) at 2.667Gb/s dual rate. The signals are demultiplexed into 2-bit 2 channels inside HSDIF. Such processing drops the data frequency to 0.667GHz at which statistical measurement units (SMU) and the cross-correlation matrix (XCM) operate. The SMUs collect 2-bit value occurrence data while the XCM cross-correlates each signal. The SMU and XCM 32-bit result data are copied into readout registers after the integration period. Thus, the next integration period can proceed while the cross-correlation result data is read out through the Result Data MUX. The RDY signal informs the cross-correlation data receiver of the integration period's end. The CLKD signal synchronizes the cross-correlation data read out through DOUT<7:0> outputs.

The XCA is controlled by the Digital Control Unit (DCU) and the control data is supplied or read through I²C Slave interface. ADDR<6:0> signal sets the address of the XCA in its aggregating system, EN – enables XCA processing. CLOCK is the main 1.334GHz clock. The clock is distributed by clock tree and used in HSDIFs, SMUs, and the XCM. The bias block provides current to support HSDIFs. EXTR is the external resistance for Bias.

DCU supplies the clock signal for the XCM and SMU, and this internal clock depends on the external CLOCK frequency. Thus, the XCA's operation speed can be adjusted.

The internal digital control and primary function can be tested by the Built-in-Self Test. The internal XCA algorithm determines the correctness of the operation of the XCA. BIST is controlled through I²C and can be run at any non-operation moment.

The ASIC is capable of processing a maximum of 2,667Gb/s data rate sufficient for very sophisticated projects. Multiple XCAs can also be used in tandem to further increase processing power for even more demanding applications.This architecture also enables to use the XCA in real-time radars because the integration time can be shortened by sacrificing the delay map resolution.

HSDIF Description

Every DIN1<63:0> and DIN2<63:0> signal comes into dedicated high-speed digital interface (Figure 3). The maximum dual data rate of the input signal is 2.667Gb/s. The input signal first arrives at a termination resistor (50Ω, 100Ω 200Ω, 400Ω, HiZ) and electrostatic discharge protection (ESD). The other end of the termination resistor is driven by a transition voltage (VTT) generator. This generator can sink or provide up to 9mA current when the termination resistance selected is not HiZ. A comparator shifts the input signal arriving with average VTT Level to approximately 0.8V internal transition level. The differential level shifter shifts voltage level to internal 0.8V rails. SDMUX deserializes 1-bit stream at 1.334GHz dual rate to parallel 2 sample 2-bit/sample single-rate at 0.667GHz. SDMUX output is converted to CMOS, and it drives BIST/FA block.

The following XCM and SMU blocks are supplied either internal test signals or a 4-bit aligned deserialized input data stream by the BIST/FA block. The digital standards BIC, HSTL, SSTL can be supported due to 50Ω termination resistance driven by VTT generator supporting VTT levels of {0.4, 0.45, 0.5, 0.6, 0.75, 0.9, 1.05, 1.25}.

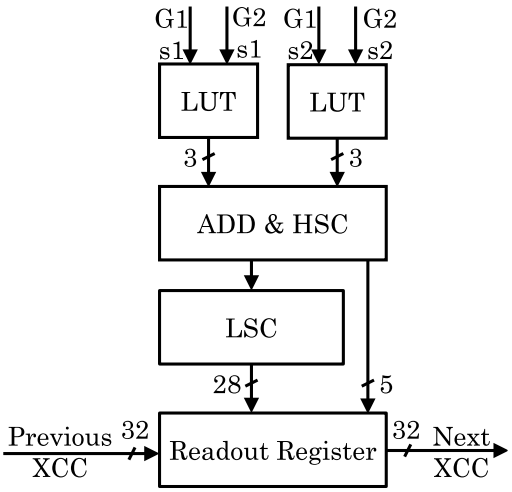

Figure 4. XCC Cell Diagram

Cross-correlator Cell

The cross-correlator cell (XCC) cross-correlates two 2-bit input signals with values encoded as {-3, -1, 1 ,3}. XCC has been implemented as a hybrid architecture (Figure 4) based on assumptions and design methods in [3].

Two inputs of the 2-bit signal from the first group (G1) and two 2-bit signals from the second group (G2) come into the multiplication unit which is realized as two look-up-tables (LUTs). Each of the LUTs multiplies the arrived 2 2-bit signals by each other resulting in the values {-9, -3, -1, 1, 3, 9}. The latter are transformed at the output to {0, 2, 3, 4, 5, 7} to simplify binary encoding and accumulation function. Such an approach reduces the maximum operation speed to 0.667GHz instead of 1.334GHz, reduces dynamic power and relaxes timing constraints.

The LUTs' results are forwarded to an adder and high-speed counter. It is a synchronous high-speed counter (HSC), which accumulates the results of the LUTs. Since the maximum value that can be output is 7+7+7=21, the HSC is designed to be 5 bits long. The second counter is a ripple-carry low-speed counter (LSC). This counter counts overflows of the HSC, therefore, it can operate at 2N lower speeds. The calculated values of both counters are output to the readout register, MSBs coming from the LSC, and LSBs coming from the HSC. This way, only 5 DFFs need to operate at 0.667GHz frequency, lowering power consumption compared to a straightforward approach of having a 32-bit adder. This complexity reduction should be sufficient to achieve the low power needed for the XCA.

A readout register has been built into each XCC to enable readout during the accumulation, i.e., seamless readout. This register loads data from counters and stores them until readout, allowing the counter to continue operation. The 32-bit values are transferred from the previous XCC cell after the readout register contents.

The maximum required readout frequency may be calculated by applying formulae:

$F_{Rmax} = \frac{4096 \cdot 32 + 128 \cdot 32}{8} \cdot \frac{1}{T_{int}}$,

where T_{int} – integration time.

Assuming shortest $T_{int} = 1\text{ms}$, $F_{Rmax} = 16.896\text{MHz}$.

Assuming longest $T_{int} = 460\text{ms}$, $F_{Rmax} = 36.73\text{kHz}$.

Radiation Hardness Estimate

The Global Foundries 22nm FD-SOI has been selected for the XCA because it features short length and thin oxide gates minimizing volume of charge induction, trapping, and improved tunneling of induced particles out of primary gate structure. It is expected that such effects increases TID up to 1MRad for the XCA. The Global Foundries 22nm FD-SOI is inherently immune to SEL between individual transistors. The custom designed cells use only SOI transistors allowing to keep TID high.

The XCA includes triple-redundant ASIC control and register bank to improve long-term control radiation hardness.

XCA has been designed with the following radiation hardness techniques: low CML gain (prevents amplification of SET), differential amplifiers (common mode mitigates SEU and SET in differential signal, increases TID), interdigitated resistors and current mirrors (mitigates SEU and SET).

Various devices fabricated using many different CMOS processes have consistently shown no SEL in guard bar (red. note: contact line, ring) protected circuits up to the highest LET tested (LET > 90MeV cm²/mg)[4]. The same [4] source reports onset threshold is about 20 MeV cm²/mg. We estimate that our substrate tie-downs will reduce SEL between large substrate area up to 20 MeV cm²/mg even for areas with 0.8V supply voltage.

Simulation Results

The XCA has been designed for the Global Foundries 22nm FD-SOI process. The extended temperature range [-40, 125] °C, ±10% power supply voltage ([0.72, 0.80] V for 0.8V, [1.62, 1.98] V for 1.8V) and full corner variation (ss_pre, tt_pre, ff_pre). "_pre" suffix is used for post-layout simulations. All custom designed blocks have been back annotated in such a way that delays match post-layout full RC extract.

The XCA power consumption has been obtained for various operating modes, temperature, power supply voltages and corner variation. The HSDIF, Clock Tree and BIAS consume between 2.9 to 9.1W of power. 2/3 of the power consumption is due to the HSDIF input since it requires to sink or provide up to 9mA current when driving 50Ω termination resistor. 1/3 of power is consumed by HSDIF's SDMUX, Clock Tree, BIAS.

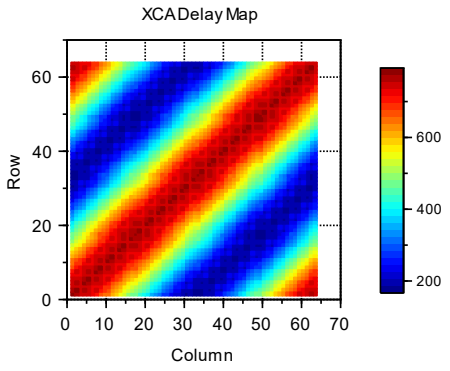

Figure 5. XCA Resulted Delay Map

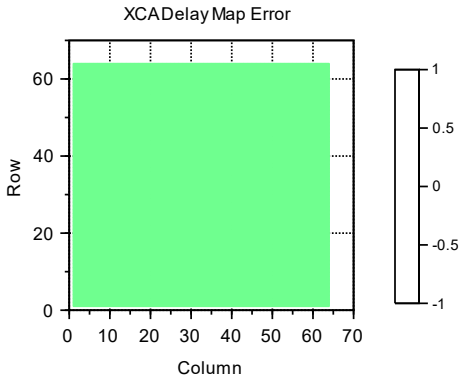

Figure 6. XCA Resulted Delay Map Error

The XCM, SMU and DCU sinks 0.7A and is powered from a 0.8V power supply. The XCCs' total power consumption is 80µW, thus the XCM consumes 330mW at the maximum operating frequency of 0.667GHz. This result can be compared to the cross-correlator presented in [1] reporting 0.13 mW/channel/GHz figure-of-merit (FOM). The ASIC reported in [1] can cross-correlate every channel, thus the XCA has 4096 channels, each channel is 4-bit operating at 0.667GHz. Thus, XCA FOM is 0.051mW/channel/GHz.

The XCA inputs are given 2-bit quantized 200MHz sinewaves with constant delay difference during function simulation. The full XCA is simulated for a 108ns integration period during analogue simulations due to relatively slow simulation speed. The resulting delay difference matrix under the typical XCA simulation conditions (40°C, tt_pre, 0.80V, 1.80V, VTT=0.75V) presented in Figure 5 is close to Figure 1b) where the qualitative expected result is shown. However, Figure 1b) shows infinite resolution while XCA takes 2-bit resolution per channel. A simple Scilab reference model has been programmed to generate a reference matrix. The XCA simulation result matrix is subtracted from the matrix calculated by the Scilab reference model and presented in Figure 6. This plot shows the error of zero for each reconstructed pixel and it shows that the XCA performs as expected. Other simulated circumstances give the same zero error and are not displayed in this article.

Conclusions

The Signal Processing ASIC (XCA) for Synthetic Aperture Based Instruments has been developed to cross-correlate the digitized synthetic aperture signals. The architecture allows to interface with the XCA by a multitude of digital standards such as (HSTL, LVDS) but this comes with increased power consumption of the receivers. The operation can be adjusted through I²C interface and together with support of multiple digital standards can interface various other digital devices such as memories or FPGAs. This allows to apply the XCA in DSP algorithms and radar systems. The XCA control allows to adjust integration time to trade between calculation delay and resolution.

The total ionizing dose is expected to be 1MRad since Global Foundries 22nm FD-SOI fabrication process features short length and thin oxide gates. The XCA includes triple-redundant ASIC control and register bank to improve long term control of radiation hardness. The XCA has been designed with the multiple radiation hardness techniques against SET, SEU and TID in schematic and layout designWith the addition of guard ring structures, SEL is expected to be 20MeV cm²/mg.

The optimally designed cross-correlation cell consumes 80µW while operating at 0.667GHz. This allows to reconstruct the delay difference map with data arriving at 2.667Gb/s through 128 channels. A similar function ASIC reported 0.13 mW/channel/GHz to compare with this XCA's 0.051mW/channel/GHz.

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