# Radiation Hardened 6.25 Gbps Serializer-Deserializer IP in 65nm Technology (GENESIS)

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A radiation hardened high speed serializer-deserializer (SerDes) IP for aerospace applications is presented. It is developed in TSMC 65nm technology, using the DARE65 rad-hard digital library. The maximum speed will be 6.25 Gbps and the power dissipation will be lower than 300mW per channel.

Integration of high-speed SERDES macros in a complex ASIC requires full-custom, application specific mega-modules (or multi-channel modules). These modules must be complete with I/O interfaces, power routing and appropriate noise isolation techniques. The existence of different applications and varying electrical specifications of different standards makes the iterative process involved in traditional mega-module design both cumbersome and cost-prohibitive. This issue is even worse for aerospace ASICs where the low number of parts needed for the application leads to low budgets for new ASIC developments. A SERDES IP which can be easily integrated in other ASICs is the right approach for low volume rad hard ASIC developments where high-speed transmission capabilities are required.

The IP will be compatible with different speeds ranging from 6.25Gbps down to 1Gbps. Speed is achieved using five techniques: (1) a driver circuit that supports programmable preemphasis to deal with cable distortion, (2) a complex adaptive equalization, based in Feed Forward/Decision Feedback (FFE /DFE) equalizers that compensate for various loss profiles of the channel; (3) an Automatic Gain Control and Continuous Time Linear Equalization (CTLE) to compensate the channel attenuation and distortion, (4) a low-jitter clock-and-data recovery (CDR) circuit that enables multiple data rates with corresponding clock generation; (5) various testability features including different type of loop-backs, PRBS generation/checking and (6) Single Channel Stacking to create multichannel systems by joining together single channel IPs. These techniques enable compatibility of the architecture with multiple ASIC requirements- speed, data rate, different cable length/quality and number of channels - without any redesign on the SerDes macro.

The receiver front-end plays a critical role in determining the operating speed and loss-compensation capabilities of the transceiver. Transmitting NRZ data at 6.25Gb/s over a cable/backplane, even at short distances results in significant inter-symbol interference dictating the use of preemphasis in TX and receiver-equalization techniques. The adaptive equalizer forms the front end of the RX that compensates for > 12 dB of loss at 3GHz for all process conditions. This equalizer uses the incoming data and “learns” the best way to compensate for the distortion before the data is recovered. Although preemphasis partially compensates for the loss in the physical link, the RX equalization capability is maximized to achieve a Bit Error Rate (BER) of at least $10^{-12}$ in GEO orbit.

Market and customers are pushing the boundaries to increase the data rate, in the range of tenths of Gbps. This is very challenging because it will imply a new set of different techniques like TX Feed Forward Equalizers, speculative RX equalizers, sub rate clock generation and possibly PAM4 codification, together with the use of smaller and faster fabrication nodes, which are more expensive and more difficult to design with.

[1] Miromico SERDES Tutorial TWEPP 21.09.2018
[2] An ASIC-Ready 1.25-6.25Gb/s SerDes in 90nm CMOS with Multi-Standard Compatibility Yoshinori Nishi, Koichi Abe, Jerome Ribo, Benoit Roederer, Anand Gopalan, Mohamed Benmansour, An Ho, Anusha Bhoi, Masahiro Konishi, Ryuichi Moriizumi, Vijay Pathak, Srikanth Gondi. IEEE Asian Solid-State Circuits Conference November 3-5, 2008
[3] A 6Gb/s Receiver with 32.7dB Adaptive DFE-IIR Equalization Yi-Chieh Huang, Shen-Iuan Liu National Taiwan University, Taipei, Taiwan ISSCC 2011 / SESSION 20 / HIGH-SPEED TRANSCEIVERS & BUILDING BLOCKS
[4] Design of a Programmable Switched-Capacitor Analog FIR Filter. Cameron Lacy. Thesis submitted in conformity with the requirements for the degree of Master of Applied Science Graduate Department of Electrical Engineering University of Toronto. 1999