Radiation Hardened 6.25 Gbps Serializer-Deserializer IP in 65nm Technology (GENESIS)

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Abstract

A radiation hardened high speed serializer-deserializer (SerDes) IP for aerospace applications is presented. It is developed in TSMC 65nm technology, using the DARE65 rad-hard digital library. The maximum speed will be 6.25 Gbps and the power dissipation will be lower than 250mW per channel. It is being developed under the GSTP program with collaboration of ESA.

Integration of high-speed SERDES macro in a complex ASIC requires full-custom, application specific mega-modules (or multi-channel modules). These modules must be complete with I/O interfaces, power routing and appropriate noise isolation techniques. The existence of different applications and varying electrical specifications of different standards makes the iterative process involved in traditional mega-module design both cumbersome and cost-prohibitive. This issue is even worse for aerospace ASICs where the low number of parts needed for the application leads to low budgets for new ASIC developments. A SERDES IP which can be easily integrated in other ASICs is the right approach for low volume rad hard ASIC developments where high-speed transmission capabilities are required.

I. INTRODUCTION

The IP will be compatible with different speeds ranging from 6.25Gbps down to 1Gbps. Speed is achieved using five techniques: (1) a driver circuit that supports programmable preemphasis to deal with cable distortion, (2) a complex adaptive equalization, based in Feed Forward/Decision Feedback (FFE /DFE) equalizers that compensate for various loss profiles of the channel; (3) an Automatic Gain Control and Continuous Time Linear Equalization (CTLE) to compensate the channel attenuation and distortion, (4) a low-jitter clock-and-data recovery (CDR) circuit that enables multiple data rates with corresponding clock generation; (5) various testability features including different type of loop-backs, PRBS generation/ checking and (6) Single Channel Stacking to create multichannel systems by joining together single channel IPs. These techniques enable compatibility of the architecture with multiple ASIC requirements-speed, data rate, different cable length/quality and number of channels - without any redesign on the SerDes macro.

The receiver front-end plays a critical role in determining the operating speed and loss-compensation capabilities of the transceiver. Transmitting NRZ data at 6.25Gbps over a cable/ backplane, even at short distances results in significant inter-symbol interference (ISI) dictating the use of preemphasis in TX and receiver-equalization techniques. The adaptive equalizer forms the front end of the RX that compensates for >12 dB of loss at 3GHz for all process conditions. This equalizer uses the incoming data and "learns" the best way to compensate for the distortion before the data is recovered. Although preemphasis partially compensates for the loss in the physical link, the RX equalization capability is maximized to achieve a Bit Error Rate (BER) of at least 10^{-12} in Geostationary Orbit (GEO).

II. Main specifications

The final goal is to develop a SERDES IP suitable for the aerospace market, which implies high reliability, extended temperature range and radiation hardening, while maintaining the power consumption within a reasonable limit.

Parameter	Range	Units
Multi-Lane stacking	Yes	N/A
Ambient Operating Temperature	-55; +125	°C
Supply Voltage	1.09; 1.32	V

Data Rate	6.25; 5; 3.125; 2.5; 2; 1.5625; 1.25; 1	Gbps
Power consumption per TX/RX channel	250	mW
BER in GEO orbit	10^{-12}	N/A
TID	>100	krad
SEL	>67	MeV*cm^2/ mg
SEFI	>67	MeV*cm^2/ mg

III. TX Section

The block diagram shown in Figure 1 is the SERDES transmitter section. The transmit data is provided through a 16-bit low-frequency bus which uses 1.2V CMOS levels. The data has to be synchronized with an external clock which can be variable between 50 and 312.5MHz depending on the data rate. The data is coded with and 8b/10b which can be disabled in case the user wants to use different codification scheme. The 16-bit data is then converted into a 20-bit word before is sent through the TX link.

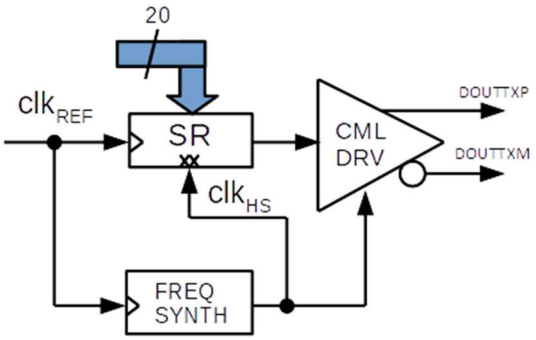

Figure 1. TX Section Architecture.

The encoded data is transferred to a high speed 10-bit DDR serializer, which generates a serial data output at a maximum rate of 6.25Gbps.

The high-speed frequency clock is generated using a Phase Locked Loop (PLL), with a programmable frequency divider in the feedback path. Achieves a maximum jitter architecture of 1.7ps RMS or 0.1UI, while keeping the radiation hardening behavior needed to achieve the adequate BER.

The output driver is a Current Mode Logic output stage (CML), which provides a maximum differential amplitude of 1200mV$_{pp\text{-}diff}$, over a common mode of 900mV. The output driver provides also "Preemphasis", which allows to individually configure the amplitude of the precursor, cursor and the three main postcursors through the digital registers. This functionality is included to allow to partially remove the Inter-Symbol Interference introduced by the transmission media when high speed signals are sent through it.

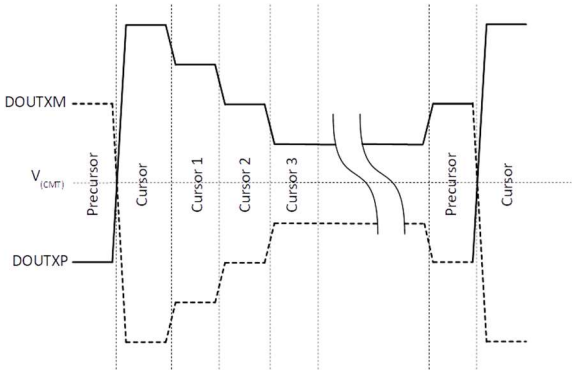

Figure 2. TX output cursor definition for pre-emphasis feature.

The output driver has 50-ohm output impedance which can be calibrated using the internal IP registers. This allows to compensate the impedance mismatch due to process variations avoiding line reflections. The output driver amplitude can also be controlled using internal registers.

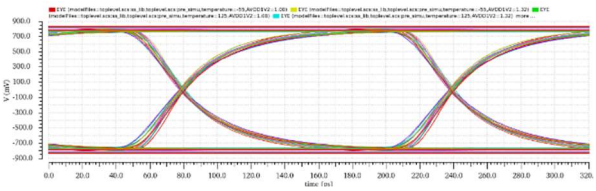

Figure 3. Eye Diagram simulations over PVT corners of the TX section, including noise.

IV. RX Section

At very high data rates, the transmission media low-pass behavior causes severe inter-symbol interference (ISI) in the signal that reaches the receiver. This problem worsens as the cable length increase or the cable quality decreases. This requires the use of several types of equalization in the receiver.

Due to the high speed of the incoming data, the receiver architecture is fully analog. All blocks in the receiver are designed as fully differential circuits. The first issue you need to deal with in the receiver is the amplitude of the input signal.

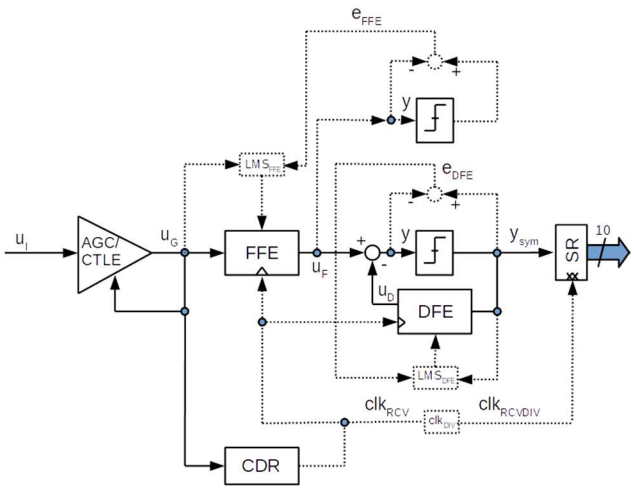

Figure 4. Receiver Block diagram.

Automatic Gain Control

The media attenuates the input signal as function of its length, so an amplifier/attenuator is needed to control the amplitude of the input signal and the signal to noise ratio (SNR). This function is performed by the Automatic Gain Control block (AGC), which senses the input amplitude and attenuates/amplifies the signal to keep a constant signal at the input of the remaining blocks of the receiver. The AGC can modify the signal amplitude between +12dB down to -10dB. The output amplitude of the AGC can be configured by internal registers.

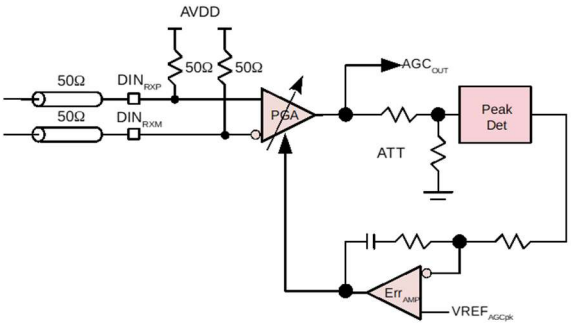

Figure 5. AGC block diagram.

Continuous Time Linear Equalizer

The output of the AGC is amplitude controlled but it contains a large amount of ISI distortion. In order to correctly sample the input data and convert into digital signals, a clock must be generated from the input signal using a Clock and Data Recovery Circuit (CDR). This process is not possible before the ISI is reduced down to a certain level to allow the CDR to properly recover the clock. To perform this operation a programmable high pass filter is introduced at output of the AGC, named Continuous Time Linear Equalizer (CTLE). This circuit can be tuned using the internal registers, generating different amount of high frequency boosting.

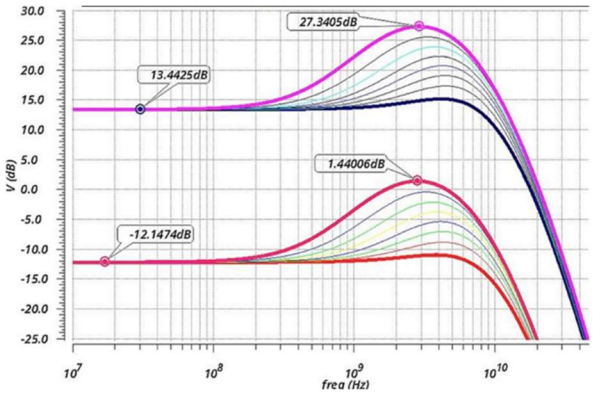

Figure 6. Combined CTLE + AGC frequency response simulation over the AGC range in nominal condition. The -3dB point is set at 10GHz for all cases.

Clock and Data Recovery

A modified version of an analog PLL is used for this task. A PLL with a modified phase detector able to deal with random signals is capable of recovering a phase synchronized clock. The phase detector (PD) used in our case is an Aleksander phase detector, which only delivers the sign of the phase not providing information of the magnitude of the phase itself. This has the advantage over the linear PDs that always provides the right phase information even for slow rise/fall times or if the frequency difference between data/clock is very small.

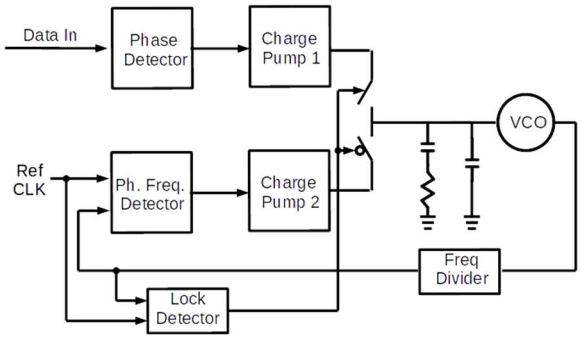

Figure 7. CDR Block Diagram.

The phase detector has the limitation that does not sense the clock/data frequency, which can lead to a situation where the CDR could lock at a harmonic frequency of the fundamental one.

To avoid this potential problem, a second feedback loop is used, which uses a reference clock (see Figure

7) of similar frequency of the incoming data. In this case a phase-frequency is used, allowing to the CDR to lock into a frequency which is very similar to data frequency. Once in frequency lock, the system switches to the random data input, allowing to the CDR to place the recovered clock edge in the data center.

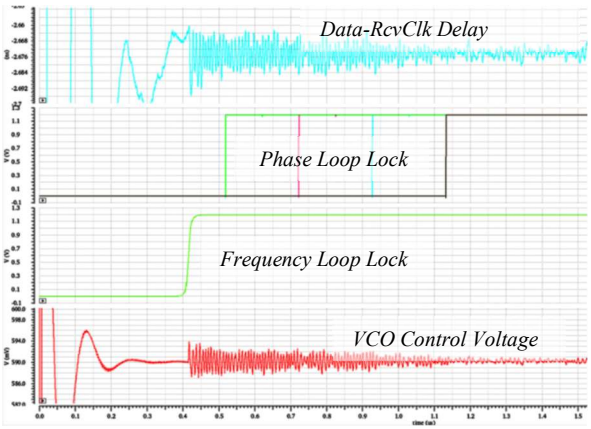

Figure 9. CDR Locking process simulation at nominal conditions and 6.25 Gbps.

Discrete Time Adaptive Equalizers

Once the input signal is amplified and ISI is partially reduced by the CTLE, the remaining ISI needs to be removed to achieve the desired Signal to Noise Ratio (SNR). The system is designed for a 19.5dB of SNR which is equivalent to a Bit Error Rate of 10^{-12}.

To do that a 5-taps discrete-time Feed Foward Equalizer (FFE) in combination with a 3-tap discrete-time Decision Feedback Equalizer (DFE) is used. The combination of FFE+DFE is ideal, because the FFE removes most of the ISI of the signal, but it is sensitive to noise and crosstalk, while DFE removes the remaining ISI. The DFE works with the sliced signal which makes it insensitive to noise, but it is prone to instabilities due to the feedback path. The FFE and DFE are analog versions of a Finite Impulse Response filter (FIR), which uses an expression as:

$$\frac{y[z]}{x[z]} = a_0 + a_1 z^{-1} + a_2 z^{-2} + \ldots + a_n z^{-n}$$

The coefficients need to be such, that the combination of FFE and DFE gives approximately the inverse transfer function of the transmission channel.

In case of the FFE, it samples analog signals using a Sample and Hold (S&H) circuit, based in coefficient shuffling scheme to implement the FIR analog filter. This is implementation it has advantages in terms of signal integrity and speed. The DFE uses an implementation similar to a shift register, using radiation hardened high speed flip-flops, where each sample is amplified and added together to generate the adequate FIR equation.

To update the equalizers coefficients, the Least Mean Square (LMS) algorithm is used. A simplified version of this algorithm, the sign-sign LMS is used to reduce complexity. As shown in Figure 4, two different LMS blocks has been implemented, one for the FFE and another for the DFE equalizers. To avoid interaction between the adaptation process of the two

Figure 8. Analog FIR implementation with coefficient shuffling.

equalizers and improve convergency, two different error signals are generated e_{FFE} and e_{DFE}, using a secondary slicer outside of the signal path.

The equalized output y_{sym} is then parallelized using a high-speed shift register (SR) and transferred to the digital section using divided clock to perform the 10b/8b if needed.

V. Additional Features

The system also includes different features like multi-channel configuration, and Built-In-Self-Test features, analog far-end, analog near-end, RX-end and digital loopbacks. It also provides PRBS sequence generation and checking.

VI. Simulated Results

Extensive schematic verification has been performed, over process, supply, and temperature variations. The simulations have been performed with different cable models (AXOMACH up to 4m), backplanes (STRADA WHISPER, MEGTRON6 up to 1m) with attenuations in excess of 20dB at maximum data rate.

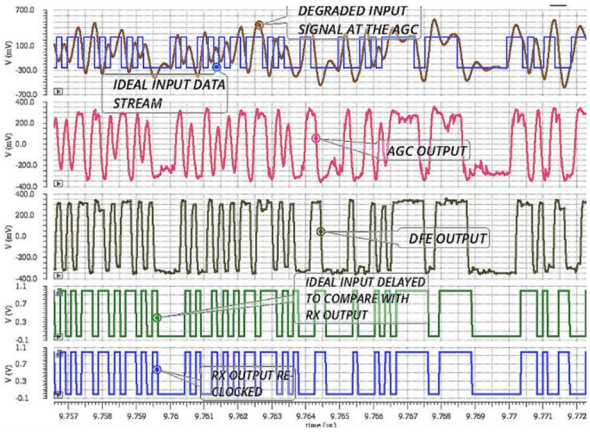

Figure 10. Receiver simulation at different receiver points for -20dB cable attenuation with inductive parasitic peaking (nominal conditions).

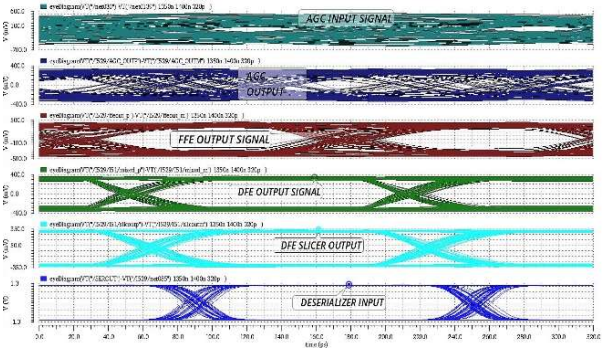

Figure 11. Eye diagrams at different receiver points for -20dB cable attenuation with inductive parasitic peaking (nominal conditions).

Simulations show how the eye diagram opens after the equalization is performed. Most of the SNR improvement is provided by the FFE equalizer, while the DFE adds some extra SNR to the system that the FFE is not able to provide (Figure 12).

The system has also showed that the SNR is well above the 19.5dB required, for the tested transmission media, which is the requirement to achieve a BER of at least 10^{-12}. A SNR of 21dB can be achieved at the FFE output, which improves up to 33.5dB at the DFE output in nominal conditions, with a media with 20dB attenuation at 3.125GHz.

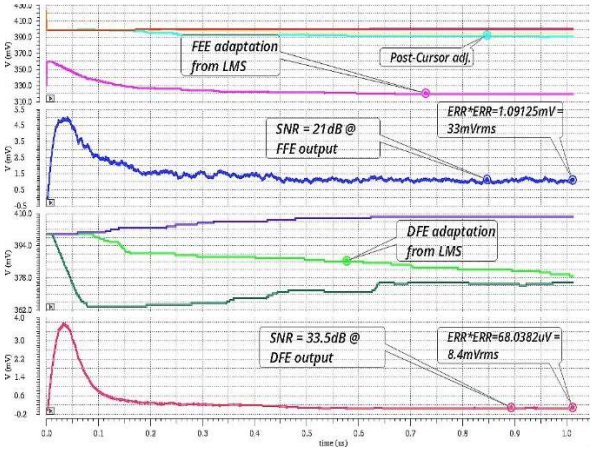

Figure 12. Equalizer convergence process in nominal conditions. FFE coefs., FFE error signal, DFE coefs, and DFE error signal is shown, using a 20dB media attenuation with inductive parasitic peaking.

VII. References

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GSTP Program