Bringing Proven PoC to Space Grade Ka Band Capable Improved Sampler for Direct Microwave Sampling in Software Defined Radio Context

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***Abstract* —. Next generation communication standardization is calling for more flexibility with an access to higher carrier frequencies and wider instantaneous bandwidth. We have proposed to tackle these challenges by introducing a proof-of-concept system in package of a wideband data converter solution capable to directly access the microwave spectrum at Ka-band (40 GHz). This paper describes the efforts made to turn this proof of concept into a space grade MCM product.**

Details are given on the strategy to address potential clock phase shift issue due to SET in the track and hold silicon die and how the ADC silicon die has been made compliant with space environment. Methods to increase reliability of the organic package are discussed, and we show the influence on the 40GHz capable RF transition of the analog input of the MCM performance. Moreover, we explain the efforts made on the assembly of the component in order to manufacture a space qualified Q band capable ADC.

***Keywords* —Multi-chip assembly, Ka-band, track-and hold amplifier, ADC, sub-sampling, direct microwave sampling, software-defined radio, organic substrate, space grade.**

I. INTRODUCTION

Every one of us is conscious of the massive amount of digital content we are accessing in a day-to-day basis through our connected smart devices and associated applications. In the years to come, there is still a forecasted increase of the bandwidth demands especially for video content [1]. These data must be accessible everywhere and anytime.

In the context of space infrastructure, new requirements are emerging for the decade ahead, in terms of higher bandwidth, higher frequencies, more flexibility and software-defined satellite payloads [2], [3]. On the ground segment, a Software Defined Radio (SDR) approach has been proposed to simplify the ground station receiver architecture of Deep Space Antenna used by the European Space Agency in the X-band. The receiver is based on commercially available Track-and-Hold Amplifier (THA) and Analog-to-Digital Converter (ADC) [4]. THA has been considered as the bottleneck of high-speed ADCs and lots of effort have been done to put into tackling the challenges of high input bandwidth, high sampling rate while achieving low distortion [5]. The THA brings the necessary system flexibility and simplification with associated power and cost savings in an SDR context and can be used in various high demanding applications such as satellite, wireless, optical and wireline communications and test equipment.

In this paper we show how we are developing a space qualified ADC MCM (Multi Chip Module) product starting from a Proof-of-Concept (PoC) of a receiving device able to sample signals up to the beginning of the Q-band (40 GHz), briefly described in Section II, which is the next step of previous developments engaged by Teledyne e2v [6]. Section III will describe current development of the designed for space stand-alone ADC product derived from the PoC, discussing the silicon technology used for the THA and the ADC and detail of the methods used to make them robust to space environment, developments in the assembly process, as well as package design simulation results and comparison with PoC, before concluding remarks.

II. PROOF-OF-CONCEPT BRIEF DESCRIPTION

The PoC [6], code named EVP12PS640, is a System in Package (MCM) built around two main functions: a microwave sampler or THA providing an extended input bandwidth to the Analog-to-Digital Converters (ADCs) behind it. The microwave sampler is based on an original THA composed of a master THA (TH_M) followed by two time-interleaved slave THAs (TH_S1 & TH_S2) sampling the master THA output in ping pong. The analog signal coming out of the slave THAs and the clocks are then provided to each ADCs for sampling. The digitized data are finally sent out through high-speed serial lanes (HSLL) using the ESIstream license free protocol [7]. The synchronization of both ADC is realized thanks to a daisy chain scheme. The SYNC signal is acquired by ADC1 and propagated synchronously to ADC2.

The PoC is composed of three dies. Whereas the ADCs (Die #2 and Die #3) are off-the-shelf Teledyne e2v products (EV12AQ600 [8]), based on BiCMOS 130 nm from STMicroelectronics [9], the microwave sampler is at the heart of this PoC (Die #1). It is realized in BiCMOS 55 nm from STMicroelectronics [10] for enhanced RF performance (bandwidth, linearity, high sampling rate leveraging high Ft of SiGe HBTs), yet operating with a 3.3 V power supply. It should be stressed out that the BiCMOS silicon technology used in the THA and in the following ADCs of the PoC allows design of very high bandwidth front end RF circuitry at the cost of high power consumption and increased junction temperature (T_j) . Finally, the dies are flip-chip assembled on a single organic Flip-Chip Ball Grid Array (FCBGA) substrate, designed to ensure non limited RF performance [REF].

In order to ease the integration into the RF front-ends and clock, the PoC is 50Ω single-ended on both its microwave analog input and clock inputs, while the internal circuitry is fully differential. The single-ended to differential conversion is realized in the THA. Moreover, the THA embed DC Block circuitry on both analog input and clock input sparing customer need to implement highly optimized Ka-band capable DC block layout it on its board.

Detailed theory of operation as well as explanations of the substrate RF transition in the package are given in [6]. Fig. 1 shows analog input bandwidth and band-flatness in each band up to

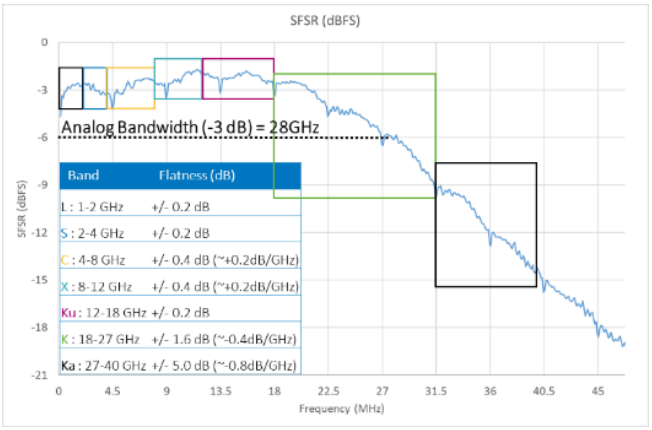

Fig. 1 Analog input bandwidth measurements from the PoC

Ka-band. Typical -3dB analog input bandwidth (BW_{-3dB}) is 28 GHz. The peaking behavior (due to internal gain) observed at 16GHz allows for a -0.5dB bandwidth of 24 GHz. Typical band flatness does not exceed +/-0.4 dB up to Ku band. Upper bands show a linear power decrease of -0.8 dB/GHz.

Table 1 shows typical performance at Fs = 11 GSps and for various frequencies in the bands of interest (Pout = -12 dBFS) with a comparison to recent State-of-the-Art in BiCMOS [12], [13]) and 16nm FinFET [14] technologies.

Table 1. Performance summary and recent State-of-the-Art

	Fin*/ Band	Fs**	BW*	SFDR[1]	THD[2]	SNR[3]	ENOB[4]
This work	8.45/X	11	28	58.1	-67.9	45.6	7.3
	11.72/Ku	11		57.4	-68.5	45.5	7.3
	17.50/Ka	11		50.0	-68.2	45.3	7.2
	32.05/Ka	11		51.2	-60.5	44.6	7.1
	34.45/Ka	11		47.2	-56.9	44.5	7.0
	40.25/Q	11		44.8	-54.2	44.0	6.9
[12]	34/Ka	10	65	45	-45	n.a.	7
[13]	30/Ka	32	58	32	-25	n.a.	7
[14]	8/X	18	18	54	n.a.	n.a.	n.a.

*: in GHz; **: in GSps; [1]: Spruious Free Dynamic Range (in dBc); [2]: Total Harmonic Distortion (in dBFS); [3]: Signal to Noise Ratio (in dBFS); [4]: Effective Number of Bits (in bitFS);

III. DESIGNED FOR SPACE MCM PRODUCT DEVELOPMENT

A. *Improvement of the THA from the PoC*

Good experimental results measured on the PoC paved the way to the development of the MCM product, which consisted in improving the THA and the design of a brand-new ADC, and to take into account the space environment constraints (especially SEU mitigation).

Since the THA die is used to divide and distribute the system clock to the ADC die, it is of paramount importance to address potential clock phase shift issue due to SET. Traditional mitigation technique based on low pass filter which is relevant for "slow" control signals or for bandgap stabilization was not applicable since we were addressing a very fast signal (clock frequency up to12.8 GHz). Therefore, we had to implement Triple Majority Voting (TMV) or Triple Modular Redundancy (TMR) in the clock divider. Based on DARE [15] simulation using current injection (simulating Heavy Ion Strike effect at different locations, with a LET of 60MeV.cm2/mg) on different critical nodes of the structure we compared both TMV and TMR triplication methods.

In each case, the weak point is the voter since events in the latches are addressed by the voter(s) and are harmless, but the triplication of the voter in the TMR structure allows for overcoming this limitation. If a voter is corrupted due to a HIS (Heavy Ion Strike), the fault is not propagated, and the phase is preserved within two of the redundant divider paths. When the voter recovers after the HIS, the phase is also restored in the associated divider path, therefore even if the divided clock is interrupted by a HIS on the output voter the phase of the divided clock is preserved (HIS on the divider latches or on the other voters will trigger neither divided clock interruption nor divided clock phase shift). This is proven by simulation results displayed in Fig. 2: top curves divider output with (red) and without (light blue) HIS, middle curves output of the second latches with HIS, and bottom curves are the output of the three voters with HIS.

In comparison the TMV structure always induces clock interruption in case of HIS on the voter with a 50% probability of divided clock phase shift. The TMR structure, shows a significant superiority in term of divided clock phase preservation over the TMV structure, therefore, despite a greater power dissipation and a larger footprint we have decided to implement the TMR structure.

B. *Design of the ADC*

The new dedicated ADC uses 28nm CMOS technology in order to dramatically decrease power consumption, while integrating digital signal processing features. This signal processing includes programmable DDC, programmable frequency hopping and beam forming capabilities, thus enabling in many use cases the reduction of used HSSL. The drastic power reduction allows for lowering junction temperature and relieving of thermal management at system level, which is often an issue for space applications.

To make the system robust to radiations, different techniques have been implemented. First, the critical signals have been identified: this mainly concerns clocks and synchronization. For these signals TMR is used all along the path. In some analog areas where the redundancy is not possible, the sensitive signals are propagated and processed using differential signal path, using buffers and gates with drive strengths strong enough to avoid edges or state changes. The drive strengths have also been improved using back-to-back driving buffers. Finally, the circuit has been verified with a specific tool injecting charges on all nodes connected to a diffusion (transistor drain or sources, diodes and BJTs) during a transient simulation. The simulation allows to confirm the strength of hardening solutions as seen in Fig. 3.

The non-critical signal nodes have also been verified to ensure safe operating areas in case of SET. When needed, the impedance was reduced by increasing the transistors width, or

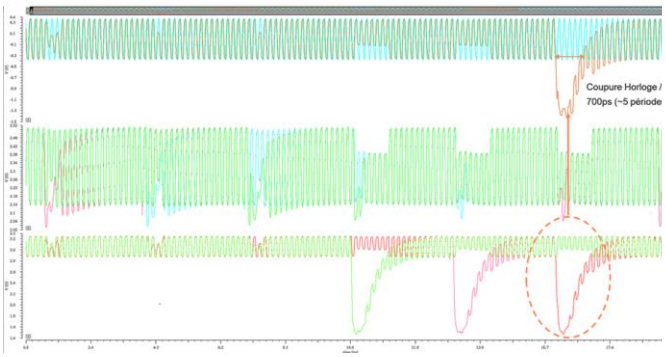

Fig. 2: DARE simulation results of the internal clock divider signal of the THA die using TMR showing divided clock output signal with injection (red) and without injection (blue) (top), internal signal (middle) and output of every voters (bottom)

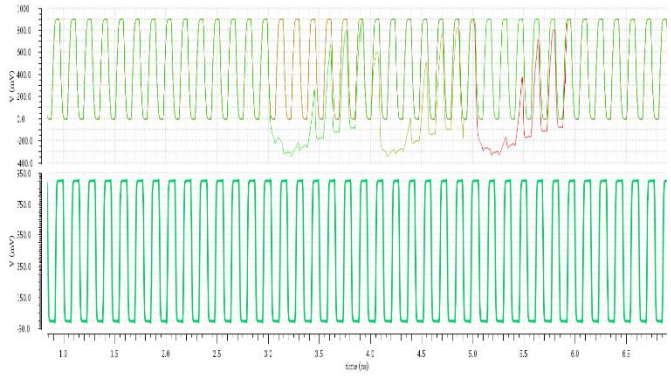

Fig. 3 : Results of transient simulations of SET events on radiation hardened sensitive s, showing ssuccessive injection on each of the 3 clocks of a TMR voter (top) and results of the voting (bottom)

a capacitance was added, to reduce voltages glitch due to the charge injection.

The static settings like trimming and enable signals are RC filtered to avoid state changes and unwanted power on/off in case of a radiation event.

From the layout point of view, all active devices are isolated in wells. Critical devices are individually surrounded by un-cut biasing rings and substrate taps are repeated frequently to avoid latch-ups. This also concerns digital functions: digital standard cells and P&R tools have been adapted to surround any group of gates with biasing rings.

C. Assembly for space

From the assembly point of view, efforts have been made to make the complete package compatible with space industry requirements. It is well known that solder resist is banished from space-oriented board due to strong outgassing [16]. For reliability purpose we used soldemask defined solder joints for the flip chip assembled dies. Consequently, we tried an organic substrate with a solder resist known for its very low outgassing performance. Confirmation by analysis of outgassing has been performed through measurements of TML (Total Mass Loss), CVCM (Collected Volatile Condensable Materials), RML (Recorded Mass Loss) and WVR (Water Vapour Regained) according to ECSS and NASA standards [17] and [18]. The analysis results are within standard requirements.

All the assembly materials used in the MCM product such as Thermal Interface Material (TIM), underfill and lid attach material are specifically chosen to be low outgassing materials. TIM and underfill are also specifically chosen to be compatible with the two silicon die technologies used in the MCM product in term of different wafer fab, bumping process, silicon surface finishing while also being compatible with the solder resist of the substrate or back side of the silicon dies [19], [20]. Moreover, the assembly materials have been carefully chosen for their mechanical properties in order to not create mechanical stress around the silicon die or to absorb mechanical deformation of the substrate when exposed to temperature cycling. We used the PoC as a test vehicle to perform manufacturing evaluations and warpage measurements at different temperatures using shadow moiré method [21], in order to check for unusual deformations.

D. Package Design

The MCM product is composed of a THA silicon die and from a single ADC silicon die. The substrate is 16.0x17.6mm organic substrate (FCBGA) with 0.8mm pitch SAC305 RoHS solder ball with a nickel-plated copper lid. Fig. 4 shows packages of the PoC and MCM for comparison.

The main improvement of the MCM product package from the PoC relies on efforts to make it as reliable as possible to sustain space qualification. Organic substrate reliability main limitation, compared to ceramic substrates traditionally used in the space industry, is that stacking of laser etched microvias can easily lead to microcracks at the interface of the bottom of the microvia and the copper layer of the build-up, mostly due to brittle interface caused by impurities after the laser etching of the build-up resin [22]. Moreover, stacking of a microvia over a plated through hole via across the core layer can also lead to reliability concerns [23]. To cope with this potential weakness, the layout of the substrate of the MCM product uses very conservative design rules which surprisingly do not degrade performances of the many RF transition of the packages (analog input, input clock, HSLL, syncs). As an instance, Fig. 5 compares the analog input performance of the PoC [6] using relaxed design rules and that of the MCM product, in the same conditions, which clearly shows comparable performances.

Another potential reliability issue from organic substrate, compared to ceramic substrate, is board level reliability (BLR). Organic substrates allow for wider dimensions and ball count than ceramic substrates, thanks to better match of the CTE of the materials between the substrate and the board. However, lower young modulus in the organic substrate leads to decreased performance in BLR for the balls under the silicon die, also called flip chip shadow. The strong CTE mismatch between the silicon die and the substrate leads to strong mechanical stress under the silicon die which reduces lifetime expectancy of the balls in the flip chip shadow. In order to make it more reliable, silicon dies of both the THA and the ADC are thinned in order to decrease mechanical stress in the flip chip shadow and improve BLR results. The downside of a thinner die is that it could lead to higher junction temperature. The die thickness is chosen thick enough so that it does not increase the MCM maximal junction temperature, or hotspot, by more than 1°C.

As mentioned before, 28nm technology used in the ADC of this MCM inherently leads to lower power consumption and lower

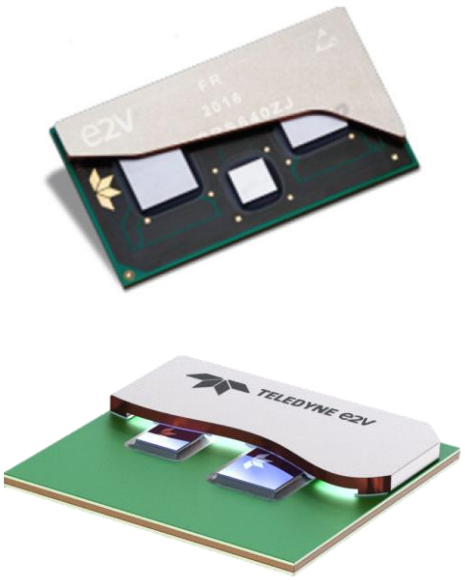

Fig. 4: photograph of the PoC package (lid cut) with the two ADCs and the THA silicon dies (top); MCM product computer generated imagery of the package (lid cut) with the ADC and the THA silicon dies (bottom)

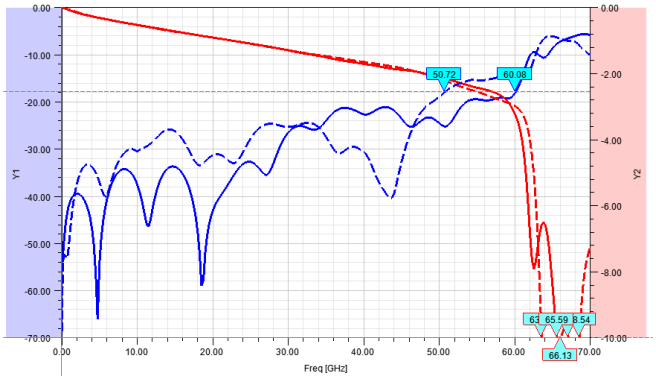

Fig. 5: Simulation results comparing S_{11} (blue line, left scale) and S_{21} (red line, right scale) versus frequency of the analog input RF transition for the PoC (dashed line) and for the MCM product (continuous line). This figure clearly shows that using strict design rules to increase the organic substrate reliability do not decrease RF performance

T_j . Fig. 6 shows thermal simulations of the MCM product at 80°C ambient temperature with heat removal at the top surface of the lid, where hotspots are clearly visible. The hotspot of the THA is 98.4°C and the hotspot of the ADC is 90.7°C. For comparison, with the same boundary conditions, the hotspot of the THA is 102.5°C and the hotspot of the ADCs is 103.3°C [6], which are significantly higher.

IV. Conclusion

A Ka-band capable direct sampler MCM product has been designed based on a PoC which achieves high performances with SFDR better than 50 dBc for input frequency range up to 34 GHz, a THD below -54 dBFS up to 40 GHz, and SNR better than 44 dBFS up to 40 GHz, resulting in an ENOB around 7 bitFS up to 40 GHz [6].

The MCM product uses a THA fabricated in BiCMOS 55nm technology from STMicroelectronics and an ADC in 28nm CMOS technology flip-chip assembled on an organic substrate. We detailed methods applied to make the silicon circuitry robust to space environment. We also explained how we developed assembly process to be compliant with space requirements as well as careful package design to improve reliability of the MCM showing little degradation of the RF performance.

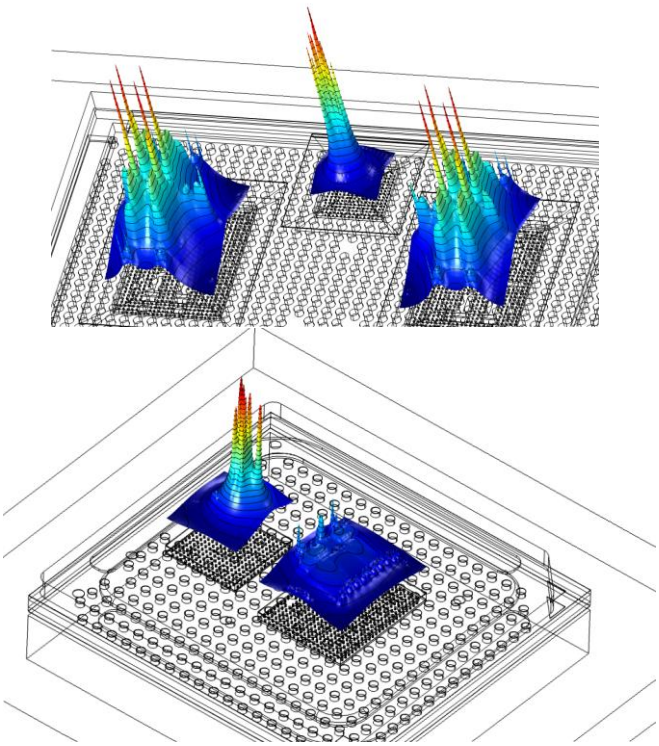

Fig. 6: Thermal simulation results of the PoC [6] (top) and of the MCM product (bottom) showing hotspots. Hotspots are significantly lower in the MCM product ADC thanks to 28nm CMOS technology benefits.

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