Radiation Hardened Versatile 14-BIT SAR ADC

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***Abstract*—This ADC has been designed to improve a Silicon proven single ended rad-hard 10 bit SAR ADC. It includes an 8:2 analog MUX combined with an auto-zero amplifier (0dB, 6dB and 12dB) and an internal voltage reference, which can be bypassed. The core ADC can be used in single-ended or differential mode and is able to sample at a rate up to 500kS/s in 11 bit mode. This mode can be extended to 14 bit (maximum sampling rate 200kS/s) with optional dithering capability.**

I. Introduction

The original design of this ADC is the first version of the DARE180U_ADC library: a single ended 10 bit SAR ADC with a single capacitor matrix (no bridge capacitor). Such ADC architecture (single DAC) is only suitable for low to medium resolution ADC as it needs 2^N unit capacitors (where N is the number of bits). A first improvement for this ADC has been to reduce the unit cap by a factor 2 and by doubling the number of unit capacitors to reach 11 bits resolution. Using MiM capacitors for the DAC matrix it was not possible to extend the resolution further: the unit capacitor was already its minimal size (a total sampling capacitor of 25pF). Finally, the capacitor bank has been duplicated to offer the differential capabilities for this ADC.

Later this ADC has been completed by an 8:2 analog input mux. This MUX offers the possibility to connect 1 of the 4 input pairs to the input of the ADC (differential mode) or 1 of the 8 inputs to the input of the ADC (single ended mode). The connection to the ADC can be a direct connection through a switch or buffered with the possibility to amplify the signal by 0dB, 6dB or 12dB.

As the 2 sampling capacitors are of 25pF, the intrinsic accuracy of this ADC is much more than 11 bit:

- Sampling noise (kT/C) is low enough for a 16 bits ADC
- DNL at mid code corresponds to a 14 bits ADC

Considering these two points it has been decided to increase the resolution of this ADC by 3 bits without any modification of the 11 bits ADC core design which is silicon proven and by adding the possibility of dithering.

II. 2:8 Analog Mux

The analog MUX has the possibility to select 1 or 2 of its inputs and to connect them to the ADC input. This connection can be realized by essentially 2 ways:

- Direct connection between the MUX input(s) and the ADC input(s) through switch(es) (e.g., switch 7 and 8 in Figure 2).
- Buffer/amplification thanks to a programable gain amplifier (PGA):
  - 0 dB, Zin > 60 kOhm
  - 6 dB, Zin > 40 kOhm
  - 12 dB, Zin > 24 kOhm

The programmability through the switch arrangement shown in Figure 2 has several advantages:

- No switch at the input of the resistor network => no distortion or gain error when the MUX is configured in buffer/amplifier mode.

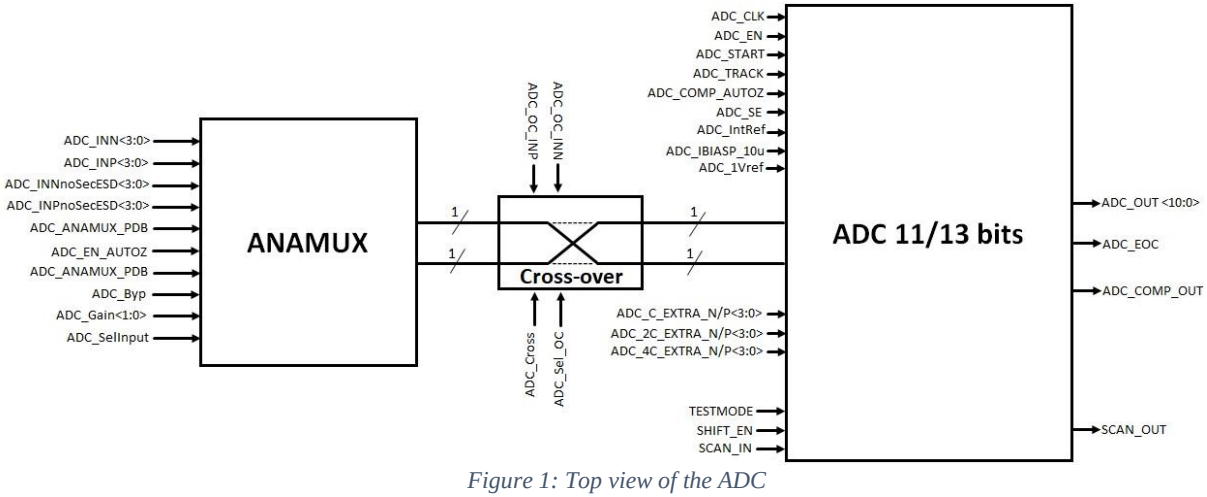

Figure 1: Top view of the ADC

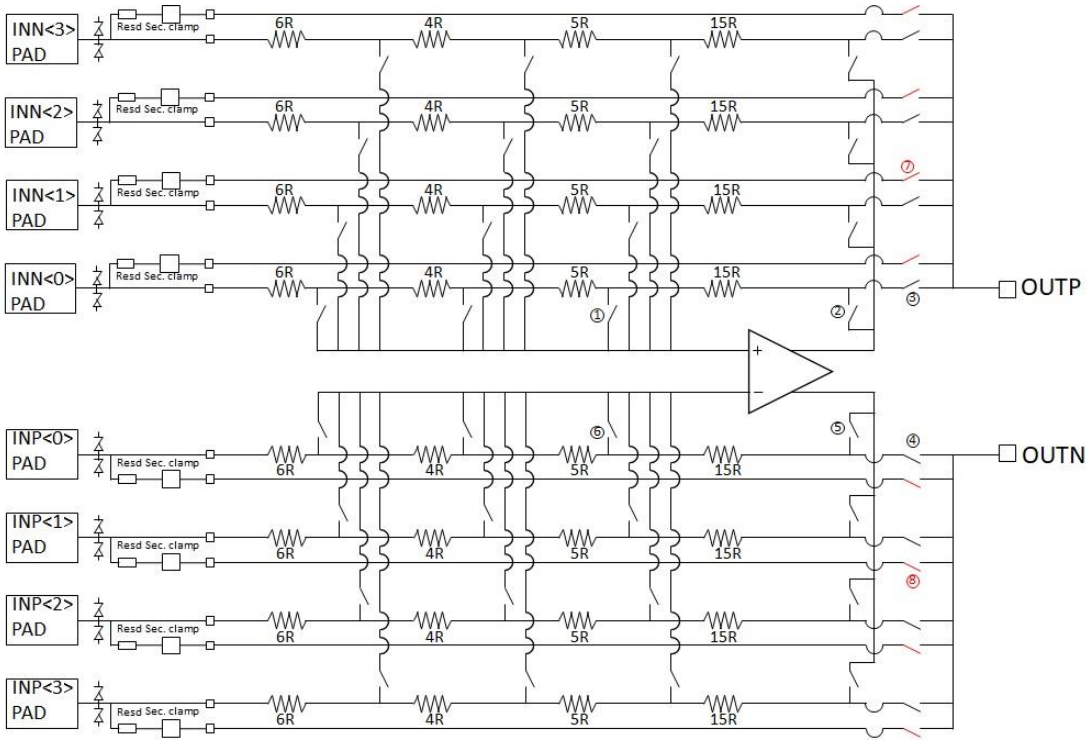

Figure 2: Schematic diagram of input analog MUX block

- The switches 1, 3, 4 and 6 don't introduce distortion or gain error as there is no current flowing through them.
- The switches 2 and 5 have current flowing but are not in the ADC signal path. It causes no distortion due to these switches.
- All these switches can be relatively small size (i.e., reducing the cross section) because they don't introduce any distortion or gain error. The size of these switches is driven by only settling time consideration.
- Thanks to the relatively high input resistance value (minimum 24 kOhm before the switches connected to the amplifier inputs on Figure 2), the secondary ESD protection is not needed in amplifier mode. In amplifier mode the gain is only a function of the feedback resistor ratio.

III. ADC Core

A. Overview

An overview of the ADC block diagram is shown in Figure 3. It is composed of:

- An autozeroed hardened comparator.
- 2048-unit capacitors in the two main DACs (DAC+ and DAC-), implemented by common centroid layout.
- Two sub-DACs (Extra DAC+ and Extra DAC-) offering the possibility to extend the resolution of 3 bits and to dither the ADC transfer function.

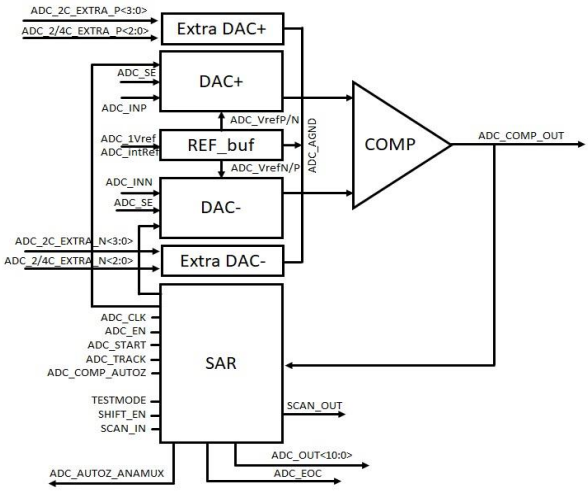

Figure 3: Block diagram of ADC Core

- A fully radiation-hardened (SET, SEU and SEL) state machine for the SAR.

B. Extension of the DAC capabilities

The original DACs (DAC+/- in Figure 3) have each a capacitor bank of 2048-unit capacitors. As this part is silicon proven the second sub-DAC (Extra DAC+/-) has been added in parallel so that the original 11 bit mode is not affected by

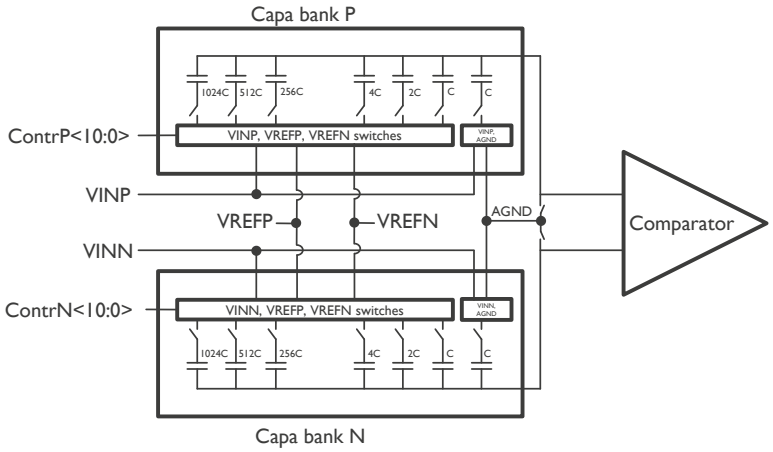

Figure 4: Original 11 bit DAC for ADC

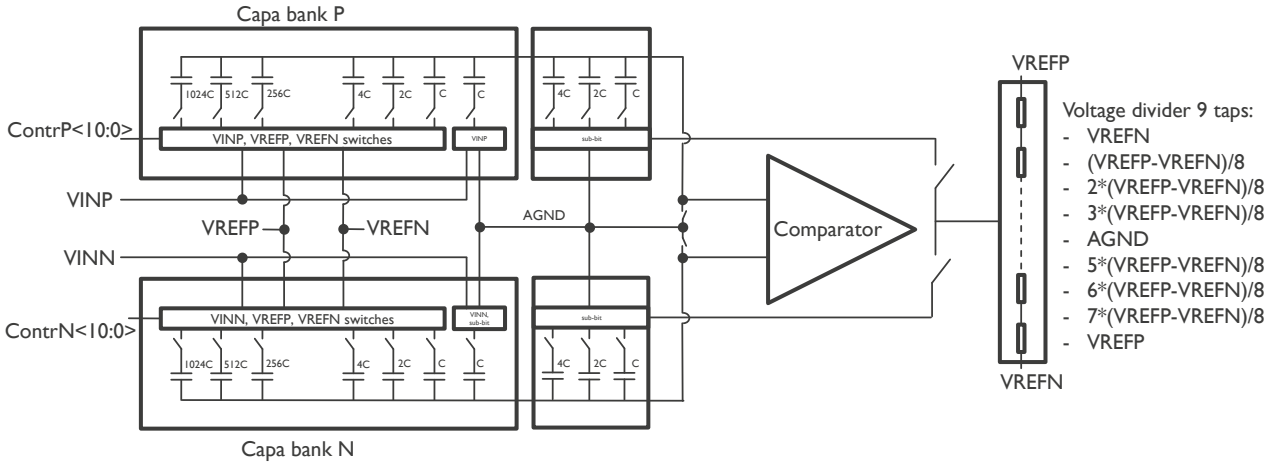

Figure 5: Improved 14 bit DAC for ADC DAC

this modification. Figure 4 and Figure 5 show how this ADC has been practically improved without any risk to degrade the original ADC (11 bit): in 11 bit mode the bottom plates of the capacitors of the extra DAC are shorted to the mid-reference (VREFP-VREFN)/2.

To add these 3 extra bits resolution there were essentially 2 ways to avoid any modification of the original ADC:

- Use the extra DAC capacitors of respectively 12.5fF/2 12.5fF/4 and 12.5fF/8
- Use 1 capacitor of 12.5fF and a sub-set of the reference voltage

These 2 possible implementations are equivalent from a charge sharing point of view but only the second is realistic. Indeed, the first solution needs to connect 8 capacitors in series to accurately divide the capacitor by 8. Such implementation is not suitable due to the nonuniformity of the charge injected during the reset of each serial element.

The sub-references have been designed with a simple resistive divider. Thanks to low capacitive load (order of 100fF) and to the relatively low clock frequency (10 MHz) it is unnecessary to have a low impedance sub-reference generator. Practically we have 8 resistors, which are about 4 kOhms leading to “leakage” of about 100uA.

The extra DAC is composed of 1 bank of 3 capacitors corresponding to x1, x2 and x4 unit capacitor (unit capacitor used in the main DAC). The 2 last extra capacitors of this bank (x2 and x4 unit capacitor) can be used for optional dithering. The following example illustrates how.

- Input signal is sampled with the bottom plate of all the capacitors connected to the mid-range reference.
- First conversion where the 2 extra capacitors stay connected to the mid-reference
- Second conversion (with the same sampled value => no extra sampling) where the 2 extra capacitors are connected to VREFP. This conversion will extract a code corresponding the sampled input signal plus 6*(VREFP-VREFN)/2048
- Third conversion (on the same sampled value => no extra sampling) where the 2 extra capacitors are connected to VREFN. This conversion will extract a code corresponding the sampled input signal minus 6*(VREFP-VREFN)/2048
- Use the averaged value of the 3 conversions for the output code

IV. Conclusion

We have improved a 11 bits ADC design, which is silicon proven, to achieve 14 bit ADC. In the risk management point of view, avoiding modification of the 11 bits ADC design was our main constrain. For this, we added extra blocks such as the amplification, internal voltage reference additional 3 bits, and dithering on the outside of the original ADC. This ADC can work in 11 bits or 14 bits ADC mode by selection of configuration bits. Our design strategy succeeded to suppress the power and area overhead of the extra blocks and it results $1mm^2$ of silicon area and 8mA of current consumption (including analog MUX and internal voltage reference).

References

[1] L. Berti, W. Sijbers, G. Pollissard, J. Ngole, J. Wouters, G. Franciscatto, S. Verhaegen, S. Zagrocky, B. Blockx, K. Vanhoutte, Geert Thys, “DARE180U New Analog IPs”, AMICSA 2018

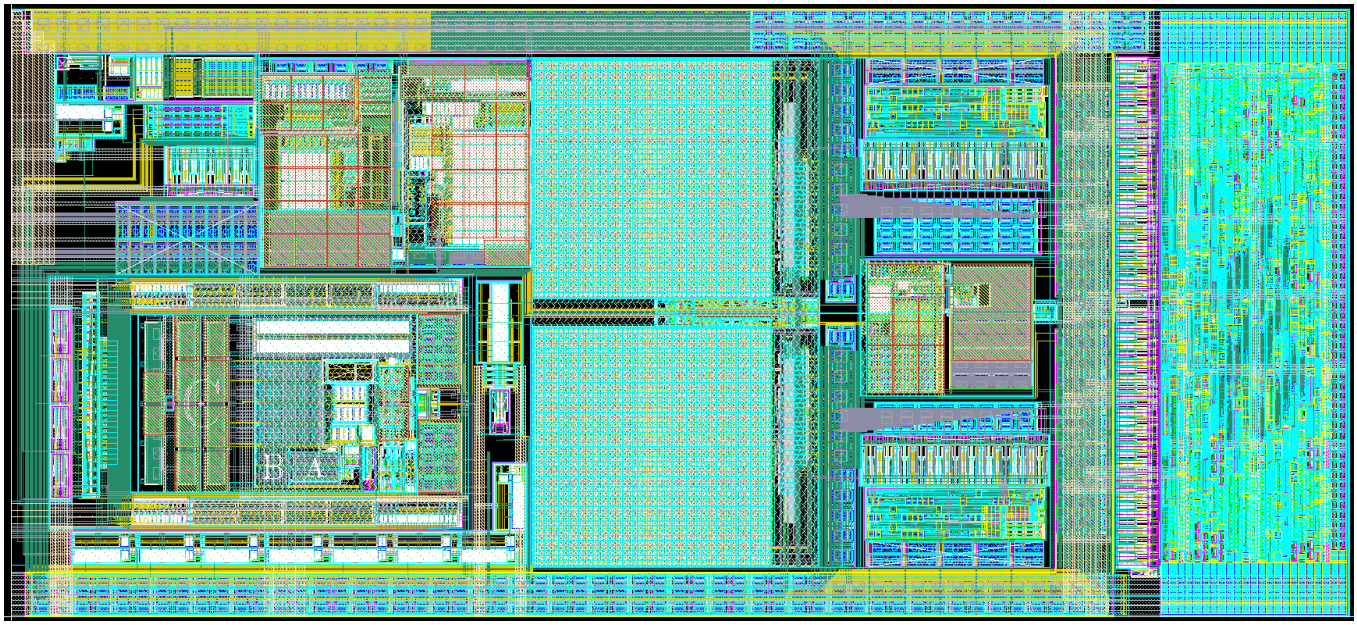

Figure 6:ADC top level layout