DARE22 Test Vehicle Design for a 22nm FDSOI Process

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***Abstract*—This paper presents the test vehicle (TV) design of the rad-hard library developed at IMEC, referenced with the acronym DARE22G, that reflects the "Design Against Radiation Effects in 22nm". Thanks to this test vehicle, the functional validation, the electrical performance, and the radiation hardening and sensitivity (SEE and TID effects) of the DARE22G library and a commercial DPRAM will be performed.**

***Keyword-lines*— Test vehicle, Hardened-By-Design, Single event effect detection, radiation effects.**

I. INTRODUCTION

Test vehicles are mostly developed to validate the new designs. Moreover, it allows to get information on how these designs are going to behave under the harsh environments such as radiation and temperature effects [1]-[3] , or even under the ESD stress.

In order to validate the DARE22G library, a test vehicle has been developed. It includes a; 1) digital core cells, mainly 228 combinatorial logic cells, 48 clock gating, 5 radiation-hard (DICE) and 12 standards sequential flipflops. 2) IO cells, including bidirectional digital IOs, and LVDS. 3) a TID sensor with an adaptive back-bias generator, 4) voltage and current references, 5) a 3GHz ultra-low jitter Phase-Locked Loop. 6) 1 GHz ring oscillators. 7) a commercial DPRAM [4]. 8) a radiation-hard digital interface using SPI (Serial Peripheral Interface) controller and control/monitor registers have been integrated to this TV, used to control the testing of all the previous blocks.

The following paragraphs shows the different tested structures, and how the SEE detections have been implemented for the different IPs present in this TV.

II. DIGITAL CORE CELLS

A. Combinatorial logic cells

More than 998 combinatorial cells are present in the DARE22G library. However, due to the area limitation of the TV, only 228 relevant cells have been selected, including inverters (CLKINV), NAND, NOR EXNOR, Triple majority voting (TMV), SET filter up to 60 MeV.cm2/mg (FILT60M). For instance, the SET sensitivity of an AND/OR/MUX or a buffer cell can be concluded from the inverter, which is always present as an output stage of these cells. The selected cells have been chosen with different drive strength, and inputs numbers (2 or 3) from the 12 available flavors of the threshold voltage and the gate lengths.

The sensitive area (SA) has been calculated to reach at least 100 events during 500s per ion with the SEE testing. To achieve such SA, multiple instances of these digital core cells are need. Several victim (DUT) cells are put in series (realizing a chain), in such a way that SET pulses generated in the chain (i.e. in the cells) do propagate to the end.
Several constraints limit the chain length:

- propagation delay to be 25 ns maximum, corresponding to an ASIC's 40 MHz minimum clock frequency
- pulse broadening: assuming a broadening in this technology of 1 ps up to 5 ps per gate, it is concluded that the chain length must be limited to 24 cells. A SET in the beginning of the first gate, can be extended of 120 ps. Therefore, a calibration of this broadening effect will be done before the SET irradiation tests.
- pulse quenching: concerns in general narrow pulse. Limiting the chain length to 24, allows to detect weak SET that can propagate through max 24 gates cells. Weaker SET that vanishes after a limited number of gates cells is ignored in our test-chip. Such kind of weak SET is indeed not critical as it disappear without a relevant impact on a digital system which includes in general more than 24 gates cells.

As much more than 24 cells are needed to reach the SA targeted, many copies of these chains are used and are put in parallel, a "merging tree" then channels events at the outputs of these chains into one node (making data handling more manageable). This "merging tree" is called Combiner.

Events at the output of the merging tree are latched, making them "permanent", which greatly eases their final read out of the chip. The architecture implemented is shown in *Figure 1*.

To determine the duration of the detected SET, a pulse filtering function is made thanks to C-Cell and different delays from 10 ps to 1 ns, with a step of 10ps for the range [10ps – 200ps]. A step of 20ps for the range [220ps – 400ps], and 50ps for the range [450ps – 1ns]. These kind of "XOR" cells are followed by RS latches (Figure 1).

To optimize the number of output signals per DUT from 40 to 6 outputs only, a thermometer-to-binary decoder is used. In fact, if the output of one RS latch RSn is triggered, all the previous latches (RSn-1 to RS0) latches related to lower delays will be as well. Therefore, a thermometer-to-bin decoder can be used.

Moreover, to distinguish between SET events from the DUT and the test structure (Combiner, C-Cell, delays, RS latch and decoder), the outputs of the chains are driving a redundant copy of Combiner and latches. Any event from the DUT will be detected in both test structures.

To perform a defect test on the combiner and the victim chains, a SET free NAND gates are put in the beginning of every victim chain. The purpose of adding these NAND gates, it's to filter (during radiation tests) any SET coming from the scan-chain structures used for the defect tests. Thanks to the NAND, only SET generated in the chains or in the combiner will be detected.

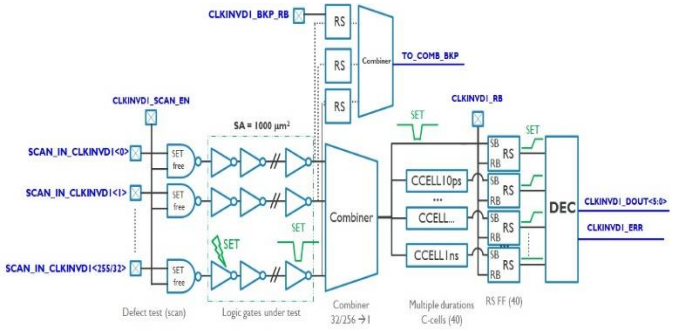

Figure 1 Logic combinatorial test structures (example for CLKINVD1) - principle diagram

The distortion of the combiners and the test structure can be calibrated using a Pulse generator as shown in Figure 2. A pulse of a width of 50, 100, 200 and 300 ps can be generated by the Pulse generator block.

Moreover, ring oscillators with a period of minimum 40 ns to reduce the pulse broadening effects, are used to calibrate the 50, 100, 200 and 300 ps delays used.

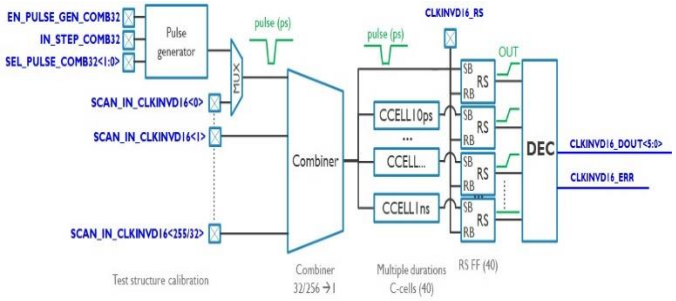

Figure 2 Distortion calibration of the Combiner and the test structure of the logic combinatorial cells- principle diagram

As shown in the calculation below, to reach a probability of double hits in such test structure lower than 5%, based on the flux available at RADEF radiation facility [5] and considering a radiation time of 500 s per ion, the maximum time between two reads (before resetting the latches) is 5ms.

With à fluence = flux . MT = 10^7 ions/cm^2, and a number of events = 100 (to have statistically relevant data)

SA = # events / fluence = 1000 µm^2

In fact, on average, there is one event every 5 seconds. To get enough hits to the target victim device, the cross-section (total drain/source area) needs to be large enough. In this design, the hit probability needs to be at least 1 hit/5s (100 hits/500s). Then the sensitive area for each type of device needs to be:

$$A_{cs} = \frac{1\ \text{hit/5s}}{500k\ \#/cm\text{^}2/s} = 1000\ \mu m^2$$

Besides enough sensitive area, double hits measurement needs also to be avoided. The measurement data is read every 5 ms (200 Hz) to avoid double hits. The probability of double hits in 5 ms can be calculated by Poisson distribution (λ=1/5(hit/s)*5 ms, k=2). λ= is the hit rate over 5 ms.

$$P(k=2,5ms) = \frac{\lambda^k e^{-\lambda}}{k!} = 4.995 \times 10^{-7}$$

$$P(k=1,5ms) = \frac{\lambda^k e^{-\lambda}}{k!} = 9.990 \times 10^{-4}$$

From the result, double hits probability is very low, so the situation that more than 2 hits in 5ms can be ignored. Then there are only three situations: zero, single hit and double hits. If the experiment time is 500 s, so the probability of double hit is:

$$P(k=2,500s) = 1 - [1 - P(k=2,5ms)]^{500/0.005} = 4.872\%$$

The zero hit in 500 s is then:

$$P(k=0,500s) = [1 - P(k=2,5ms) - P(k=1,5ms)]^{500/0.005} = 3.72 \times 10^{-44}$$

In conclusion, every victim device needs to achieve $1000\ \mu m^2$ sensitive area and the measurement period needs to be 5ms.

The detecting FF need be reset say every 5 ms (the probability to have two or more events within 5 ms is sufficiently small; second and further events would indeed go undetected)

The eventual SEL events of the logic combinatorial cells, as for the rest of the blocks of this TV, will be detected by monitoring carefully the power supply of the eight different logic gates (following table).

Logic Gate in the TV	Description
CLKINVD1/4/8/16_SLVT/ RVT/LVT/HVT20/24/28N	CLKINV, drive strength 1/4/8/16, 20/24/28nm length, SLVT/HVT/LVT/RVT flavors
EXNOR2D1_SLVT/RVT/L VT/HVT20/24/28N	CLKINV, drive strength 1, 20/24/28nm length, SLVT/RVT/LVT/HVT flavors
NAND2D1/2/4_SLVT/RVT /LVT/HVT20/24/28N	Two inputs NAND, drive strength 1/2/4, 20/24/28nm length, SLVT/RVT/LVT/HVT flavors
NAND3D1/2/4_SLVT/RVT /LVT/HVT20/24/28N	Three inputs NAND, drive strength 1/2/4, 20/24/28nm length, SLVT/RVT/LVT/HVT flavors
NOR2D1/2/4_SLVT/RVT/ LVT/HVT20/24/28N	Two inputs NOR, drive strength 1/2/4, 20/24/28nm length, flavors SLVT/RVT/LVT/HVT flavors
NOR3D1/2/4_SLVT/RVT/ LVT/HVT20/24/28N	Three inputs NOR, drive strength 1/2/4, 20/24/28nm length, SLVT/RVT/LVT/HVT flavors
FILTER60M_SLVT/RVT/L VT/HVT20/24/28N	60 MeV SET FILTER, 20/24/28nm length, SLVT/RVT/LVT/HVT flavors
TMV_SLVT/RVT/LVT/HV T20/24/28N	Triple majority voter, 20/24/28nm length, SLVT/RVT/LVT/HVT flavors

B. *Integrated Clock gating cells (ICG)*

The developed clock gating cells consists of a NOR gate followed by a latch, a NAND gate and a CCELL (Figure 3). It is a mix of combinatorial and sequential blocks.

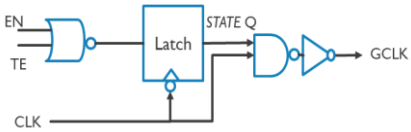

Figure 3 Integrated Clock Gating cell - simplified structure

Combinatorial blocks are susceptible to SETs and the sequential block is susceptible to SEU when there are double hits (DICE structure) and to SET. Hence both SET and SEU must be tested. Due to area limitation, three rad-hard (up to 25, 40, 60 MeV.cm2/mg) and one standard ICG has been selected, for each of the 12 available flavors.

The test structure proposed consists of a chain of ICG cells as shown in Figure 4. All outputs of the ICG cell in the chain are individually connected to a combiner. For instance, the total number of the cells to achieve enough sensitive area (SA) in the standard ICG chain is 384. Therefore three of 128-1 combiner are used to connect the output of each of these ICG cells.

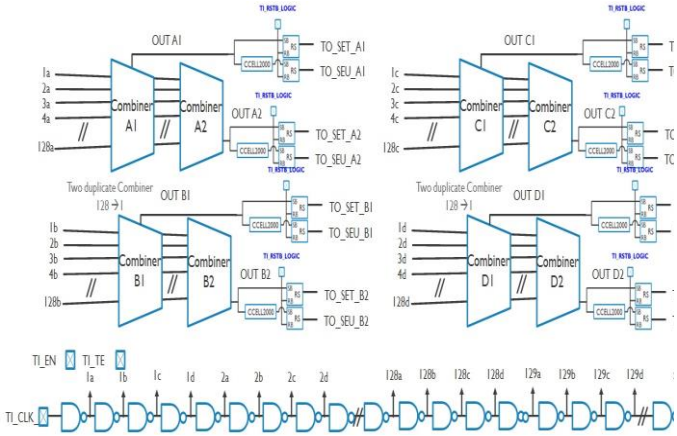

Figure 4 ICG test structure - principle diagram

To see if SETs generated in the ICG are propagating, the 384 ICG chain constructed using 4 series ICG cell (a,b,c,d) as shown in figure above. Each output of the (a,b,c,d) are connected to separate combiners and this is repeated 128 times.

If only one combiner (for instance A1/A2) detect a SET, but not detected by the next combiner (for instance B1/B2), it means this SET event is not propagated though the ICG chain. However, when a SEU happens it will propagate up to the end of the chain and be flagged by all the combiners connected to this part of the ICG chain.

To differentiate between SET and SEU the output of the combiner is fed to two latches in the following way:

- One goes directly to the RS latch to capture the error. It can be an SET or SEU. The output of the latch is read every 5ms and reset.
- The other output goes through a delay element of 1ns followed by a C-cell, and then captured by the latch. This will capture only SEUs (SETs < 1ns will be filtered out).

As the SA of the test structure (combiners + RS latches) is not negligeable compared to the victims (ICG cells), and to differentiate between events caused by the victims and the one from test structure, the latter has been duplicated. The combiners, the RS and the C-cells are duplicated, and outputs are read separately (Figure 4).

As in the case of the logic combinatorial cells, to avoid double hits, the output readings of these test structures are performed every 5ms.

C. *Sequential logic cells*

Functionality, the SEU sensitivity and TID behavior of D flip flops (D-FF) will be evaluated. During irradiation all inputs are static.
The structure of the sequential logic is made for non-radhard and for radhard DICE cells. Due to area limitation, only five versions of DICE (SXDFFRLSLQD2) have been chosen. For the non-hardened DFF all the 12 available flavors of SDFFRLSLQD2 will be tested.

The DICE D-FF are designed to be SEU free. Therefore, it's complicated to correctly estimate the sensitive area for such cells. A way to tackle that, is to consider an area of DICE 10 times bigger than the area needed to achieve enough SA for the non-hard flip flops. And if no event is detected with this huge area compared to non-hard flip-flop, we can conclude that DICE are SEU free.

Therefore, about 42.4k non-hard D-FF and 424.4k DICE are needed. However, to fit inside the available area for this TV (15mm^2), the sensitive area of all these flipflops has been divided by two, but their radiation exposition time will be doubled with respect to the statistical relevance.

The D-FFs are implemented as a Shift Register as shown in *Figure 5*. Many rad-hard buffers are used to clock properly the shift register. External pad is used to check the clock in the last register. The clock flows opposite to data to avoid hold violations.

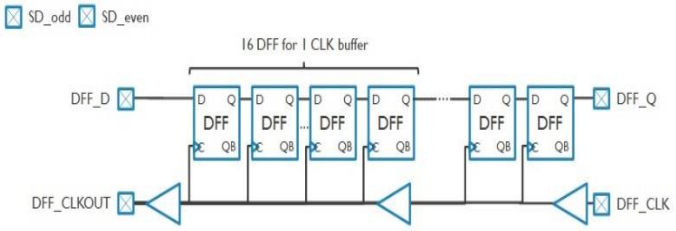

Figure 5: D-FF SEU test structure - principle diagram

Six different tests patterns will be performed on D-FF under irradiation. These are as follows:

- CLK = 0
  - Data = 0 simply reset the SR
  - Data = 1 simply set the SR
  - Data = 101010 … shift in the pattern
- CLK = 1
  - Data = 0 simply reset the SR
  - Data = 1 simply set the SR
  - Data = 101010 … shift in the pattern

The SD input is shorted to the D input in the flip flop laches shift register. This increases a bit the load and improve the hold time during the STA. Also to get a better hold margin, the Scan-Enable is always tied high (shift through scan D).

A mode with a loop back of chain end to chain start through a lockup register has been implemented. This way we can perform barrel shifting to check for dynamic effects during irradiation.

The shift register structures will also be used for TID testing, mainly the current consumption and the leakage current consumption will be characterized in order to validate the library's TID hardening strategy.

III. RING OSCILLATORS

The ring oscillators are mainly used to test the TID effects on the transistors and to characterize the delay and the power over corners and back bias.

16 ring oscillators (1GHz) are designed using the smallest size inverter INVD1 from each core library present in DARE22G. Their frequency variation (so their delays) under total dose radiations will be characterized.

The reason for choosing 1GHz is to have enough inverters to neglect the delay due to NAND cell present in the input stage used to enable/disable these ring oscillators (*Figure 6*).

To allow easier measurements, the frequency of 1 GHz is divided by 128. To optimize the pad numbers of this TV, the power supplies and the ground node are shared between all the oscillators.

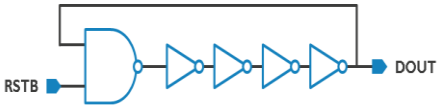

Figure 6 : Ring oscillators schematic - principle diagram

The ring oscillations will be used also to calibrate the delays used for the estimation of the SET duration used with logic combinatorial cells.

IV. INPUT OUTPUT CELLS

A. Bidirectional digital (BD) IO cells

The SEE detection of these cells depends on the TX/RX mode. For the RX one, as shown in Figure 7 two rad-hard latches are connected to the digital output of the RX. Any SET from the RX can trig the latch and become detectable. To filter the events coming from the RS latches itself, a SET filter has been added at the outputs of these latches.

Two internal RS are needed: one is triggered by negative SET and the other triggered by a positive SET. The outputs of these latched will be scanned every 5ms to avoid any double hits.

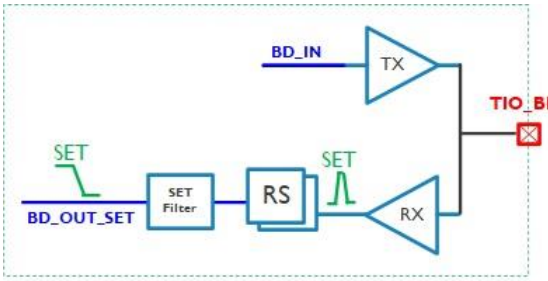

Figure 7: BD RX SET test structure - principle diagram

For the TX mode, two RXs including two rad-hard latches are connected to the output of the TX (Figure 8). Any SET from the TX can trig both latches connected to the two RXs and become detectable. Using two RXs allows to discriminate between events from the TX and RX BD.

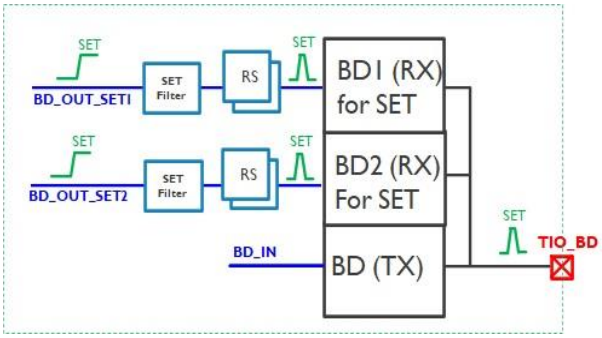

Figure 8: BD TX SET test structure - principle diagram

Half of the radiation exposure time will be used to detect the negative SET, the other half will be used to detect the positive SET on the BD IOs.

TID effects on the BD IO will be performed by characterizing the delay, the leakage versus doses.

B. LVDS TX and RX cells

The test structure of the LVDS TX and RX is presented in *Figure 9*. A loopback configuration between RX and TX can be mounted by the test setup. Thus, a signal will be set in the RX inputs and will be monitored through the TX outputs.

During the SET measurements, the loopback configuration between the RX and TX is needed. As in the case of BD IOs, a hardened RS will be used to detect SETs.

A differential DC signal will be fixed in the inputs of the main RX, any single event from this RX, will trig the RSs connected to that main RX outputs. However, SETs from the TX will be shown in two duplicated RXs (RX1/RX2).

To be noted that an integrated IVREF will be used to provide internally the required biasing current and a voltage reference for the TX/RX. Therefore, to distinguish between SET from the LVDS and the ones from IVREF, this last will be also monitored during SET tests of these LVDS.

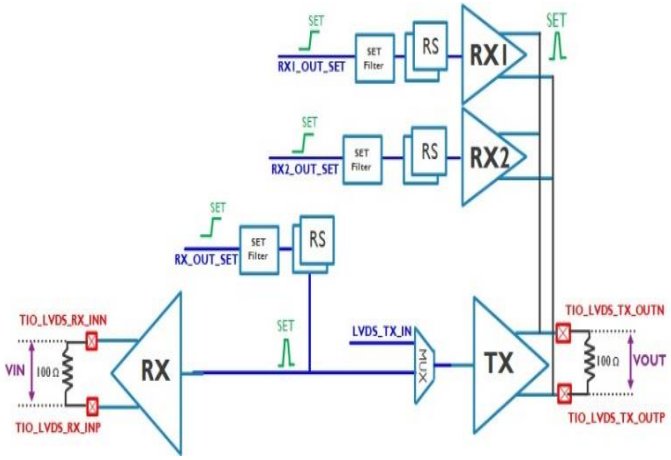

Figure 9: LVDS SET test structure - principle diagram

The eye diagrams, the leakage, and the LVDS features will also be evaluate versus TID doses.

V. ANALOG IP CELLS

All available analog IPs of the library DARE22 is added to this TV. Validation, characterization pre and post TID, and SET testing will be performed for these cells.

The analog IP has been designed to be SET free up to 60Mev.cm2/mg. Therefore, the sensitive area should be null. This must be proven by the SEE measurements.

A. Voltage and current reference IVREF1V8

Figure 10 shows the test configuration for the current/voltage references IVREF1V8. The outputs can be tested on the external pad TO_IVREF_VREF through switches, which isolate (from the external noise) the IVREF1V8 outputs when a direct connection to these external pads is not needed.

Mainly the current consumptions (power-on/down), the voltage, the current references, and the trimming of these voltage/current versus temperature (code giving the smallest temperature coefficient) will be extracted.

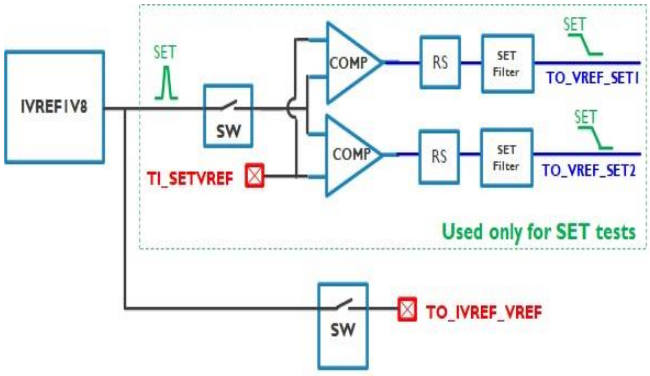

Figure 10: IVREF1V8 SET test structure - principle diagram

Using an external pin to measure on internal signal adds a big parasitic capacitor (capacitor of the pad, the bonding, the package pin, the PCB, the connectors, and the measurement device) on this signal, which will filter some SETs, limiting their observability during the measurements.

Thus, as shown in Figure 10 two fast comparators, which can toggle for any SET on the reference voltage higher than 1ns. The negative input of these comparators can be fixed externally (pin TI_SETVREF).

For instance, to detect negative SET with amplitude higher than 5% and a duration of minimum 1ns, this input will be set to 5% lower than the voltage reference. Once the comparators toggles by a SET, the two latches connected to these comparator outputs will be reset and the SET can be detected. Every 5ms, these latches will be read and reset during the whole radiation campaign.

To distinguish between SET events from the VREF and those from the comparator itself, two comparators are connected on the VREF voltage. Any event not showing in the outputs of the two comparator is not related to the VREF block.

The comparator can be put in power down when not needed.

B. Phase locked loop (PLL)

Figure 11 shows the test configuration for the PLL.

The output frequency of the PLL (up to 3GHz) and the jitter will through a special buffer that has been designed to allow the measurements of such high frequencies and low jitter. To reduce the parasitic inductor of the standard package (CPGA256) used for this TV, three pins are needed to bond the output frequency (TO_PLL_CLKOUT1/2/3 in Figure 11).

The output clock of the PLL is also divided internally by 128 and can be monitored on the pin TO_PLL_CLKOUT_DIV128. This divided frequency will be used during SET measurements. An oscilloscope will be connected to this divided frequency with trigger on the pulse duration if this frequency.

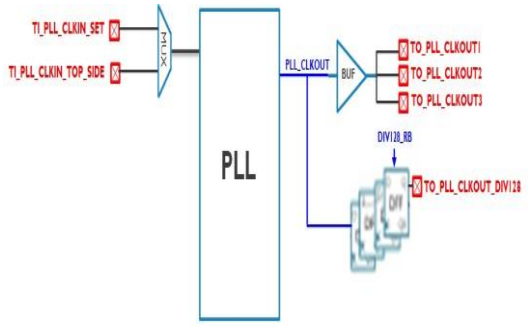

Figure 11: PLL test structure - principle diagram

Two pins are available for the input clock. A mux is used to select between these pins. One pin TI_PPL_CLKIN_TOP_SIDE is placed far from the PLL in the north side of the IO ring, where the PLL is placed in the middle of the west side of this IO ring. The goal is to reduce as much as possible the coupling (mainly through the package) between the input and output clock of the PLL. This coupling degrades the PLL performances, mainly the low jitter that needs to be measured during characterizations.

The drawback of this far pin is the fact that it crosses many noisy blocks before reaching the PLL. Therefore, during the characterization all others blocks present in the TV will be off, except the SPI. However, this last will be quiet as it just used to send the controls.

During SET tests, the noisy blocks crossed by the far clock can't be quiet, so the far clock can't be used. The second clock (pin TI_PPL_CLKIN_SET) placed next to the PLL will be used.

C. *Back Bias Generator (BBG)*

The Back Bias Generator block generates an adaptative voltage depending on the TID dose rate received by this block. This adaptive voltage can be used to drive the body bias of transistors, in order to compensate the effects of TID on such transistors. The BBG output voltages and the current consumptions (on and off mode) will be monitored versus TID irradiation doses.

For the single events effects, the BBG output will be monitored during SET irradiation, but we don't expect events. In fact, the simulations show internal SET with duration lower "ns" order. However, the filtering on this output is in the order of 10 us (Big capacitors).

D. *TID sensor (TIDSENSOR)*

TIDSENSOR is meant to provide an idea of the threshold voltage evolution of all transistors of the target technology with total dose and aging, especially the core transistors. It uses the IVREF1V8 current reference to bias the transistors at their threshold voltage in typical corner then outputs their Vgs when diode-connected. The default mode of the TIDSENSOR connects all measured transistors together to form a ring oscillator that mimics the bias of the core gates. Temperature is also measured using a delta-Vbe bandgap core biased at 1.8V, to remove, in digital, the temperature dependency of the threshold voltage.

The TIDSENSOR output voltages and the current consumptions (on and off mode) will be monitored before irradiation, and versus TID irradiation.

As for the BBG, no SET is expected for this block.

VI. COMMERCIAL DPRAM

There are several motivations to analyse the robustness of different DPRAM configurations.

- To answer future questions of designers of space SoC's on how to select robust DPRAM configurations.
- Often, there are system level choices on speed, size aspect ratio of DPRAM cuts. If there is free choice, then the robustness should be part of the decision.
- Target robustness can be a serious system constraint. Feasibility can be assessed if good characterization is available.

A. *What to Analyse?*

We want to investigate different memory cut sizes to be able to project the effects also on other cuts that are not on the test vehicle.

We need to distinguish between periphery and matrix, and between static and dynamic errors, transient and upset, and between fresh and aged or irradiated chips.

B. *Matrix/Periphery*

The matrix consists only of densely packed 8-transistor bit-cells. Two word-line-parts per column and two bit-line pairs per row are used to address and read/write the cells at two independent ports, respectively. Read or write can happen freely at any port. In the matrix, there are mainly upsets to look for, although an impact in a bit-line could also lead to non-upset in the bit-cell but in the read-out value.

The periphery consists of word-line drivers, address decoders, sense amplifiers, write logic, timing circuits, redundancy logic and other features like test multiplexers. Most of this area consists of combinational logic or analog circuits, and is therefore sensitive to transient faults, but typically no storage elements exist.

Depending on the size of the memory, the area ratio between matrix and periphery can be different from cut to cut. In general, large memories have less relative overhead.

C. *Static/Dynamic*

A static test means that a memory is not in operation during irradiation. Its only job is to hold data properly. Particple impact can lead to upsets of single or multiple cells in the matrix and of output latches. Such tests are straight forward, the content needs to be read out at regular intervals and checked against the expected value.

Dynamic tests are more involved but required to check for sensitivity during operation. In the matrix, there could be destructive or non-destructive read fails, or unsuccessful

writes. In the periphery, there could be unwanted particle related transitions or upsets in the address decoding, causing reading from or writing to the wrong address. There could also be timing problems caused by impact in the timing generation circuits which is active only during an operation.

Dynamic test should be repeated at different frequencies, to break out static and dynamic components. Dynamic tests should be integrated, as the data rate allowed at the test chip during irradiation may be limited.

D. Fresh/Aged

Basic Characterization should be done (leakage, power, max speed) at fresh state and in several irradiated stats (after accumulation of TID).

Also, the Transient and Upset tests should be repeated in several irradiated stats (after accumulation of TID).

E. How to Analyse?

It is possible to analyze a few DPRAM cuts, but not every possible constellation.

We need to distinguish between periphery and matrix. Two or more DPRAM with same address space and size, but different cuts should be chosen for radiation tests.

F. Choosing the DPRAM

Two or more DPRAM with same address space and size, but different cuts should be chosen for radiation tests.

About the memory compiler

In the Global Foundries sponsored IP program, there is only one true dual port SRAM Compiler, the SDPV compiler originally developed INVECAS, now owned by Synopsys [4].

It uses the Global Foundries 8-Transistor (dual port) bit-cell of 0.274 µm2. The bit-cell is about 1.2 µm in bit-to-bit direction and about 0.2 µm in word-line-to-word-line direction. Bit-lines and word-line-lines are grouped into bank-quadrants (always 4), banks (1-4 depending on address depth) and segments (1 or 2) depending on bit width. Here, we consider 8-bit word-lines only, meaning only one segment. In each bank, the bit-cell array is divided into quadrants. Sense amplifiers and write logic divide the bank into left and right, and word-line-line drivers into top and bottom. At most 32 (C064 option) or 64 (C128 option) bit-cells are in one word-line-line of a quadrant. During any read or write, only one quadrant is active.

Single or Multiple Cell Upset During Hold

From an earlier estimation of sensitive area of 10% of the bit-cell, the required max fluence, and previous silicon data, about 5796 DPRAM bytes are need. The next larger size is 8192 word-lines.

Because of the same bit-cell, it is expected that the static Single or Multiple Cell Upset behavior of different cuts will be identical.

Single or Multiple Cell Upset During Read and Write

When considering dynamic cell upset, different cuts may behave differently. For example, during read operation, the word-line line opens the pass transistors, connecting the bit-lines to the cell latches. The sense amplifiers are enabled. During this time, an impact can cause a destructive read. The bit-line capacitance is expected to influence the sensitivity. A larger capacitance requires larger read times, and the sensitive portion of the clock period is increased. Victim cuts should therefore differ in bit-line capacitance to measure an effect.

Another effect is the number of open bit-lines at any time. In general, the larger the MUX-x option, the higher the chances for a heavy ion to disturb a cell opened for read or write. Therefore, the word-line length (in bits) should play a role as well, and victim cuts with different word-line lengths are ideal.

Multi-bit upset and multi-Cell upset

If multiple cells are upset, and the cells belong to different word-lines, chances are that error correcting codes can repair the word-line. If multiple cells belong to the same word-line (multi bit upset), this chance decreases. A safe memory places bits of a word-line as far apart as the worst-case particle impact corridor requires. This calls for largest possible MUX-x options. The bit-pitch in this technology is ~1.2um * x. Notice the design conflict with the dynamic stability which calls for low x. Since multi-bit upsets can be detected in the pattern of the test chip, no special experiment is designed which influences the cut selection.

Choosing the cut

For a target size of 8192 word-lines with 8 bit each, there are only three monolithic aspect ratio options:

Macro name		W08192 B008 M16C064	W08192 B008 M16C128	W08192 B008 M08C128
Word-line length per quadrant	bit	64	64	32
	um	78	78	39
Bit-line length per quadrant	bit	64	128	128
	um	13	26	26
Banks		4	2	4
Quadrants		4	4	4
Bit-cell Area	um2	13312	13312	13312
	%	33.7	41.2	36.2
Macro Area	um2	39471	32339	36757

Testing all three would provide the most insights into testing dynamic effects both of bit-line and word-line lengths.

Note that all cuts have optimum (maximal) multiplexor setting of 16. This maximally avoids multi-bit upsets.

Next to a monolithic solution, the same size could also be reached with multiple instances of smaller macros, e.g.

Macro name		W00128 B008 M08C064	W00256 B008 M08C064	W00256 B008 M16C064	W00512 B008 M16C064	W01024 B008 M16C064
Word-line length	bit	32	32	32	32	32
Bit-line length	bit	8	16	32	64	128
Banks		1	1	1	1	1
Quadrants		4	4	4	4	4
# of instances		64	32	32	16	8
Macro Area	um^2	4316	4730	7245	7939	9328
Total Area	um^2	276248	87364	231832	127024	74628

But the additional area overhead and the limited additional parameter change make the choice less reasonable.

G. *TID effects*

TID effects make the PMOS weaker and the NMOS stronger. Since there is no compensation possible with back-bias (the array well connections are not pinned out), there should be measurements of write-ability before and after TID. There are special write-ability techniques, which can be activated and deactivated by an external pin of the memory.

The periphery does support back biasing (default 0V and 0V for N and P). Compensation is possible but only for PMOS. A test of the maximum R/W speed can be conducted to check for TID impact on speed before/after irradiation. No special experiment is designed which influences the cut selection.

VII. General Access to Digital Signals - SPI-based Digital Test Interface

In order to spare on numbers of (package) pins, many digital signals, both inputs and outputs, are made available through a SPI-type approach. This applies e.g. to digital settings of blocks, to the observation of static digital outputs, etc. On the other hand, the high frequency output of the ring oscillator block is directly available on a pin, i.e. does not pass through the SPI. *Figure 12* shows a top-level view of the TV, including the test interface.

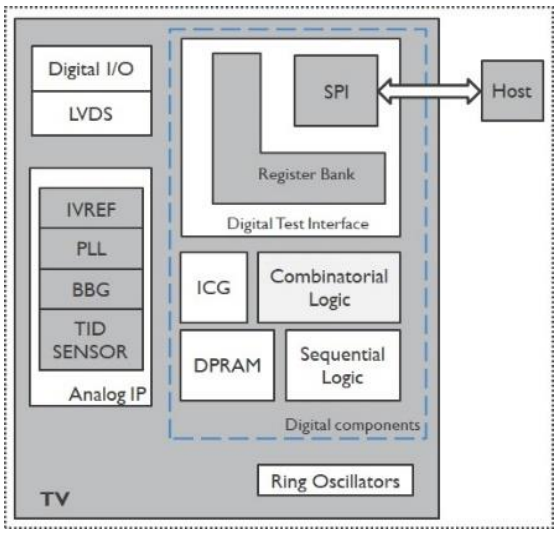

Figure 12: DTI top level view

The protocol used is compatible with the SPI master as implemented commonly in a commercial microcontroller [6].

Next to the SPI is a register bank, in which the data/signals are stored; both together comprise a Digital Test Interface (DTI).

This Digital Test Interface has been designed to be rad-hard up to 60 MeV.cm2/mg, using the DICE flip-flops and a rad-hard clock-trees with triplication. *Figure 13* shows a top-level view of the DTI, and *Figure 14* shows the final layout of this TV.

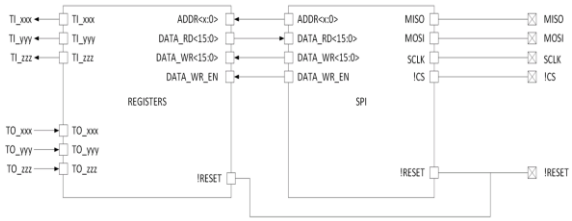

Figure 13: TV top level view

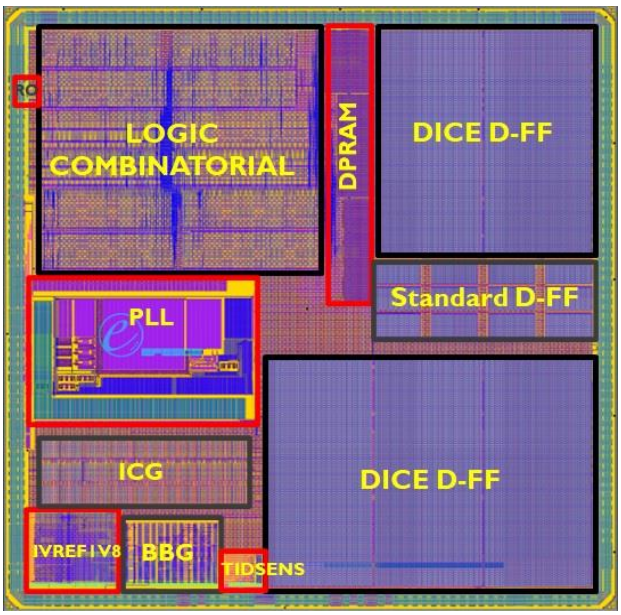

Figure 14: TV top layout

VIII. Conclusion

The description of the DARE22G library test vehicle has been presented. The different tested structures, and how the SET/SEU detections have been implemented are detailed.

The TV has been designed and simulated using the Global Foundry FDSOI 22nm process. Mixed mode simulations including the Digital Test Interface and the victims have been also performed. The final layout has been taped out, and the test developments have already started. The characterization should start once the packaged dies are received, expected early August. The radiation measurements are foreseen before the end this year 2022.

For detailed objectives and consortium information see [7].

Some of the base IP like the foundation libraries and the IVREF1V8 described in this paper is also used in another DARE22G test chip developed for rad-hard non-volatile memory [8],[9].

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