Rad-Hard Mixed-Signal IP-cores in a Fully Depleted Silicon-On-Insulator 22nm Technology

(Abstract)

I. CONTENT

The preliminary structure of the paper is described below:

II. ABSTRACT

The 22FDX technology from Global Foundries [1] is a commercial cutting-edge manufacturing process for integrated circuits. This process combines a characteristic minimum gate length of 22 nm and a FD-SOI (Fully Depleted Silicon-On-Insulator) multi-layered structure. These technological features allow adaptative body bias, ultra-low voltage supply and ultra-low leakage, that benefit, from an electrical circuit application point of view, power-efficient RF signaling, high-performance computing, and robust MRAMs (Magneto-resistive Random-Access Memory). Therefore, this technology is extremely suitable to overcome the current product solutions used in high-speed and low-power AMS (Analogue and Mixed-Signal) applications. Particularly, the SOI technological feature guarantees immunity against single event latch-up.

Although the 22FDX technology is noteworthy, it also presents several challenges for AMS applications. The ultra-low voltage supply leaves reduced space for analog signals. Additionally, the inter-device variability of the threshold voltage due to short channel effects voids some design assumptions used in classic circuit structures. Moreover, for AMS Space applications, ionizing radiation affects the threshold voltage of the FET (Filed-Effect Transistor) devices and degrades the performance of linear circuits. In return, the high operational speed of the technology devices increases the time resolution. Consequently, novel circuital solutions are required to cover the same higher-level functionality.

Our ongoing research, in the frame of the EFESOS project [2], is focused on the development of several rad-hard AMS IP-cores suitable for their integration in complex SoC (System-on-Chip) products for Space applications. For the time being, the design of a high-speed (2 Gsps) medium resolution (10-bit, 5-ENOB) DAC (Digital-to-Analogue Converter) and a high-speed data transmitter (10 Gbps, 1E-12 BER) IP-cores has been accomplished. Furthermore, the design of a high-speed (2 Gsps) medium resolution (10-bit, 9-ENOB) ADC (Analogue-to-Digital Converter) IP-core is ongoing. Although verified by simulation (or partially verified in the case of the ADC), none of these designs have been electrically tested yet. In any case, there are still not similar European solutions available in the market based in the 22FDX technology and proven under radiation [3–5].

The DAC has a current steering segmented architecture, taking the best of the binary-weighted and thermometrical approaches for the current source implementation: on one hand, binary weighted current sources occupy smaller area and are easier to control; on the other hand, thermometrical current sources bring lower DNL (Differential non-Linearity), greater dynamic performance, and monotonicity. Therefore, the combination of both topologies brings a good balance among dynamic performance, power consumption, and area. The 10-bit digital input is binary coded. The six MSBs (Most Significant Bits) drive the thermometric segment by means of two binary-to-thermometric decoders: the most significant three control the row decoder, and the least significant three the column decoder. In fact, the 63 unary elements of this segment are arranged physically and logically in a matrix configuration to optimize area. The four LSBs (Least Significant Bits) are synchronized with the six MSBs with a delay equalizer, so that the binary-weighted current sources are aligned in time with the unary ones.

The data transmitter converts low-speed (up to 625MHz) words (16-bit) into a high-speed single bit stream up to 10 Gbps. Transmitted data can be encoded in an 8b/10b scheme. A high-speed clock (up to 5 GHz) is obtained by multiplying the input clock (up to 625MHz) and used to synchronize the data transmission. The data are serialised using a DDR (Double Data Rate) high-speed shift register and then sent to the communication channel using a CML (Current-Mode Logic) high-speed driver with 50Ω output impedance. In addition, the transmitter allows signal pre-emphasis to mitigate the effect of the channel high frequency attenuation. The pre-emphasis levels are configurable to adapt the transmission to different channels.

The ADC digitize a high-frequency analogue signal (up to 1.4 GHz) with a 10-bit resolution. It is implemented with an 8-stage pipelined architecture. Each of the initial seven stages is composed by a ping-pong residue amplifier and a 1.5-bit ADSC (Analogue-to Digital Sub-Converter). The seven MSBs of the ADC output are obtained from the redundant digital information generated by these initial stages. The three LSBs are directly obtained from the final stage, which is implemented

as a 3-bit flash ADSC with a one-hot digital output after bubble correction. A digital core aligns the data of the different stages and corrects detected errors. All the composing parts of the ADC operate at 2 GHz.

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