Rad-Hard Mixed-Signal IP-cores in a Fully Depleted Silicon-On-Insulator 22nm Technology (EFESOS)

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Abstract

The 22FDX technology from Global Foundries is a commercial cutting-edge manufacturing process for integrated circuits. This process combines a characteristic minimum gate length of 22 nm and a FD-SOI (Fully Depleted Silicon-On-Insulator) multi-layered structure. These technological features allow adaptative body bias, ultra-low voltage supply and ultra-low leakage, that benefit, from an electrical circuit application point of view, power-efficient RF signaling, high-performance computing, and robust MRAMs (Magneto-resistive Random-Access Memory). Therefore, this technology is extremely suitable to overcome the current product solutions used in high-speed and low-power AMS (Analogue and Mixed-Signal) applications. Particularly, the SOI technological feature guarantees immunity against single event latch-up.

Although the 22FDX technology is noteworthy, it also presents several challenges for AMS applications. The ultra-low voltage supply leaves reduced space for analog signals. Additionally, the inter-device variability of the threshold voltage due to short channel effects voids some design assumptions used in classic circuit structures. Moreover, for AMS Space applications, ionizing radiation affects the threshold voltage of the FET (Field-Effect Transistor) devices and degrades the performance of linear circuits. In return, the high operational speed of the technology devices increases the time resolution. Consequently, novel circuital solutions are required to cover the same higher-level functionality.

I. INTRODUCTION

Our ongoing research, in the frame of the EFESOS project (European Commission GA No. 821883), is focused on the development of several rad-hard AMS (Analog Mixed-Signal) IP-cores suitable for their integration in complex SoC (System-on-Chip) products for Space applications. For the time being, the design of a high-speed (2 Gsps), medium resolution (10-bit) DAC (Digital-to-Analog Converter) and a high-speed data transmitter (10 Gbps, 10^{-12} BER) IP-cores has been accomplished. Furthermore, the design of a high-speed (2 Gsps), medium resolution (10-bit) ADC (Analog-to-Digital Converter) IP-core is ongoing. All designs have been verified by simulation (or partially verified in the case of the ADC). In any case, there are still not similar European solutions available in the market based in the 22FDX technology and proven under radiation. All IPs are rad-hard, using a Rad-Hard-By-Design RHBD) approach.

II. Main specifications

The goal is to develop a set of analog IPs suitable for the aerospace market, which implies high reliability, extended temperature range and radiation hardening, while maintain adequate performance.

Parameter	Range	Units
Ambient Operating Temperature	-40; +125	°C
Supply Voltage	0.8; 1.8	V
Data Rate	10	Gbps
Power consumption per TX/RX channel	500	mW
BER in GEO orbit	10^{-12}	N/A
TID	<100	krad
SEL	>70	MeV*cm^2/mg
SEU/SET thr	>20	MeV*cm^2/mg

Table 1. TX SERDES specification

Parameter	Range	Units
Ambient Operating Temperature	-40; +125	°C
Supply Voltage	0.8/1.8	V
Power consumption	<30	mW
Sample Rate	<2	Gsps

Resolution	10	Bits
ENOB	>8	Bits
SFDR (f_{in}<1GHz)	>50	dB
DNL	< ±0.5	LSB
INL	< ±0.5	LSB
TID	>100	krad
SEL thr	>70	MeV*cm^2/ mg
SEU/SET thr	>20	MeV*cm^2/ mg

Table 2. DAC specification

Parameter	Range	Units
Ambient Operating Temperature	-40; +125	°C
Supply Voltage	0.8/1.8	V
Power consumption	<1500	mW
Sample Rate	1;2	Gsps
Resolution	10	Bits
ENOB (125MHz tone)	>8	Bits
ENOB (1.6GHz tone)	>5	Bits
DNL	< ±0.5	LSB
INL	< ±0.5	LSB
TID	>100	krad
SEL thr	>70	MeV*cm^2/ mg
SEU/SET thr	>20	MeV*cm^2/ mg

Table 3. ADC specification

III. TX SERDES

The block diagram shown in Figure 1 is the SERDES transmitter section. The transmit data is provided through a 16/20-bit low-frequency bus which uses 0.8V CMOS levels. Data is transmitted using Non-Return to Zero (NRZ) signals. Incoming digital data has to be synchronized with an external clock which will be 500MHz. The data is coded with and 8b/10b which can be disabled in case the user wants to use different codification scheme. The 16-bit data is then converted into a 20-bit word before is sent through the TX link. This type of encoding is used because it ensures proper DC-balance of 1s and 0s imposing an overhead of 20% on the data rate.

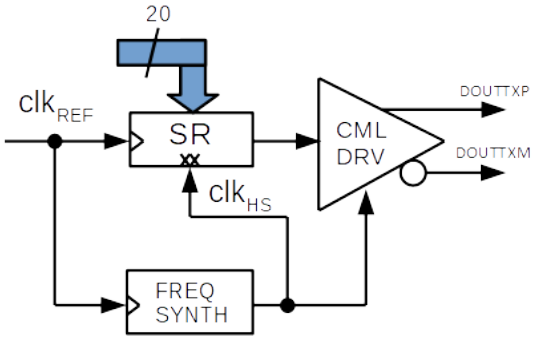

Figure 1. TX Section Architecture.

The encoded data is transferred to a high speed 10-bit DDR serializer, which generates a serial data output at a maximum rate of 10Gbps. It consists of a 10-bit dual shift register loaded in both clock edges. This allows using a half-rate clock reducing the power consumption.

The high-speed frequency clock is generated using a Phase Locked Loop (PLL), with a frequency divider in the feedback path. It uses the reference clock as input and multiplies it by a factor of 10. Achieves a maximum jitter architecture of 0.7ps RMS or 0.1UI, while keeping the radiation hardening behavior needed to achieve the adequate BER.

The output driver is a Current Mode Logic output stage (CML), which provides a maximum differential amplitude of 1600mVpp-diff, over a common mode of 1400mV. The output driver provides also "Preemphasis", which allows to individually configure the amplitude of the precursor through a digital register. This functionality is included to allow to partially remove the Inter-Symbol Interference introduced by the transmission media when high speed signals are sent through it.

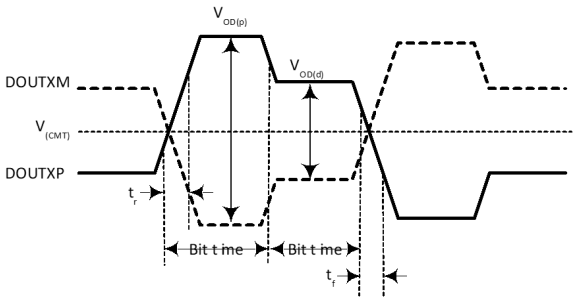

Figure 2. Driver output signals

The output driver has 50-ohm output impedance termination. The output driver amplitude can also be controlled using internal registers.

The digital interface it is based in an AMBA APB interface.

Simulated Results

Simulations have been performed over Process, Supply Voltage and Temperature corners (PVT) to evaluate the system specifications. The achieved BER at the driver output is better than the expected 10-12. In Figure 3, an eye diagram at the driver output in nominal conditions is shown. Single Event Transient (SET) simulations have been performed to guarantee that SEU/SET threshold is achieved.

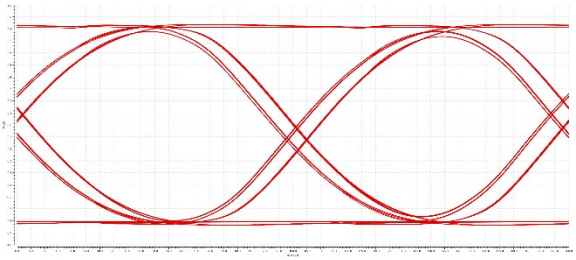

Figure 3. Eye Diagram simulation in nominal conditions (10Gbps) of the TX section output, including noise.

IV. DAC IP

The DAC IP is a high-speed (2 Gsps) medium-resolution (10bit) current steering DAC. This type of topology is well known for its suitability for high speed applications. The architecture consists of a segmented current steering of 6+4 bits (10-bits) at 2 Gsps. This topology achieves the right balance of area and power consumption due to the 4-bit binary encoded block, low INL/DNL, small dynamic errors and good monotonic behavior provided by the 6-bit unitary current sources blocks.

The digital input word (D9-D0) consists of 10 bits with binary coding. The 6 MSB bits drive two binary to thermometric decoders each of 3 to 8 bits, so that the 3 MSB (D9-D7) go to the row decoder and the 4 intermediate bits (D6-D4) go to the column decoder. The 4 LSB bits go to a delay equalizer, so that the bits that drive the unit cells and those that drive the binary cells are synchronized. Then the thermometric bits in rows and columns will control the on/off switching of the unary current cells in matrix, while the binary bits will control the on/off switching of the binary current cells. Finally, the output current DAC (IOUTP and IOUTN) will be an analogical representation of the 10-bit digital word converted. The thermometric segment will be placed in matrix configuration to obtain a more compact design and optimize the maximum possible area, since 63 unary current cells will be required.

The main functional blocks that form the architecture shown in Figure 4 are:

- Binary to thermometric code decoders
- Delay Equalizer
- Unary current cell matrix
- Binary current cells.
- Current and voltage reference

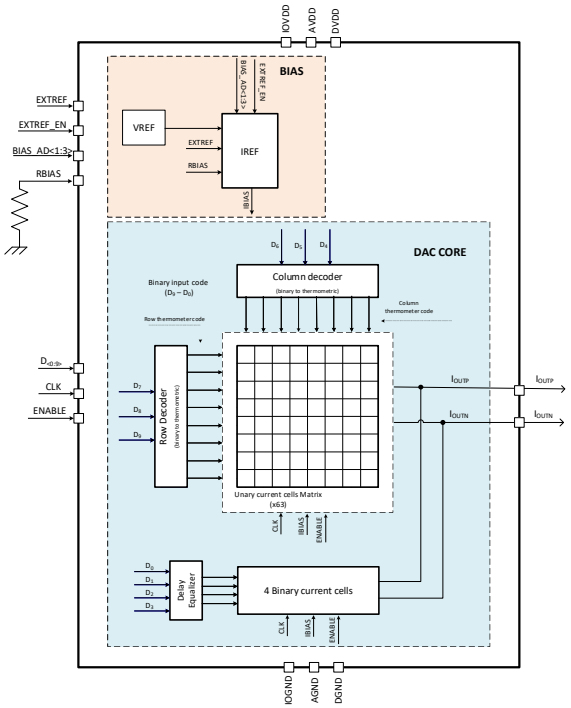

Figure 4. EFESOS DAC IP Architecture

Unary current cells Matrix

To implement the thermometric segment of the DAC 63, equal unary current cells are required. One of the most efficient ways to organize these cells is by using a matrix configuration. This arrangement not only makes the location of the cells more manageable and compact than in a linear array, but also makes the parasites that appear in the data, clock and power lines smaller. Improving the current differences that may exist between some cells and others, just because of their location and routing. Furthermore, as we have seen before, this matrix configuration considerably reduces the complexity of the binary to thermometric decoders to be used. The matrix arrangement, therefore, simplifies both the circuit design and the layout of the DAC.

The output bits of the row and column decoders are used to select which unit cells should be on or off. For this purpose, there is a local decoder within each cell. It is important that the local decoders are simple and do not have many cascading stages in order to obtain a high matrix decoding speed (2 Gsps).

Therefore, the choice of cell selection scheme is very important as it will set the characteristics of the local decoder to be used. An element selection scheme has been chosen which selects the cells from left to right within a row and from top to bottom. Thus, when the first row is completely selected, the first cell of the second row will be selected and so on. A cell is turned on as long as the bit of its row is at high level or the bit of the previous row and its column are high level too.

Unary current cell

Each of the 63 cells will be the same and will have an architecture like the one shown in Figure 5. It is very important that all the unit cells are as similar to each other as possible. To do this, a symmetric design of the unary current cell matrix must be made, ensuring that all the cells are loaded with the same load and have a similar routing.

The local decoder will be responsible to decide whether the cell should remain on or off based on the column (T_{ci}) and row (T_{ri} and $T_{r(i-1)}$) thermometer bits. This local decoder is dependent on the selection scheme of the matrix, which has already been analyzed above. It will be designed with the smallest serial elements to guarantee simplicity and high speed.

The latch will be in charge of implementing the synchronization of the control signals since a degradation in the dynamic behavior of the DAC can be caused by a deficient synchronization of the control signals. The clock that drives the latch will also be buffered to prevent the input data from interfering with the clock. The output of the latch will be differential and buffered to minimize inter-symbol interference (ISI) between the input codes, thus reducing the distortion of the DAC

The latch outputs will be conditioned using a switch driver. It will be designed so that the control signals do not both have a zero value at the same time (make-before-break), so at the switching point between the high level of one and the low level of the other there will be an overlap. Finally, the control signals, once conditioned, drive two control switches (switches S_1 and S_2) which will be responsible for letting the current generated in the current source pass or not. The current output will be differential (positive and negative) and each of the switches will control the positive or negative output (I_{outp} and I_{outn}). The current source will be unique for both branches (I_u).

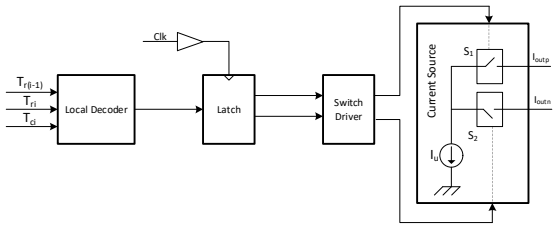

Figure 5. Unary current cell architecture

Binary current cell

There will be 4 binary cells, one for each of the 4 LSB bits. Unlike the unary cells, they will be different from each other, since the current of each cell will be scaled binarily according to the bit that controls it ($2^N \times I$), taking N value from 0 to 3 (0 will be the LSB). *I* is the lowest step of current in the DAC and correspond to the current value of the binary current cell driven by the LSB. Therefore, if the current source of the LSB takes the value *I*, the source of the 4th LSB will take the value 8*I*. The blocks of latch switch driver and control switches will be equal to those used in the unary cells. It may be necessary to use a local dummy decoder to synchronize the output currents of the binary current cells with the output currents of the unary current cells, thus minimizing the spectral distortion of the total current output of the DAC.

Figure 6 shows the architecture of a binary cell where the scaling of its corresponding current will depend on the N-th position of the binary bit (D_i) that controls it.

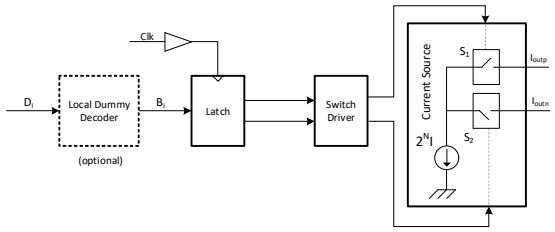

Figure 6: Binary current cell architecture

Current source and control switches

Current sources are one of the key elements in the design of a DAC as they are responsible for generating, as accurately as possible, the output current required by the converter. Most of the accuracy and linearity of the converter will depend on the characteristics of the current source. As mentioned above, the DAC will be composed of several current sources: 63 equal current sources for the unary current cell matrix and 4 current sources with binary currents for the binary part. The output impedance of the current sources and the pairing between different current sources will be two important parameters to take into account when

designing the current source. On the other hand, the control switches must be fast enough to allow the current to pass or not at the maximum data rate that the DAC can support.

Figure 7 shows the typical topology based on a current source and a differential pair of control switches, generating two currents (positive and negative) for each current cell. The control switches should be sized as small as possible so that they are fast enough to make the switching speed of them at least 2GSps. It is important that the signals that control these switches are synchronized to improve the dynamic behavior of the DAC and therefore the spectral distortion. Normally, the current source is implemented in a cascade configuration to have a high output impedance and a more constant current thanks to the lower voltage fluctuations in the current source, in addition it will be necessary to find a compromise between the size of the transistors and the required precision. It must be taken into account when designing it that due to the effects of the transistor parasites the output impedance is finite and decreases as the frequency increases.

The same topology will be used to implement both binary and unitary current cells, the only difference being the current scaling of each, which will be achieved by varying the W/L ratio of the current source transistors.

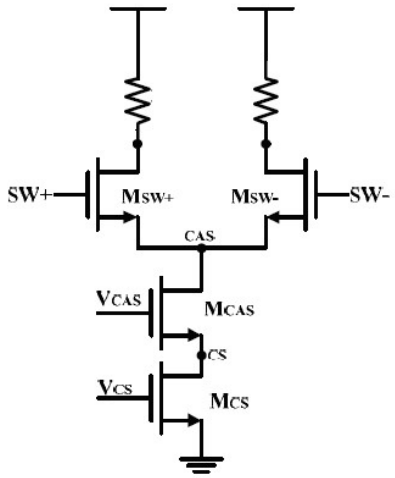

Figure 7. Current source and control switches basic topology of current-steering DAC.

Static errors are one of the most important errors that affect the accuracy of a DAC. Among them, the two most analyzed errors that limit the operation of the DAC are INL and DNL. DNL depends mainly on the DAC architecture, while INL is independent of the architecture and depends on the differences between the currents of the current cells. Therefore, the current source will be a fundamental element to determine the performance of the DAC, being very important to carry out a robust design of it, in which the precision will be very high and the difference between the currents of each current cell will be as small as possible so that the INL is the specified one.

Latch

The latch is responsible for implementing the synchronization of the control signals of the switches. The dynamic behavior of the DAC depends mainly on the latch and also on the switch driver since an imperfect synchronization of the control signals of the current sources will lead to a degradation in the dynamic operation of the DAC. Therefore, it will be very important to put effort during the layout stage in the routing of the control signals and latches, so that all the signals have a similar delay.

The Latch needs to be fast enough to be able to work with 2GSps digital input signals. The topology used for the latch will be based on the topology shown in Figure 8. This topology has been chosen because it is not only fast but also radiation-protected, making it more insensitive to SEE. Since a latch is a circuit that maintains a state, it is highly advisable to use radiation-hardened topologies instead of conventional topologies, because a failure to impact a particle on the latch could be catastrophic for the DAC sample. To reduce the ISI between consecutive codes the output of the latch will be differential and buffered. It may be necessary to isolate areas using rings in the layout to prevent the load from being shared between them.

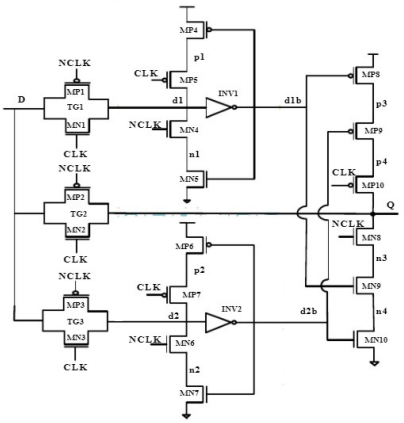

Figure 8. Rad-hard Latch topology

Simulated results

Simulation have been performed over process, temperature and power supply variations (PVT corners). Shown in Figure 9 you can see a detail of the DAC Ioutp output for worst, nominal and best case.

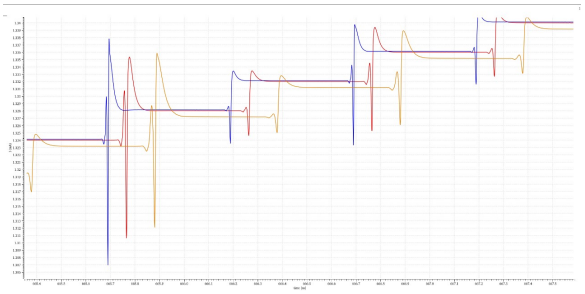

Figure 9. Detail of Ioutp DAC output for nominal, worst and best cases.

Static error simulations have also been performed with very good results. Due to the slow simulation time, DNL and INL have been simulated using mismatch variations at the worst input code only, which corresponds to mid-input code. Simulations gives a DNL of 0.249 LSBs and INL of 0.183 LSB which is much better than expected 0.5 LSB.

Dynamic simulations have also been performed at three different frequencies: Low Frequency (LF), one quarter of the bandwidth (BW/4) and at full bandwidth (BW). PVT corners have been simulated and the worst-case results are presented.

Parameter	LF	BW/4	BW	BW/4 Mismatch (Nominal)
ENOB (Bits)	7,6	7,9	7,7	7,8
SFDR (dBc)	59,4	57,8	62,9	58,1

Table 4. DAC dynamic sim results

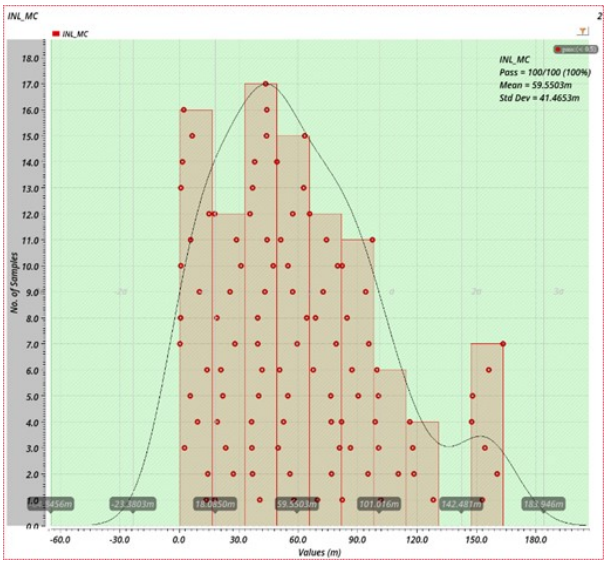

Figure 10. INL Mismatch simulation in nominal conditions at mid-input code. The X-axis units are LSBs.

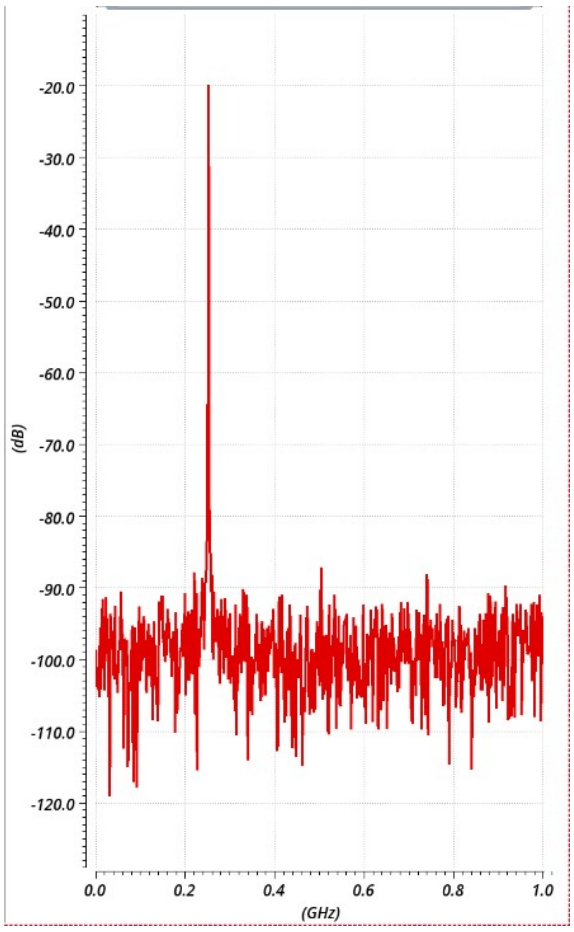

Figure 11. Mismatch simulation, DAC output spectrum worst case plot. ENOB is 7.8bits at BW/4.

V. ADC

The ADC IP is a high-speed (2 Gsps) medium-resolution (10bit) pipeline ADC. This type of topology is well known for its suitability for high-speed applications. The architecture consists of seven 1.5bit stages with an additional 3-bit flash ADC. This topology achieves the right balance of area and power consumption, low INL/DNL and dynamic errors. The latency of this topology is 8 clock cycles.

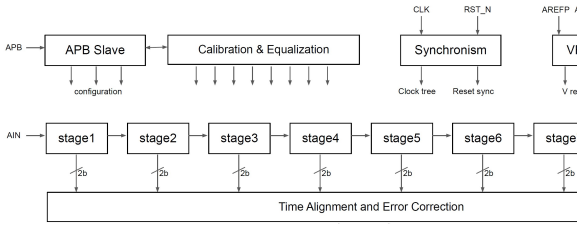

Figure 12. ADC Core Block Diagram

1.5-bit sub-ADC

Conversion stages 1 to 7 are fully differential and share the same block diagram (Figure 13). A 1.5-bit sub-ADC codes the stage's digital output in 2-bit. The conversion residue of each of these stages is amplified to fit the input range of the following stage. The plus and minus references (350 mV and 550 mV) for the 1.5-bit sub-ADC and 1.5-bit sub-DAC are provided by the VREF block.

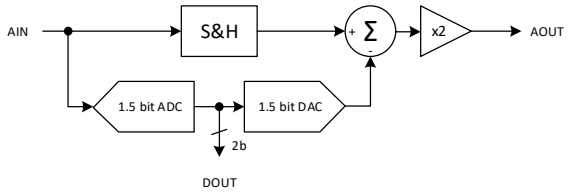

Figure 13. Stage block diagram

3-bit sub-ADC

The sub-ADC is the seventh conversion stage. It has been implemented as a 3-bit flash ADC with fully differential input and signed thermometric output. It is composed by eight fully differential comparators (same as those used in the stages 1.5-bit sub-ADCs).

Synch Block

The synchronism block considers both the reset and the clock trees. Both trees have been SET hardened. Particularly, in the clock tree have been considered the non-overlapping phases needed in the conversion stages 1-6.

Time Alignment and Error Detection and Correction (EDAC)

The block generates the 10-bit digital output from the 2-bit redundant (nominal and complementary) digital outputs of stages 1-7 and the 9-bit redundant (nominal and complementary) thermometric output of the 3-bit sub-ADC. These redundant bits allow the error detection and correction occurred in the analog core due to SET. The time alignment functionality is schematized in Figure 14. To avoid the use of TMR flip-flops, a Hamming-3 coding will be implemented. This concept is represented Figure 15 in for stages 1 to 7.

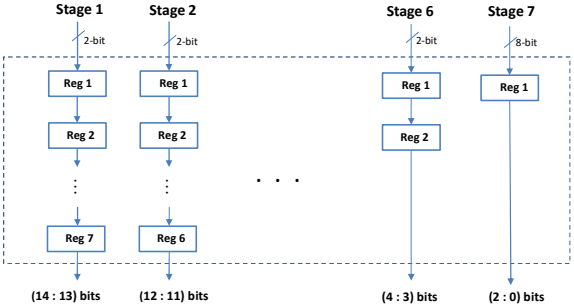

Figure 14. Time alignment diagram for stages 1-7

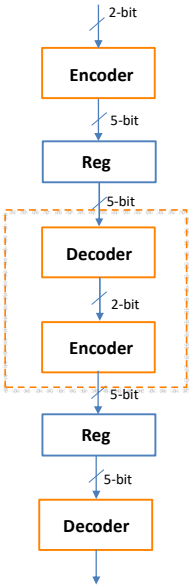

Figure 15. Time alignment hardening concept

APB Interface

The block implements an APB slave interface to program the configuration registers of the ADC IP-core. Its hardening concept is depicted in Figure 16. The EDAC Code can be SEC-DED (Hsiao code: 6 parity bits for 16-bit data word = 22 bits for codeword) or DEC (BCH code: 10 parity bits for 16-bit data word = 26 bits for codeword). Scrubber is mandatory block to avoid accumulation of errors in APB registers.

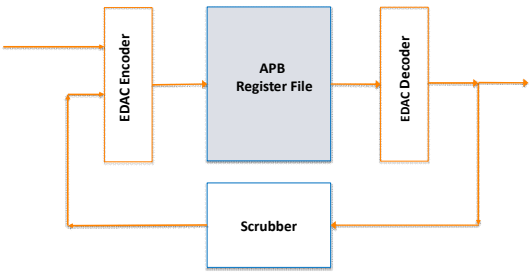

Figure 16. APB hardening concept

Simulated results

Simulations have been performed over PVT corners at schematic level. Analysis shows that an ENOB of 8.4 bits and SFDR of 54.9 dB is achieved for BW/8 input tone in nominal conditions at maximum sample rate. For the worst-case conditions, the ENOB degrades to 7.1 bits and the SFDR to 45 dB also using BW/8 input tone. The degradation observed in the worst case makes to be non-compliant with the specifications. Further investigations will be performed to improve this behaviour.

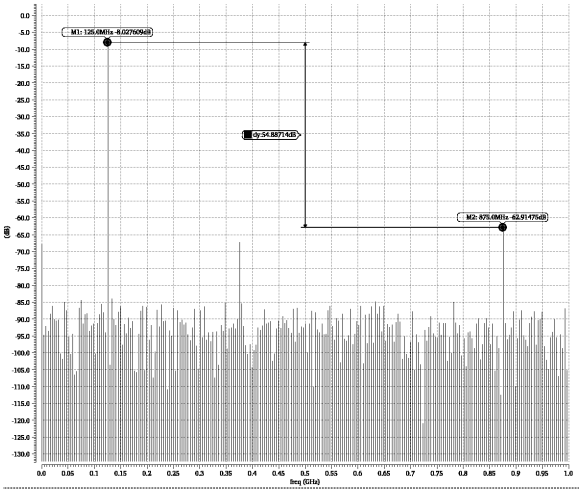

Figure 17. Nominal case, ADC spectrum plot, for an input tone of BW/8 and fs=2Gsps, ENOB=8.4 Bits.

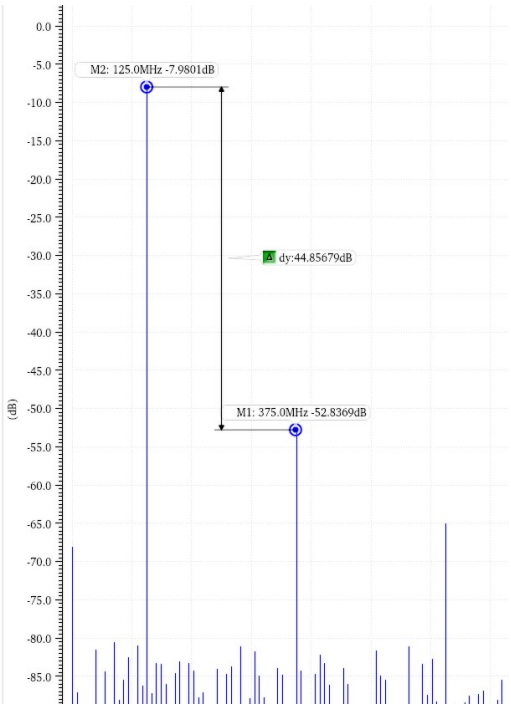

Figure 18. Worst case conditions (ss, +125°C, 0.72V/1.62V), ADC spectrum plot, for an input tone of BW/8 and fs=2Gsps, ENOB=7.1 Bits.

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European Commission GA No. 821883