A Mixed-Signal, Single Event Upset Tolerant Analog Front-End IC for Redundant Electromechanical Actuator Applications

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***Abstract*— A highly integrated, mixed signal integrated circuit (IC) implements most functions needed for acquisition and for control synchronization in redundant electromechanical actuator applications currently targeting aviation/launch/low Earth orbit. The IC is implemented using circuit and system design techniques to be immune to single events affecting internal circuits and/or communications interfaces. Actuator system design is highly simplified, and system reliability is increased by dramatically reducing the number of components v.s. traditional approach.**

I. Introduction

Electronics for electromechanical actuators usually extend from the sensors for position/velocity to be controlled (usually Linear / Rotational Variable Differential Transformer - LVDT / RVDT - or resolver) to driving the currents in the windings of an electrical motor and brake solenoid. Typically, besides position, other sensor data related to the safe operation of the actuator is needed (e.g. temperature at several points that determine the safety envelope (e.g. torque/pressure, currents, voltages etc.). This data is fed to a control algorithm that is executed via software on an MCU or via digital signal processing (DSP) and state machines if running in a field programmable gate array (FPGA) fabric. Control outputs in the form of pulse width modulation (PWM) are fed via gate drivers and power devices to the motor/brake. In this type of control, usually, a synchronous sampling scheme is needed to reduce system interactions.

While high-safety, high-reliability electro-mechanical actuator design normally involves a redundant scheme it also requires quite a large amount of IC and discrete devices to cover all functions (see Figure 1). Therefore, there is a need to integrate as many of these functions as possible to reduce size/mass and increase reliability at system level. This is especially important for aviation and launch system applications.

II. A Fully Integrated Analog Front-End IC for Electro-Mechanical Actuators [1]

A fully integrated analog front-end (AFE) shall cover all acquisition functions and support synchronous sampling while implementing a single event upset (SEU) immune interface to the MCU/FPGA processing. Additionally, the IC shall have a simple power scheme while still interfacing with some of the sensors' larger voltage. Early in the design process the decision was made to not integrate gate drivers and power

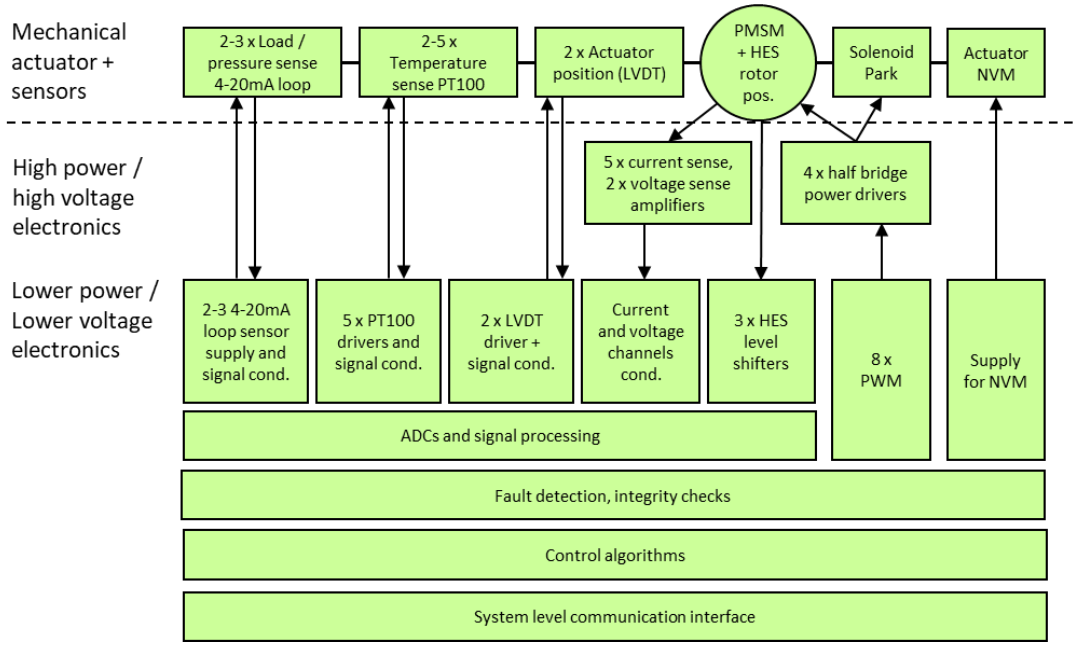

Fig. 1. Functional diagram for a high end electro-mechanical actuator

devices to drive the motor windings to allow the usage of same AFE with different actuator power/voltage level combinations. Also, the level shifting/isolation needed for current and DC line voltage sense is not included in the IC as it is application dependent.

The following is a summary of the functions that are integrated in this circuit (see Figure 2 - AFE block diagram):

- Redundant LVDT/resolver driver with primary voltage sense
- Redundant LVDT/resolver 2 x secondary sense supporting 5/6 wire sensor connections
- Multiple PT100/PT1K channels supporting 2/3/4 wire sensor connections
- Multiple 4-20mA loop sensor interfaces (high side power switch with protection and low side current sense) for other sensors
- Redundant motor DC line voltage sense channels
- Multiple motor winding current sense channels
- Internal DC regulators to support single 10-30V input supply
- Internal register file for ADC conversion results and subsystem status using triple redundant storage

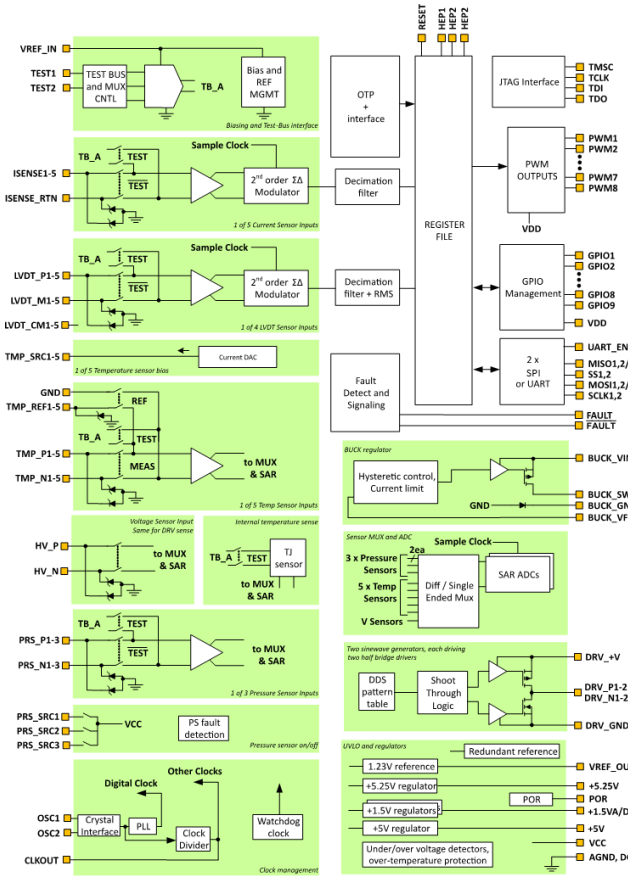

Fig. 2. AFE block diagram

- Fully programmable set of PWM generators that are synchronous with the overall channel acquisition.
- Redundant SEU immune SPI/UART communication interface to host with hardware single error correction / double error detection.
- Internal fault checkers and redundant fault signaling.

This IC implements an extended set of fault-checking for inputs impedances, internal supplies compliance and measurement data range thus detecting open /shorts or parametric faults internally or by using host-level software drivers. Additionally, the AFE sports two dissimilar reference voltage blocks with a cross-checker to detect parametric drift. This way reference value drifts and analog to digital converter (ADC) parametric errors can be detected during normal operation while acquiring data.

For SEU immunity, the higher accuracy channels (LVDT and current sense) are implemented with delta sigma modulators followed by SEU immune decimation filters while the other channels can be fed to one of the two redundant 10-bit successive approximation register (SAR) ADCs that use triple redundant comparators for the successive approximation decision.

Digital communication (SPI or UART) to the host integrates a single error correction, double error detection hardware encoding to avoid executing incorrect writes from the host and allow for single bit correction of acquisition data received by the host. This is more efficient than the host to operate majority/redundant read/write cycles.

III. LVDT SENSING

Within this IC, the position-sensing has the better precision and noise requirements and is done using two independent channels usable as fully independent or as redundant driver / sense. The LVDT drivers can be independently programmed for frequency and waveform and are implemented using a PWM based direct digital synthesis (DDS) topology with external L-C filters. Usually, the user will program a sinusoidal waveform and will run a slow amplitude regulation software loop that will update periodically the DDS tables used to synthesize the output waveforms. Overall the circuit can drive up-to 10V RMS sinewave. Two differential voltage acquisition channels are used to sense the DDS generated waveform on the LVDT primaries.

The LVDT secondary channels (2+2) are fed via voltage dividers and some external filtering to per-channel sigma delta modulators. Internally each secondary channel samples a fixed number of samples per LVDT driver period and calculates the true root mean square (RMS) value as the square root of the sum of squares of acquired samples. This is done by a triple modular redundant (TMR) based logic DSP block that implements a first decimation filter, a squarer, an averaging filter with a second decimation and a square root calculation. The RMS value for each of the two secondary channels (A and B) is available as a register value to be read by the host. The actual position calculation is finalized by the host to calculate the relative position as (Va-Vb)/(Va+Vb).

Additionally, the host should implement the system level mechanical linearization and calibration for position.

The overall position measurement error at system level for one LVDT channel is 1.2x10-4xMR and the RMS noise of each sample is below 6.1x10-5xMR (where MR is the input measurement range).

In order to achieve this level of precision there are several factors that were addressed:

- IC is calibrated at test,
- at board level we provide guidance on how to implement a gain matching calibration for the two secondaries channels,
- at system level (when integrated with the actual sensor) one can also implement an overall gain/offset/linearization of the overall characteristic

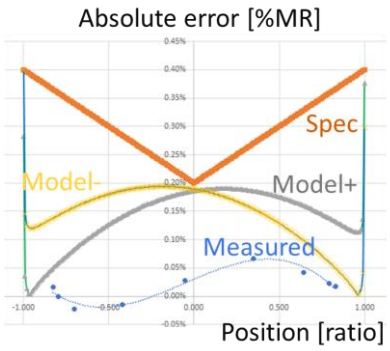

Fig. 3. LVDT absolute position error: specification v.s. system model v.s. measured data

For the design of this IC we used a methodology compatible with DO-254 US aviation standard for hardware that implements requirements tracking from system modelling down to hardware validation. Figure 3 compares the system model and IC measured data v.s. the system requirements.

There are on-chip error checkers for LVDT drivers that detect open/short on primary or secondary channels and common mode driver faults for secondary windings. These are implemented by a combination of DC current sources sourcing/sinking from the pin. The effect of these is observed either via dedicated comparators or at system level by observing the effect on the digital value from the channel..

IV. OTHER CHANNELS

Other acquisition channels that are needed to support the electromechanical actuator are remote temperature sensing and pressure, torque or other mechanical measures characteristic to the system.

The temperature interface consists in a current source driving a current in a series connection of a remote RTD and a local reference resistor. Each temperature channel uses an operational amplifier (OPAMP) based differential amplifier that reads either the voltage across the resistive temperature detector (RTD) or across the reference resistor. The ratio of the two values is the ratio of the two resistors because the same current flows through both resistors. At the host level, the MCU can calculate the temperature based on the standard curve corresponding to the PT100 RTD. LX4580 implements five such temperature channels.

The other mechanical channels are in the form of 4-20mA loop read channels with high side, current limiting current switch. The voltage drop across the switch is amplified and converted to digital via a SAR channel, the current is acquired using an external low side reference resistor and a n OPAMP based signal conditioning block.

To support power control the circuit implements five current sense delta-sigma ADCs and two DC rail voltage sense SAR channels. All analog input channels implement open/short detection.

V. APPLICATIONS

In a typical application, LX4580 is used in a Permanent Magnet Synchronous Motor (PMSM) linear actuator with redundant drive and sense electronics. We implemented a demonstrator using the LX4580 evaluation board (EVB) connected to an off-the-shelf power motor driver board (PWMs, current sense, DC rail voltage sense) and to an MCU evaluation board via the redundant SPI interface, GPIOs and FAULT interface. The MCU executes filed-oriented-control (FOC) algorithm for each PWM cycle on the motor winding drivers. For each PWM cycle the MCU reads over SPI from

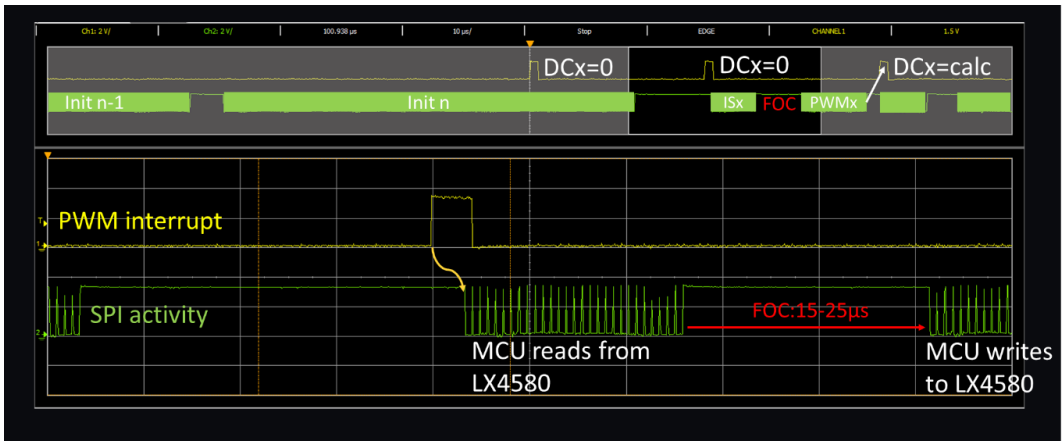

Fig. 4. Typical timing sequence in a PMSM application using LX4580 and an MCU.

LX4580 phase currents, DC rail voltage and position, based on these values it calculates the PWM duty cycles for the next cycle, see Figure 4. After calculation the MCU writes the next cycle PWM values and can do other lower sampling rate safety checks.

VI. Conclusions and Future work

A highly integrated mixed signal IC with SEU tolerance by design was presented together with results in applications involving electromechanical actuators for aviation/launch and low Earth orbit. Among other blocks it integrates 9 delta-sigma ADCs and 2 SAR ADCs and a single input supply power management scheme allowing to power both internal electronics and all sensors. Position accuracy in system is better than 13 bits and RMS noise is below 1 LSB of 14 bits. Radiation and reliability tests still need to be carried out, preliminary LASER tests and proton tests predict good single event latch-up (SEL) immunity, ratiometric measurements and self-calibration for all critical channels should provide good support for total dose performance.

References

[1] "24 Channel Data Acquisition System with Synchronized Motor Control Interface," LX4580 preliminary datasheet, Microchip Technology Inc., 2021. https://www.microsemi.com/document-portal/doc_download/1244912-lx4580-datasheet