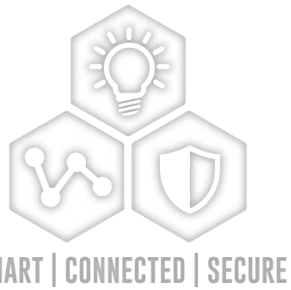
A Mixed-Signal, Single Event Upset Tolerant Analog Front-End IC for Redundant Electro-mechanical Actuator Applications

A Leading Provider of Smart, Connected and Secure Embedded Control Solutions



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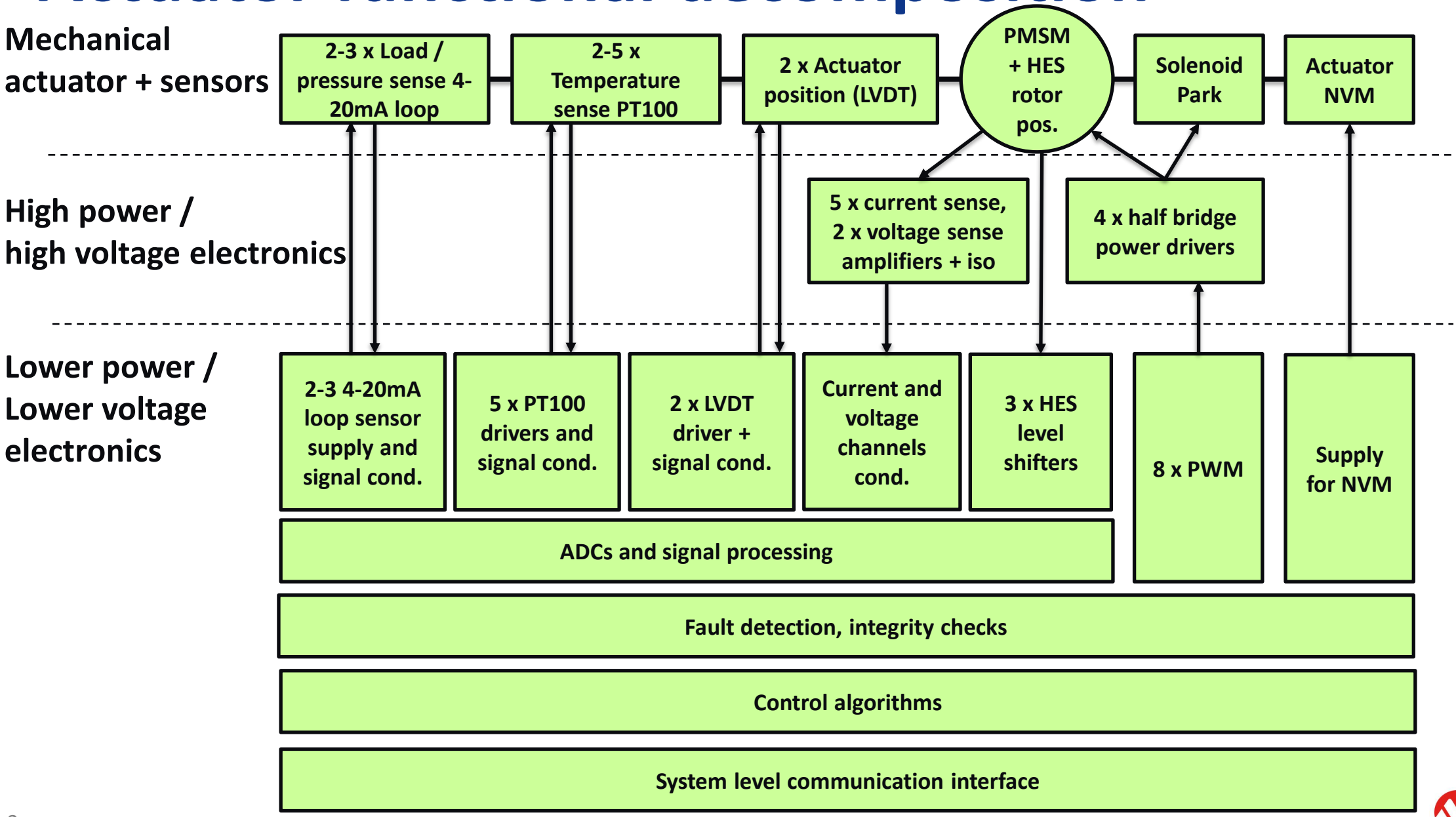
Agenda

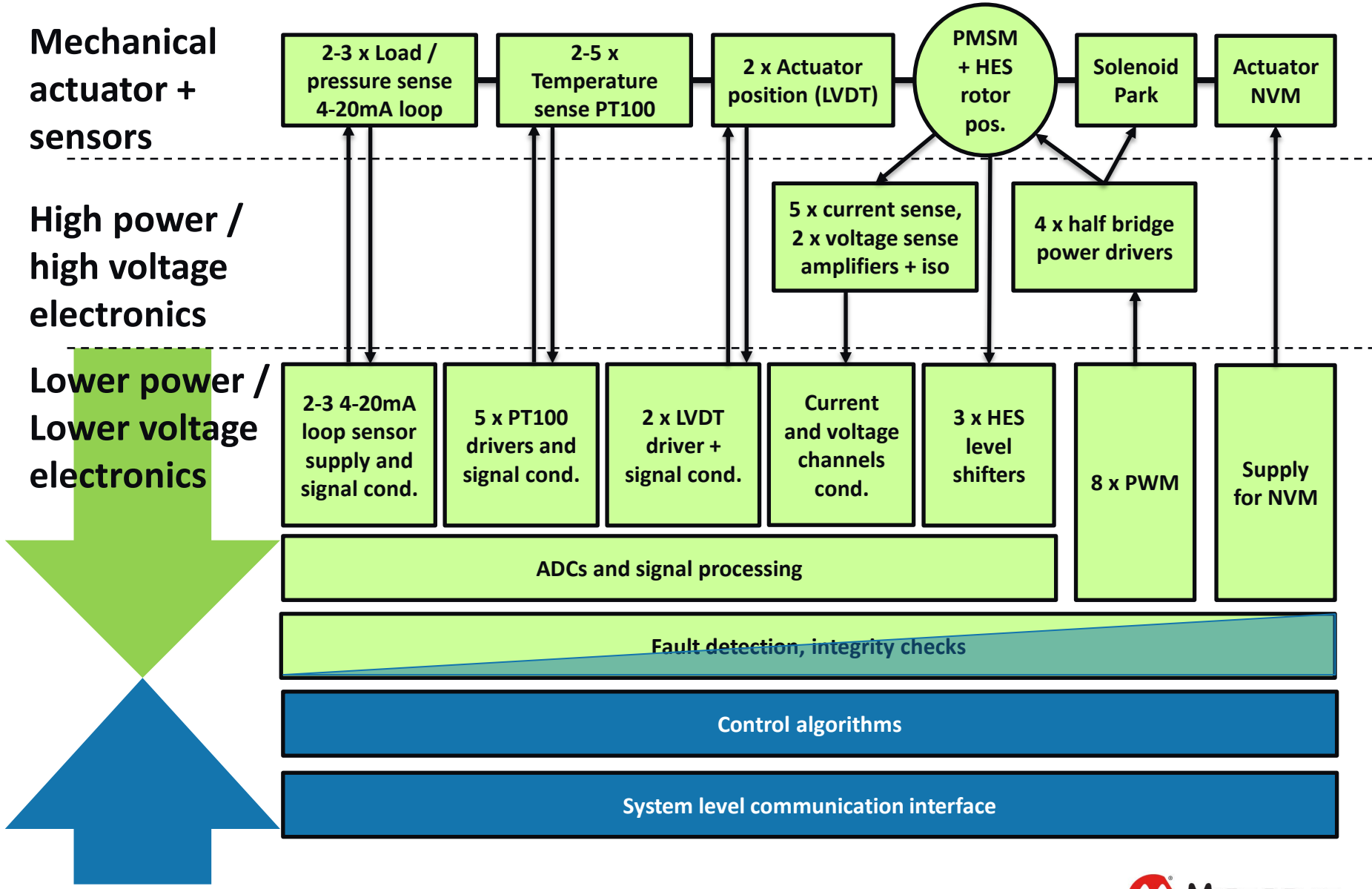
- **Architecture of acquisition for an actuator system**
  - Perspective of IC integration
  - Position sensing
  - Other channels
  - Support for power control
- **Synchronous system**
- **AFE IC**
- **Applications**
- **Experimental data**
- **Conclusions**

Actuator functional decomposition

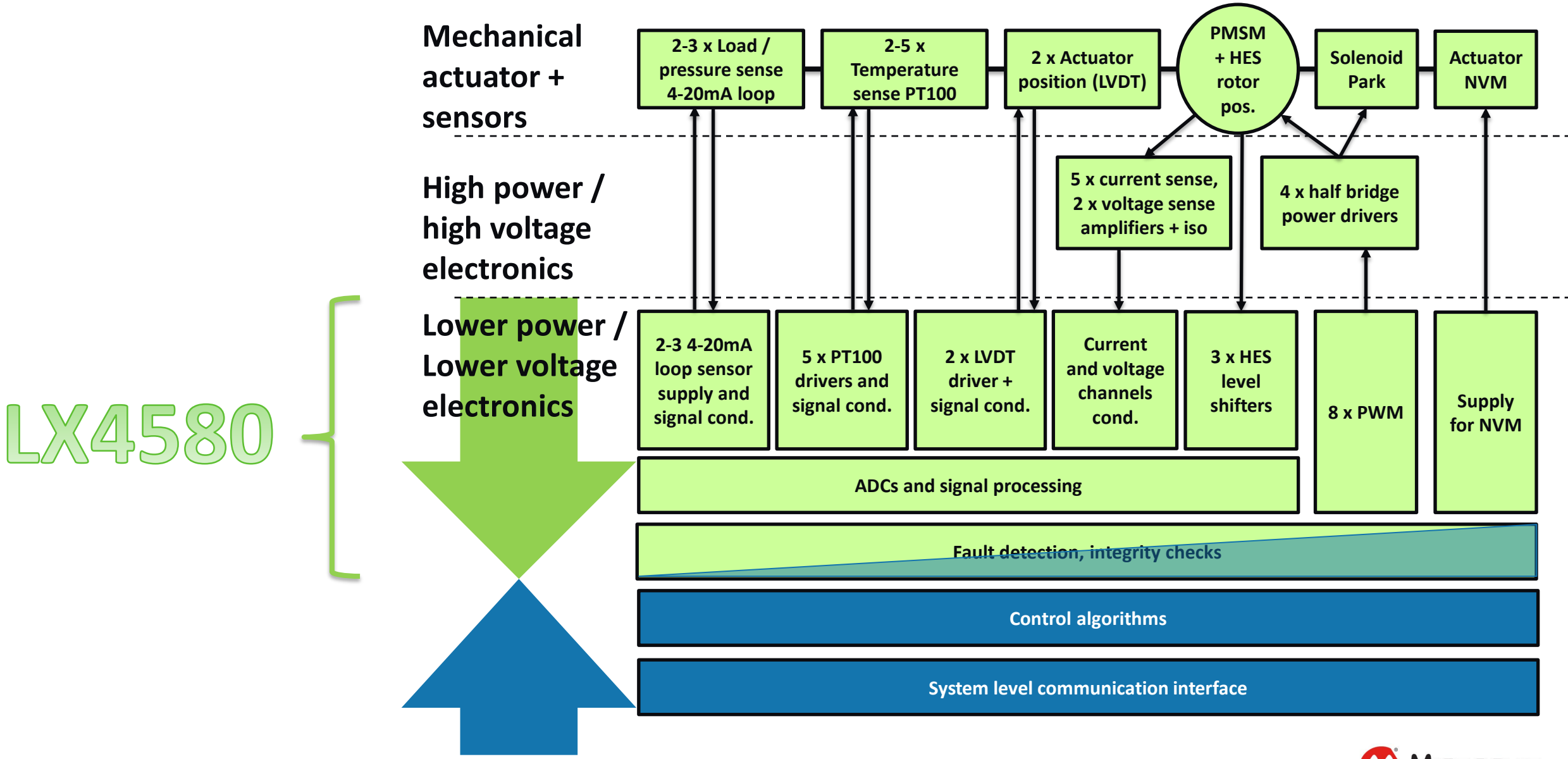


Actuator functional decomposition

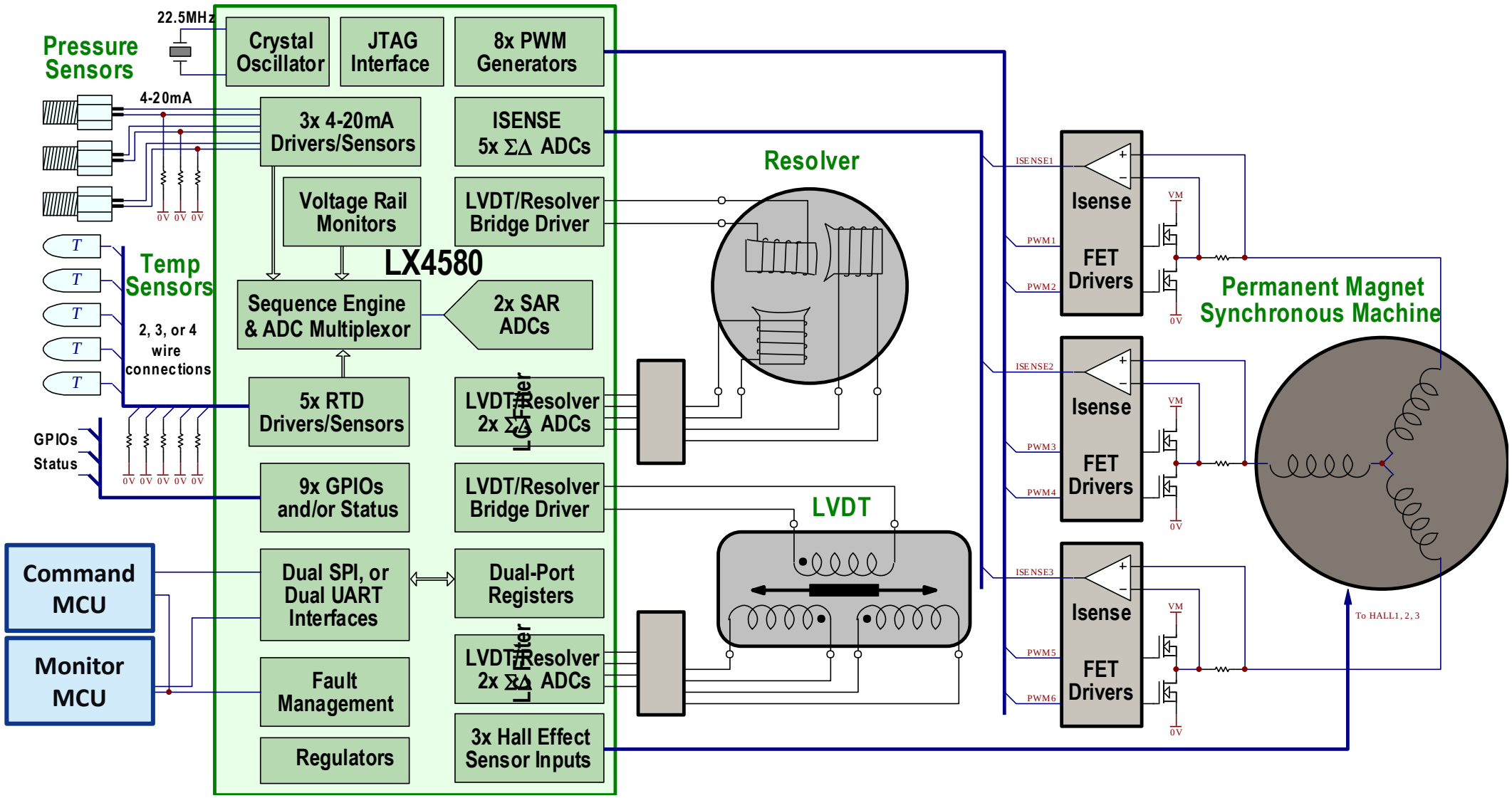
- High voltage / isolation technology needed
- In a regular technology, it makes sense to integrate all low voltage functions as much as possible.
- MCU / FPGA land



Actuator functional decomposition



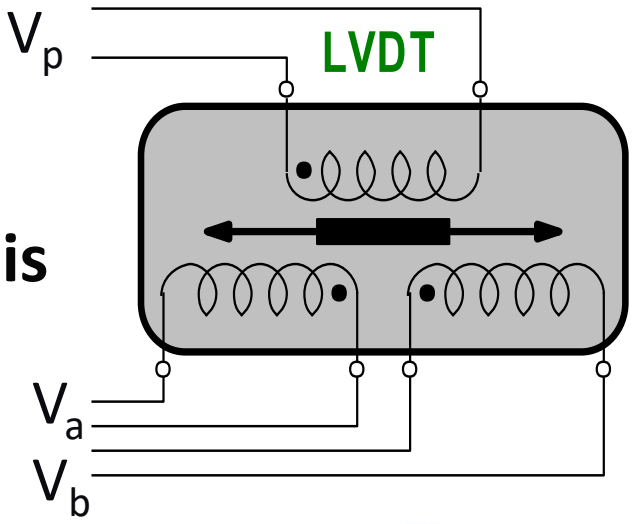
A fully integrated analog front-end for actuation



Position sensing

- **Higher performance position sensing is usually based on LVDT sensors, requires:**
  1. Driver for the LVDT primary: low frequency (~kHz), Vp=3-10Vac RMS
  2. Two AC RMS acquisition channels to determine the RMS voltage in each of the two secondary windings.
  3. Post-processing to determine position, usually a combination of an ideal equation with some added calibration/corrections done in system

$$x = \mathfrak{F}\left(\frac{V_a - V_b}{V_a + V_b}\right)$$



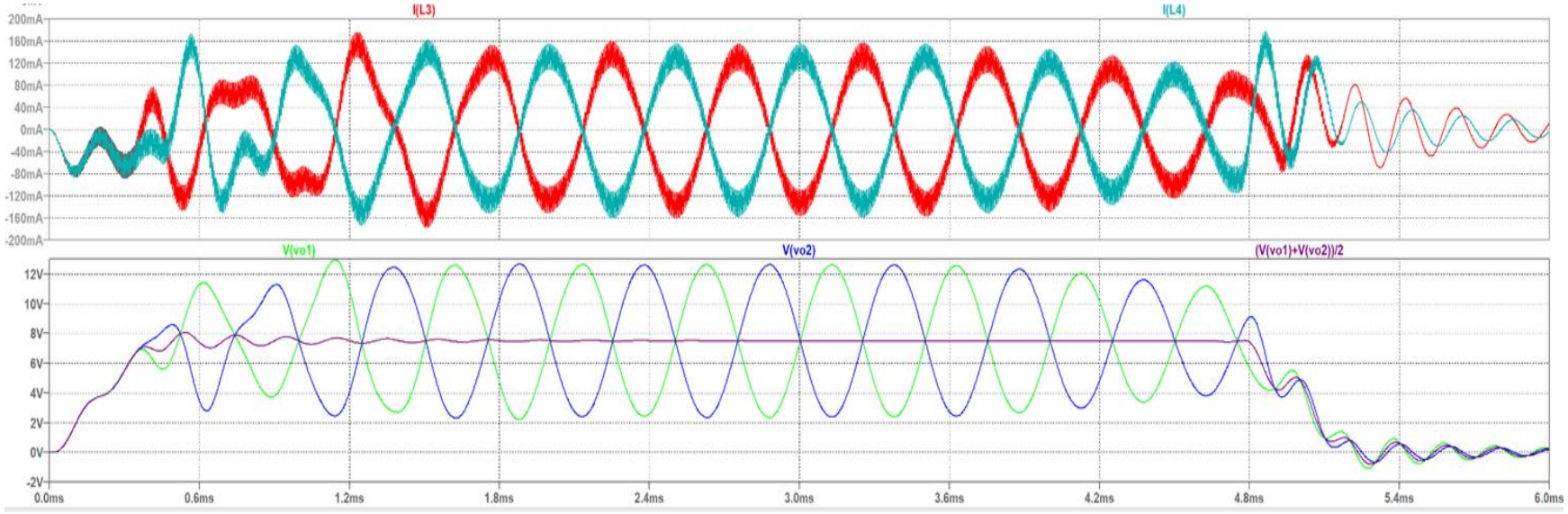
- **Post-processing is system/application-dependent, and it is desirable to be user-programmable: will implement only (1) and (2) on-chip**

Position sensing (cont.)

- **For redundancy, system implementation uses either two separate LVDT sensors or one sensor but two sets of electronics for driving and reading secondaries.**
- **Our design features two separate sets of electronics for driver and channel read that can run as:**
  - 2 fully independent LVDT drive/read channels with potentially different primary frequency / amplitude / phase.
  - 2 redundant drivers and redundant read channels connected to the same LVDT using same primary frequency.
  - Read channels can be synchronized or phased to obtain twice the sampling rate on the same sensor.

LVDT driver

- **Circuit implemented as a differential H-bridge with external LC filter**
- **PWM data is played periodically from a vector on-chip register with the following programmable parameters:**
  - Each PWM value in the pattern
  - Repetition length of pattern
  - Frequency of each PWM pattern element.
- **If LVDT sampling is slow (much slower than once per half sinewave period), at system level driver can be started and stopped on demand for lower power:**



LVDT read channels

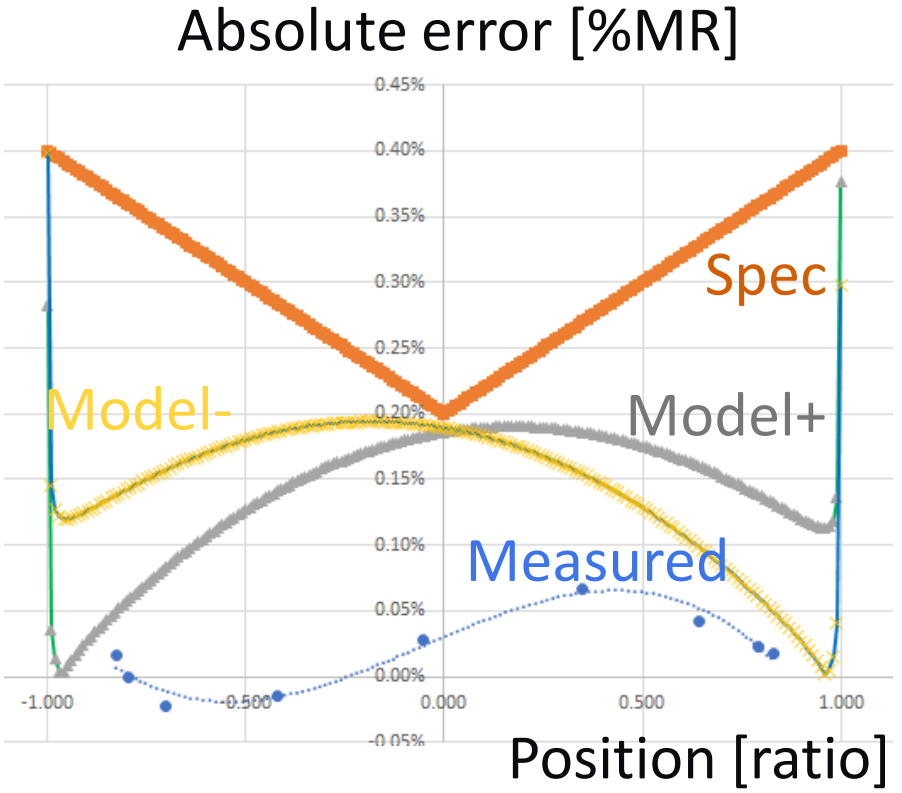
- **External resistive dividers + filters to support a large range of sensors: voltage and 5/6-wire type**
- **Input impedance and biasing fault detection**
- **Delta Sigma ADCs dedicated for each channel**
- **DSP block to calculate RMS or alternate measures:**
  - Filter + decimate -> squarer -> per period average -> square root
  - In our implementation sampling is designed to be synchronous with the DDS generated.

  This is possible because both the driver signal and the sampling signal are generated starting from the same time base on our IC.

  The harmonic / synchronous design of LX4580 enables integrating a lot of high accuracy / low noise channels

Accuracy and noise of LVDT channels

- **Test setup: use LVDT driven by LVDT driver, 15V input voltage.**
- **At several positions, measure LVDT RMS sense values using a 6 digits meter and using LX4580 (average and stdev).**
- **Calculate position = $(V_a-V_b)/(V_a+V_b)$ and calibrate w.r.t. full scale (no extra linearization).**
- **Plot results v.s. model v.s. requirements.**
- **Calculate position equivalent noise and compare to requirements: ENOB = 13.4 bits > 13 bits**
- **Resolution > 14 bits by design**



			Req (max)
Max err	Blue dots	MR	Orange
Resolution	$2^{-(14+)}$	MR	2^{-14}
Noise RMS	$2^{-13.4}$	MR	2^{-13}

Design / Verification assurance

Targeting DAL-A (highest level of assurance for DO-254 US aviation standard)

- **Complete requirements tracking across all design phases**
  - Requirements are clearly enumerated (a single html file contains all requirements)
  - System and circuit design artifacts (source files, schematics) were annotated with links to requirements (unique tags)
  - Verification test-benches were annotated with links to requirements
  - Design review documents were annotated with links to requirements
  - Daily, all artifacts were parsed, and a table of coverage was published
- **Independent verification**
- **Revision control system for all artifacts including design reviews**
- **Documented and proven Microsemi/Microchip design flow:**
  - Using a top-down model-based design approach (high level models before low level implementation)

Other auxiliary functions beyond position

- **High power electronics and motor interfaces:**
  - Temperature sensing:
    - 5 independent PT100/PT1000 channels with internal current source
    - Supports 2-3-4 wire connection of remote RTD
    - Detects open/short on the analog interface
    - Implemented as an internal OPAMP based signal conditioning measuring ratiometric the RTD and a reference resistor, result is converted to digital using one of the two redundant SAR ADCs
  - Pressure, torque, etc.
    - 3 x 4…20mA loop external sensors
    - Includes power switch and low side current sense
    - Supports high side current limit and open/short detect for high side and low side of the sensor.
    - Implemented as an internal OPAMP based signal conditioning measuring the voltage drop on the external sense resistor

Support for power control

- **PMSM/stepper application:**
  - Sense:
    - Currents in 4 windings
      - Signal conditioning, OPAMP based (differential sense w.r.t. a common return pin)
      - Detects output impedance of external driver to determine per channel fault
      - Detects shorts between neighboring pins.
      - One delta sigma ADC per current sense channel, programmable sampling rate
    - Voltage 2 DC rails, external resistive divider and possibly RC filter, ADC done using the dual redundant SAR
  - PWM drive synchronized with sense
    - 8 independently programmable PWM digital outputs
    - Programmable phase and harmonic relation to the sampling frequency

Synchronous system

- **Main problem with a high level of dissimilar acquisition channels: Interference.**
- **In our IC we decided to make all processes either synchronous or in a harmonic relationship:**
  - Most errors / interference = offsets that can be calibrated at system level
  - However, user need some frequency configuration planning in advance

Frequency plan example

- **Input / crystal frequency = 22.5 MHz (20-30 MHz)**
- **Timing resolution = PLL output = Input clock x 4**
- **Motor control**
  - PWM frequency = Input frequency / 2048 = 10.986 kHz (5-21 kHz)
  - Current sense modulator clock = Input frequency / 16; OSR = 256 => sample frequency: one per switching cycle (average current) (1x – 32x per PWM)
- **LVDT1 driver + sense**
  - PWM cycle = Input frequency / 128 = 175.78 kHz (90-500 kHz)
  - Sinewave frequency = LVDT1 PWM cycle / 124 = 1.418 kHz (0.6-22 kHz)
  - Modulator clock = Input frequency / 16 = 1.406 MHz (1-5MHz)
  - OSR1 = 124; OSR2 = 8 => 1.518 ksps (1x or 2x sinewave frequency)
- **LVDT2 driver**
  - PWM cycle = Input frequency / 96 = 234.38 kHz
  - Sinewave frequency = LVDT2 PWM cycle / 116 = 2.020 kHz
  - Modulator clock = Input frequency / 12 = 1.875 MHz
  - OSR1 = 116; OSR2 = 8 => 2.020 ksps

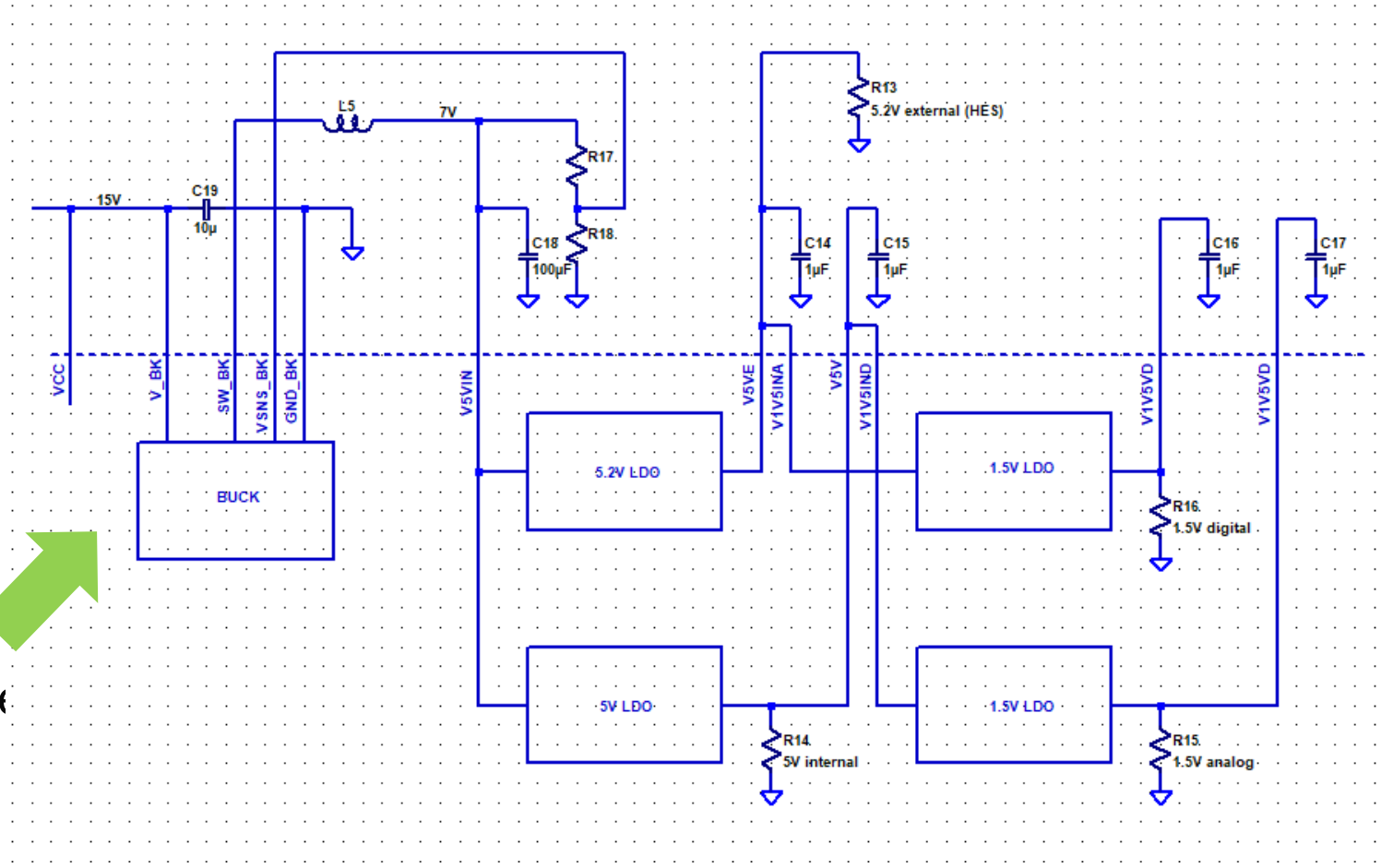
IC power management: single input power rail

- **On-chip regulators:**
  - 1.5V digital supply LDO
  - 1.5V analog supply LDO
  - 5V internal supply LDO
  - 5.2V external supply LDO
  - Buck DC/DC converter with external inductor and external divider

Case 1: Power 5V LDOs from VCC, power 1.5V LDOs from 5V rails

Case 2 (recommended): Use buck regulator to feed the 5V LDOs, use the 5V LDOs to power the 1.5V LDOs

Case 3: Case2 + use an external buck regulator to feed the 1.5V LDOs



Other functions

- **Communication with the host**
  - 2 SPI interfaces addressing a two-port register file with collision management:
    - Can run independently for redundancy / spare
    - Can use both interfaces to double the bandwidth
    - Communication protocol uses a hardware implemented SECDED code for immunity to single event upsets.
- **Synchronization with the host**
  - Master clock is either generated on chip using an external crystal or can be driven by the host
  - A set of programmable GPIOs are provided to generate interrupts liked to different internal processes
- **Fault signaling**
  - A two IO (FAULT and FAULTB) redundant interface to protect against single event upset triggering.

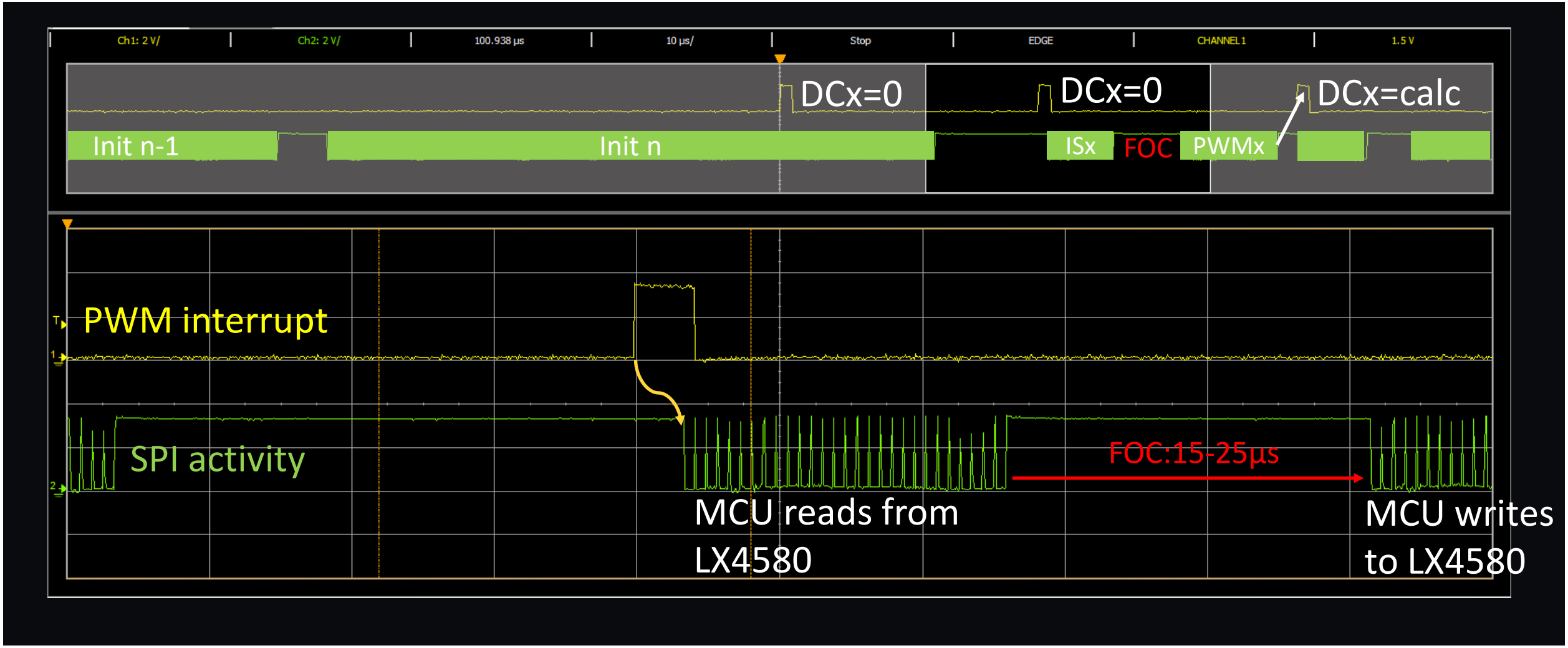
Fault management

- **Self-detected faults:**
  - Inconsistencies, wrong inputs, wrong configuration
  - Wrong output or power load (max or min current)
  - Under and over voltage detection, Over-current, Local over-temperature protection
  - Host communication issues (SPI SECDED encoding)
- **Host assisted fault detection**
  - Prevent wrong data to host: 2 pin fault I/F, encoded SPI, sync signals freq
  - All analog channels (LVDT, PT100, 4-20mA loop, motor voltage and current sense) support detection of open / shorts and some parametric faults via internal current injected in pins or other impedance detecting.
  - Other redundancy: redundant SAR, redundant band-gap reference.

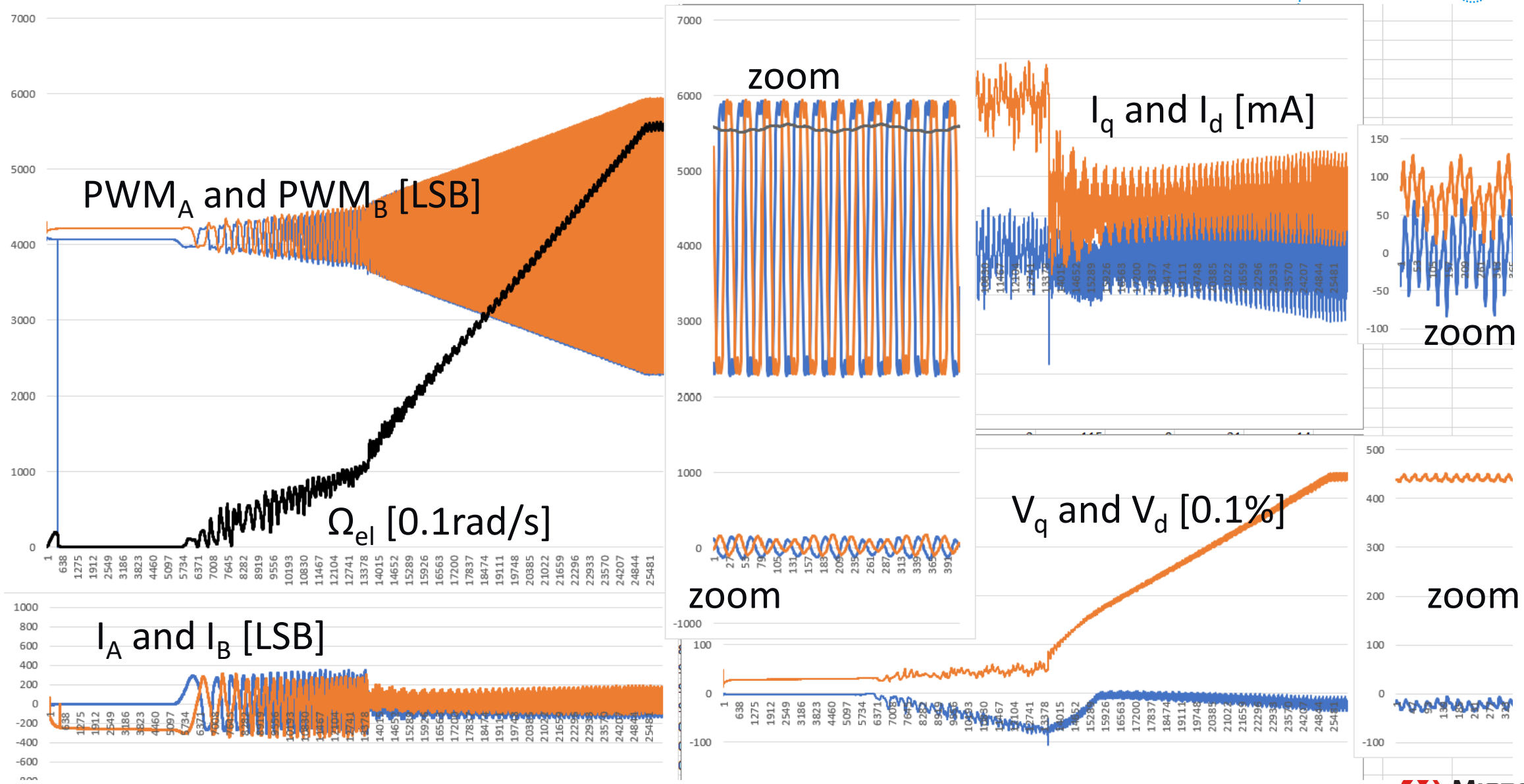
Application in PMSM

- **A 3-phase 5 pairs of poles PMSM is driven using an off-the-shelf driver board**
- **The LX4580 EVB was wired to the driver board**
- **An MCU board was connected to the LX4580 EVB**
  - MCU runs a FOC regulating speed of the motor
  - MCU captures data during motor control
  - MCU interfaces with a host PC emulating higher-level control

Initialization and PWM start detail

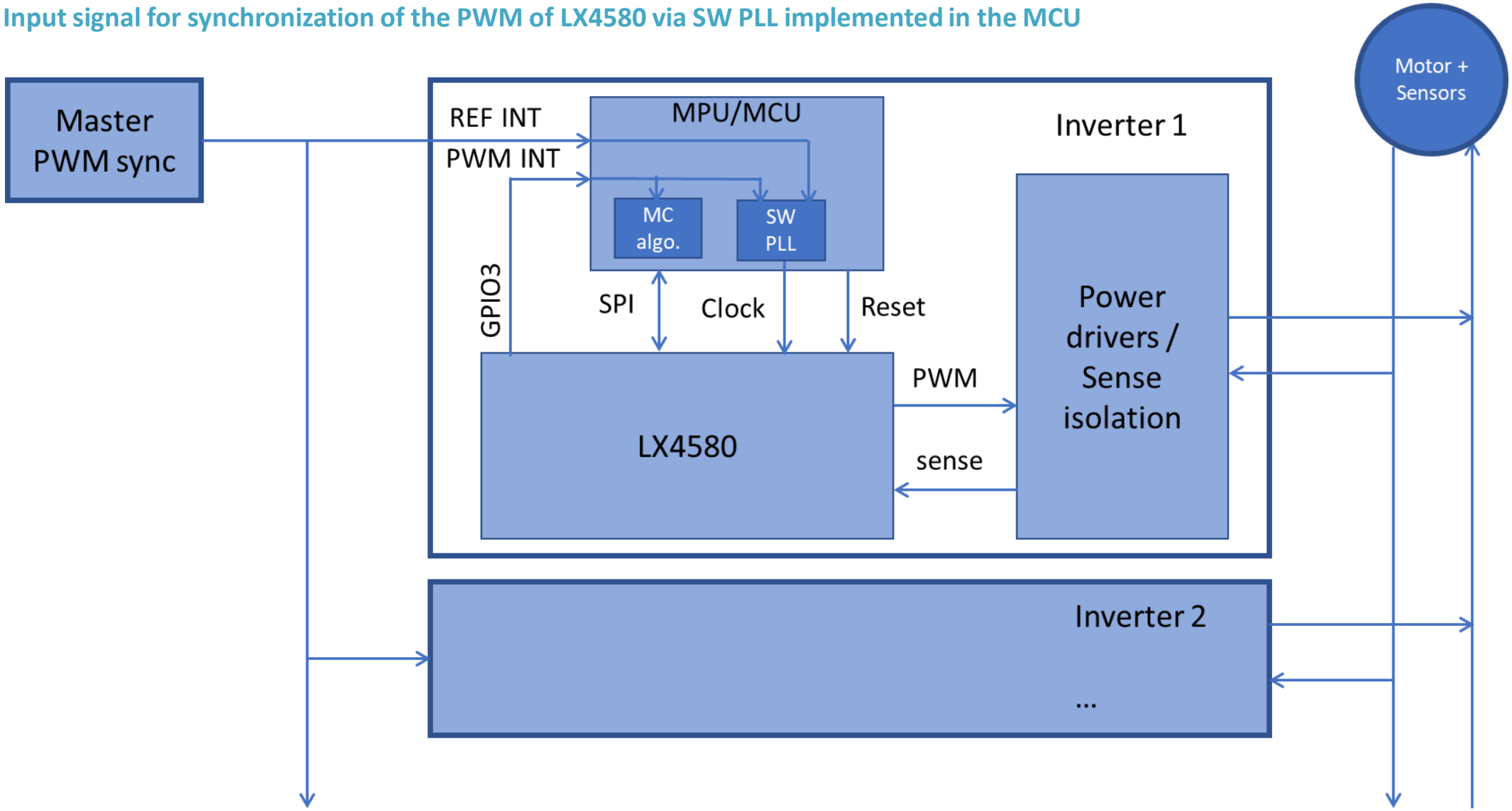


Waveforms dump at low velocity (decimate by 4)



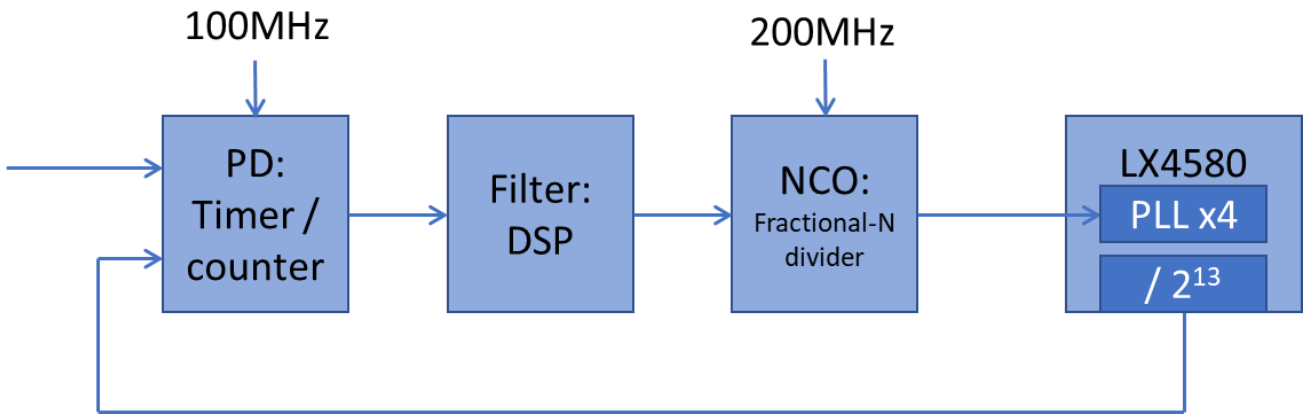
External PWM synchronization (blade architecture)

Input signal for synchronization of the PWM of LX4580 via SW PLL implemented in the MCU



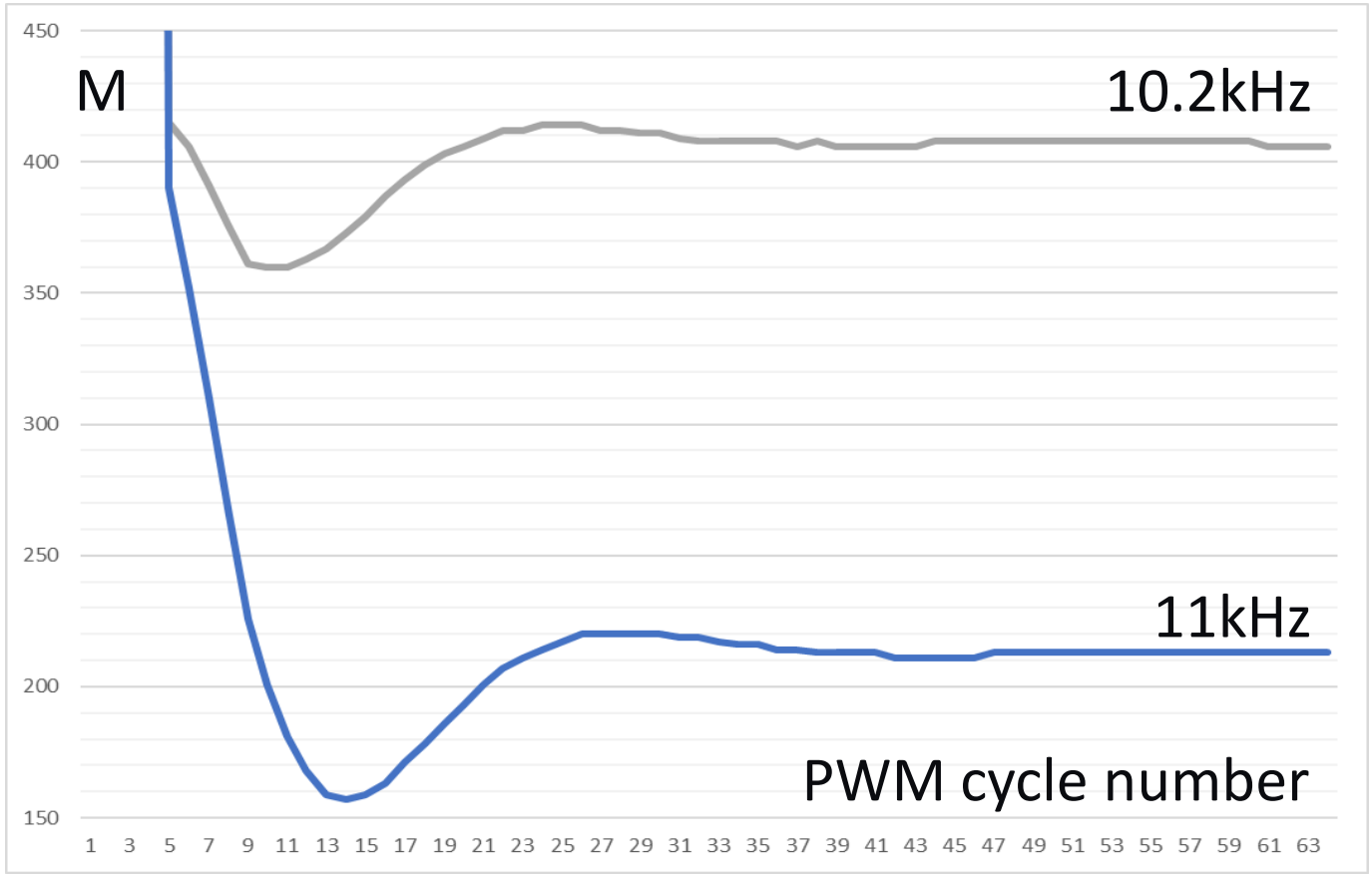
Software PLL details

- **Demonstrator implemented using an MCU.**
  - Phase Detector runs using two interrupts (for the two inputs of the Phase Detector) measuring the phase difference with a 100MHz resolution.
  - DSP filter creates a PI loop,
  - The Numerically Controlled Oscillator is a fractional-N divider with output frequency 200MHz/(2*(N+M/512)). For this application we set N=4 and control M.
  - LX4580 is programmed to generate a PWM cycle by dividing input clock effectively by 2^{11}.
  - Loop is designed to lock at 180 degrees w.r.t. reference signal. PWMs can be programmed to have any phase w.r.t. the feedback clock.
  - More sophisticated techniques can be used for higher performance.



Prototype results

- **SW PLL lock range is 10.2-11.2kHz (out of 9.6-12kHz range of the NCO).**
- **Tracking jitter is about 1µs-pp**
- **Lock time: after ~40 cycles phase is locked.**

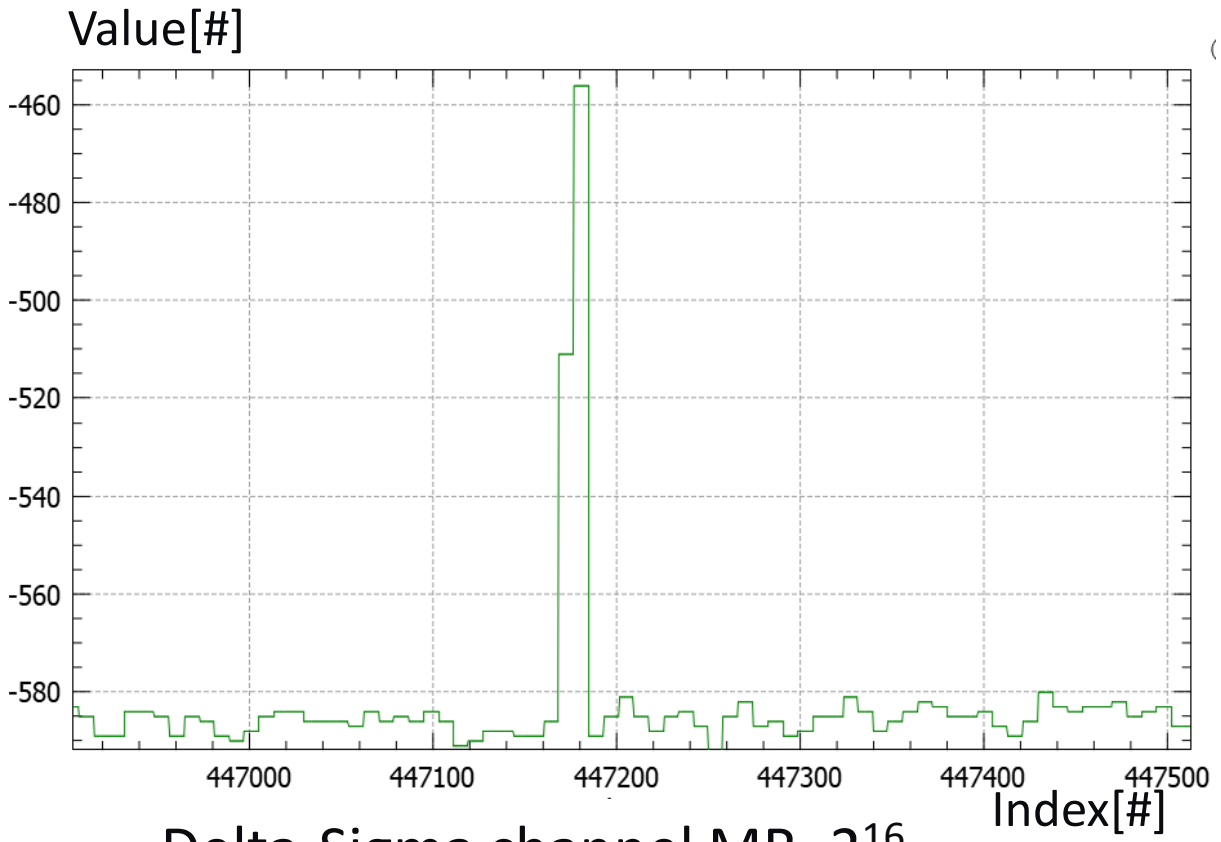


SEU experimental data

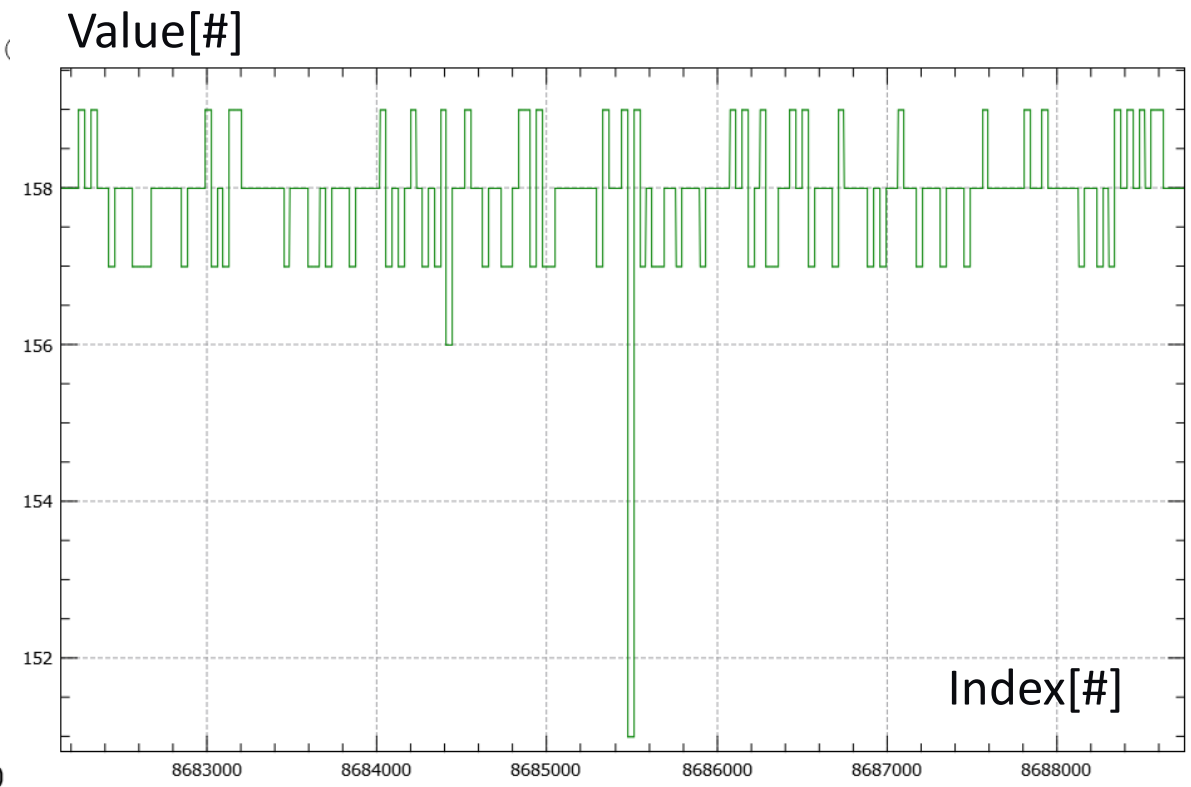
- **Currently we did some TID experiments with heavy ions and proton SEL/SEE:**
  - Single event induced latchup was not observed
  - We are currently characterizing LVDT and SAR channels acquired data:
  - Both LVDT nor SAR always recover after events and the response to events is small.
    - SAR events manifest themselves as one sample off by a small amount
    - Delta sigma event outputs show up as two samples off by a small amount (due to the nature of the $SINC^3$ filter)
  - In both cases data can be easily filtered at system level by a low order running median digital filter.

SEU experimental data (cont.)

- **Examples of acquired data**



Delta-Sigma channel MR=2^{16}
Peak error = 0.2%MR



SAR channel MR=2^{10}
Peak error = 0.7%MR

Additional data

https://www.microsemi.com/product-directory/actuation/5581-lx4580
https://www.microchip.com/en-us/solutions/aerospace-and-defense/aviation

- **Package:**
  - Plastic LQFP 144 with exposed pad (0.5mm pitch)
  - Looking in the future at:
    - Hermetic packaging if needed
    - Smaller size smaller number of pins with reduced functions
- **FIT**
  - Current FMEDA analysis for LX4580 using automotive Siemens standard and IEC28680 applied to aviation application (mission profile, redundancies, etc.): PMHF FIT = 2.54 (qualifies for ASIL-D <10)
- **IC Sampling**
  - Early engineering samples are available (rev up will be available in Q4)
  - Evaluation board Rev1 available to order
  - Code examples (C, Python) for several MCUs (ARM, MIPS, RISCV) and FPGA
  - Applications for PMSM, linear actuator control, COM/MON architecture example.

Conclusions and future work

- **We have shown a fully integrated option for all low voltage functions needed for a redundant actuator, targeting high safety applications for aviation/launch and possibly in LEO**
- **Many aspects of the design concur to the high immunity of the IC to single events:**
  - TMR logic
  - Redundant analog and ADC blocks
  - Using delta-sigma for higher resolution channels
  - Digital filtering
  - Synchronous design

- **Further activities will address more characterization for radiation tolerance to support LEO or better.**