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Radiation Hardened DDR3 Physical Interface (PHY and IOs) in Flip-Chip C65SPACE Process

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Abstract

The aim of this communication is to present the hardening approach that has been followed towards the realisation of a hardened DDR3 PHY when targeted on the C65SPACE platform of ST Microelectronics. The implementation concerns the flip-chip version of the IP. The key points that will be presented are: i) the key requirements the PHY IP should meet, ii) the PHY architecture, iii) the RTL to gate flow that has been executed for the digital part of the PHY with emphasis on the hardening precautions, iv) the gate to layout flow that has been executed for the digital part of the design with emphasis on the hardening of the delay elements, v) the modification of the commercial I/O buffers in order to become hardened while maintaining the I/O pitch as small as possible, vi) the modification of the hardened I/O buffers in order to become flip-chip and vii) the hardening rules that have been followed during the top-level IP integration.

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