Radiation Hardened DDR3 Physical Interface (PHY and IOs) in Flip-Chip C65SPACE Process

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Outline

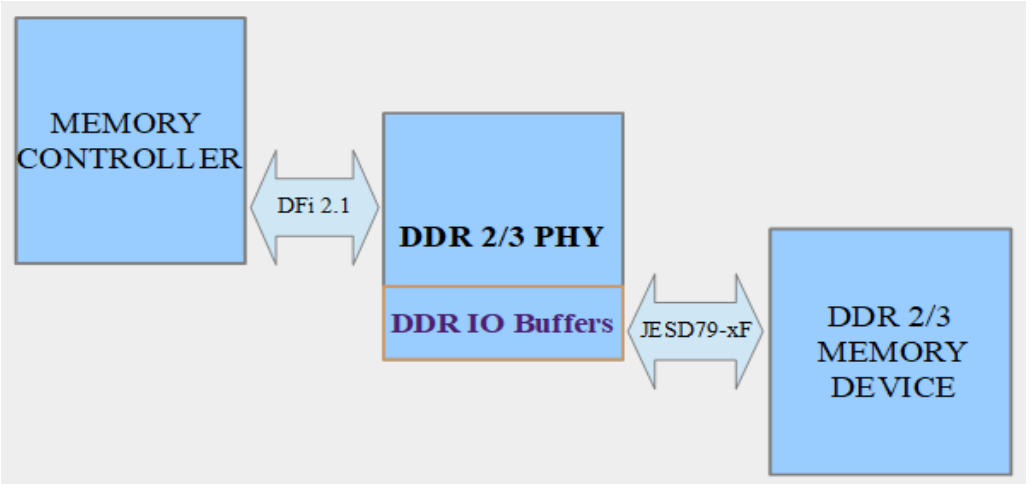
- Project facts
- DDR PHY features
- Synthesis
- Place & Route
- Radiation Hardening techniques
- Radiation Hardened I/O Library
- Radiation Hardened I/O Library for Flip-Chip applications
- Summary

Project facts

- Technology: STMicroelectronics C65SPACE 65nm.
- This development has been performed under ESA contract and the main outcome is the PHY IP and the associated I/O buffers, in classical wire-bond configuration, targeted in the hardened 65nm CMOS platform of ST Microelectronics
- In a second step, under CNES contract, the IPs have been re-engineered in order to become flip-chip compatible in the hardened 65nm CMOS platform of ST Microelectronics.

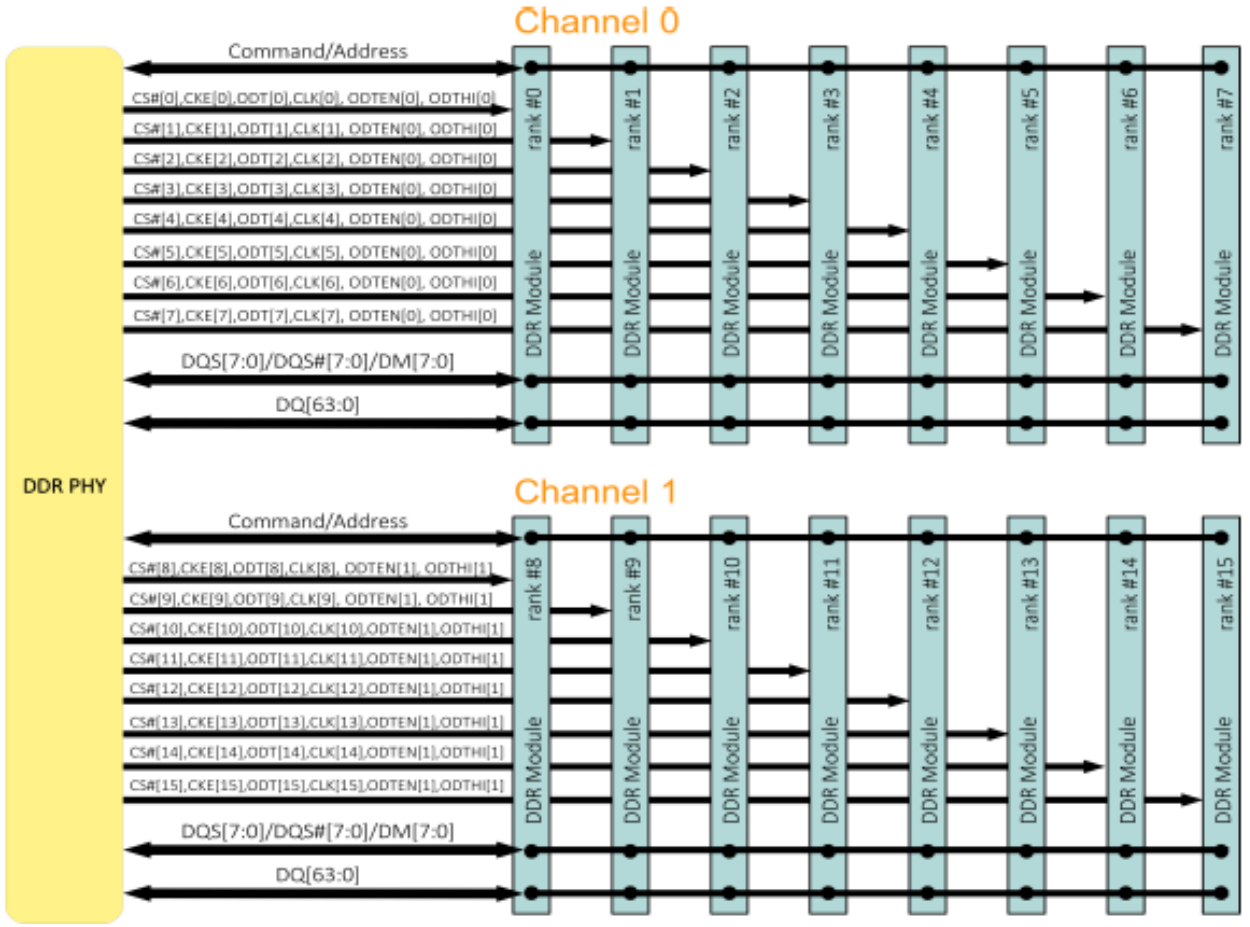
DDR PHY features (1/2)

- Supports both DDR 2 & DDR 3 memory devices (JESD-2F, JESD-3F).
- Compatible with T-branch & Fly-by topologies.
- Supports minimum data rate of 666 Mbps per data line.
- Each memory channel is independent with configurable width up to 64 bits, in increments of 8 bits.
- Up to 8 ranks (chip selects) per memory channel.
- Supports DFI 2.1.1 [RD13] interface between Memory Controller (MC) and the PHY.
- Supports DLL off operation.
- Supports dynamic On-Die Termination.



DDR PHY features (2/2)

- Supports 1:1 frequency ratio interface between MC and DFI.
- Support for 1 or 2 memory channels.
- Supports x4, x8, x16 device configuration.
- Supports Gate, Read and Write Leveling schemes.
- Supports automated or manual ZQ Calibration.
- Supports a loopback mode for high-speed test.
- Full control of the accompanied IO Buffers.

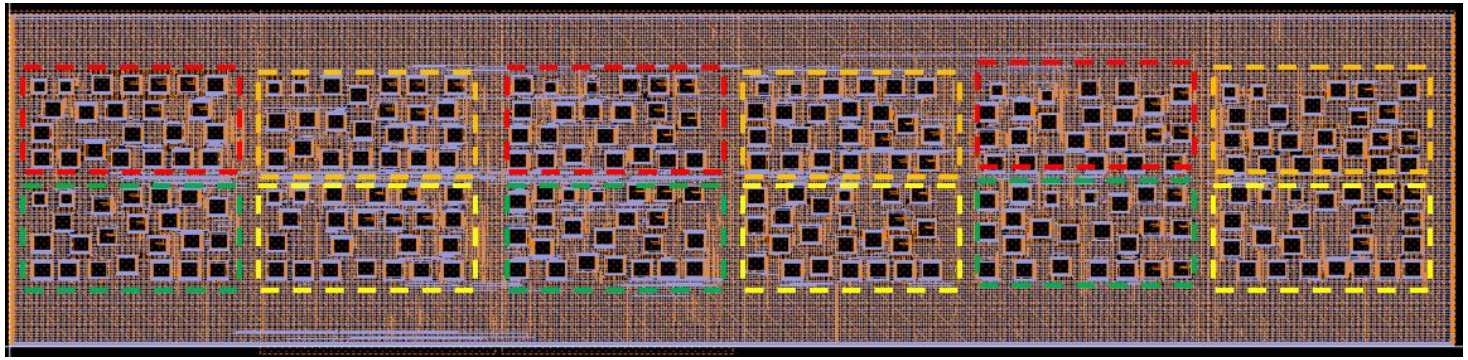


Synthesis Process

- Worst case process
- Worst case voltage (1.10V)
- Worst case temperature (125ºC)
- 20 years degradation

Only cells from STMicroelectronics' radiation hardened library "SKYROB" were used.

The synthesis process of PHY is done in hierarchical mode.

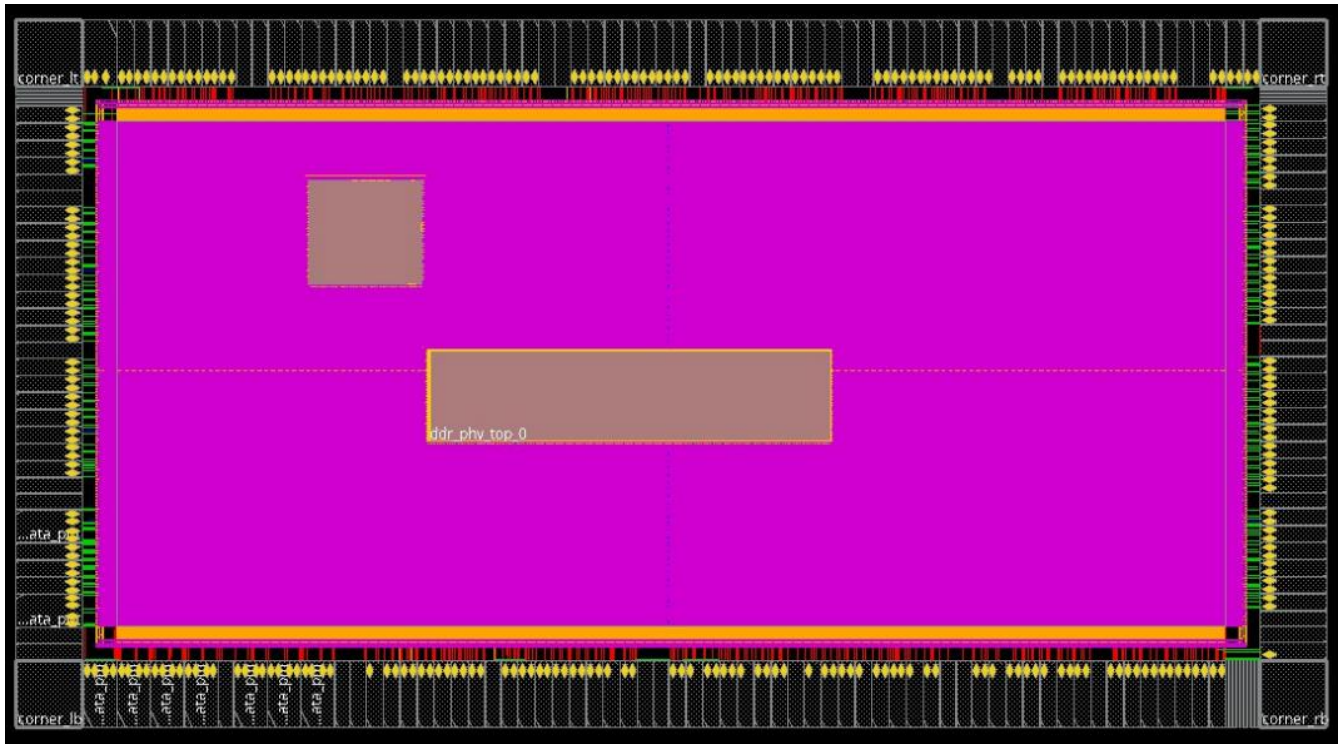


Place & Route

- Floor planning
- I/O placement (from hardened I/O linrary)
- Special net routing
- Clock tree synthesis

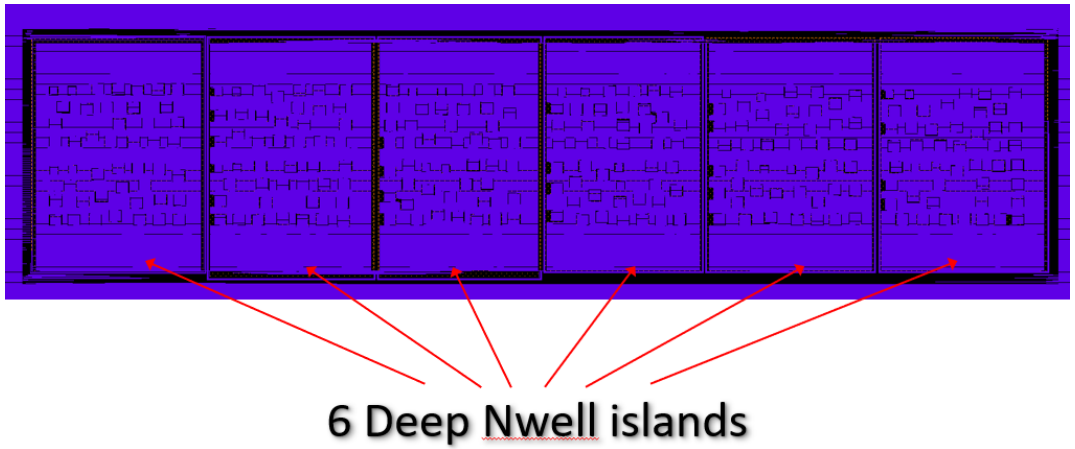
Timings analysis performed at end of each stage with extreme case conditions:

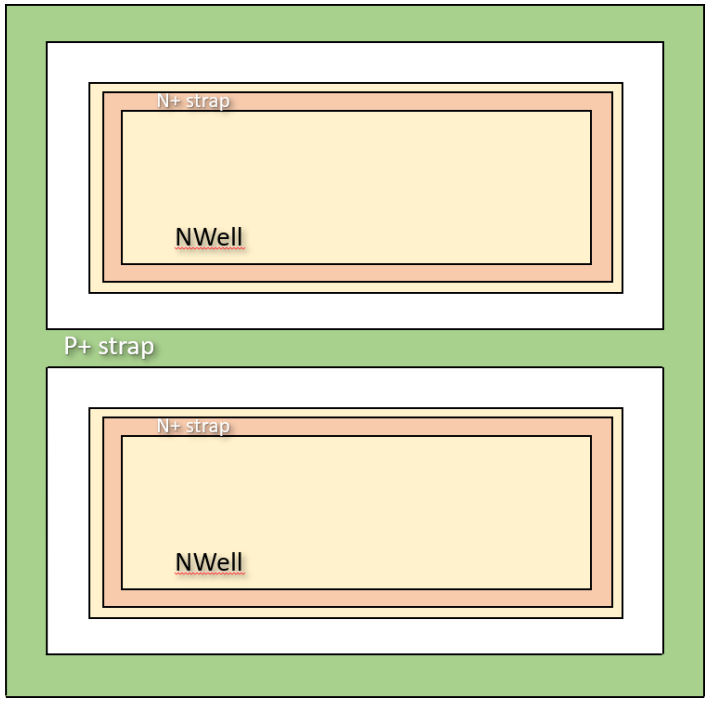
- 1.10V @ 125ºC with 20 years aging factor
- 1.30V @ -40ºC



Radiation Hardening Techniques (1/2)

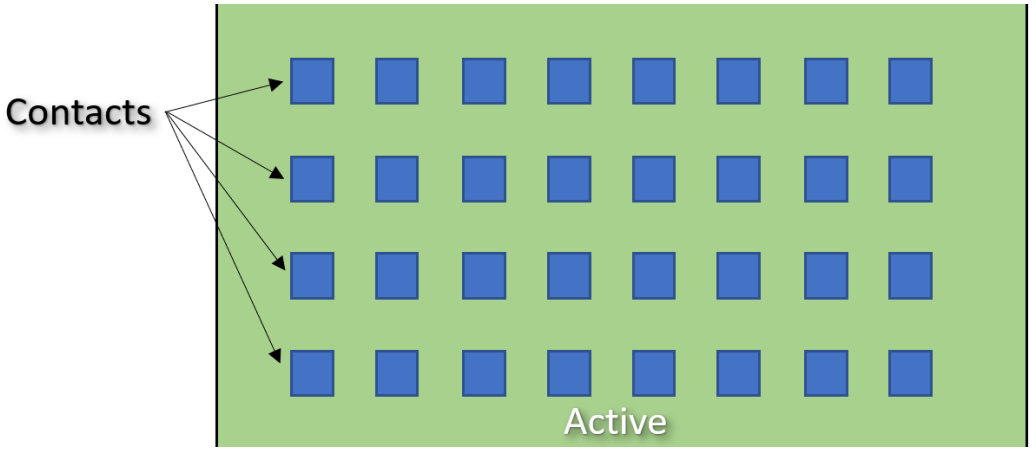
- All active devices are over Deep N Well (DNW) islands
- Small DNW islands created
- All DNW regions fully enclosed by p+ guard rings.
- Each DNW island has a continuous strap at its edge

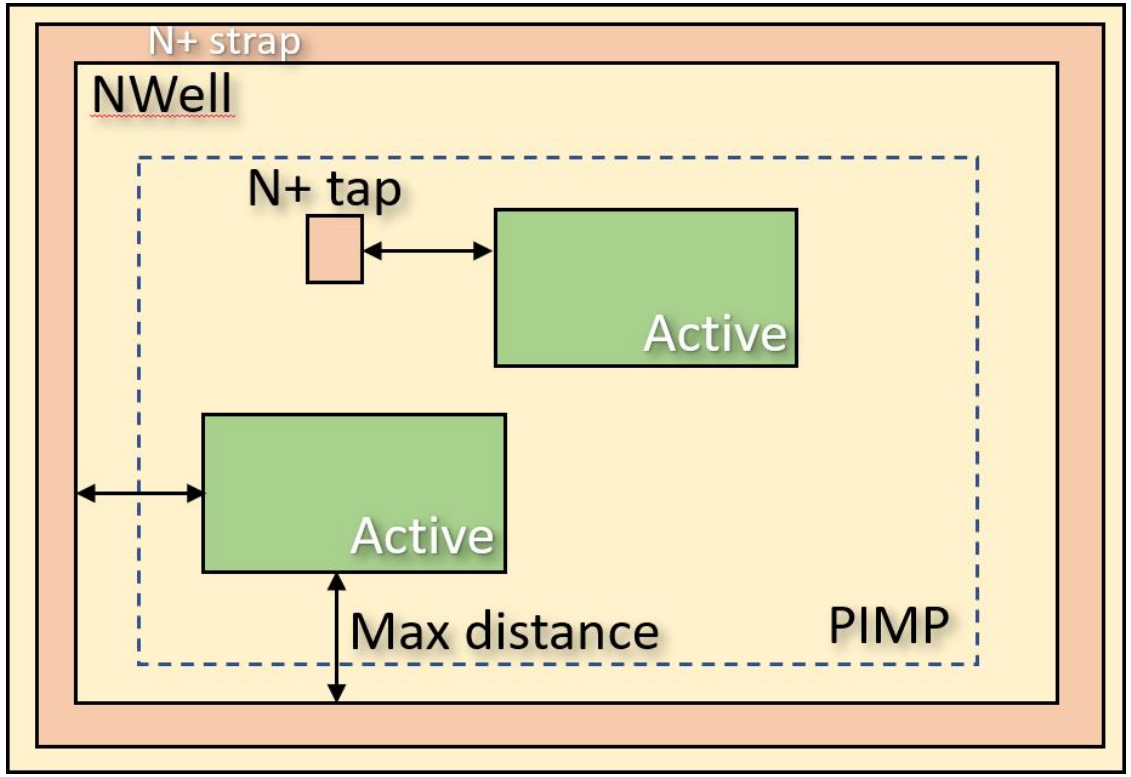




Radiation Hardening Techniques (2/2)

- Straps and taps are placed as close as possible to active devices
- Guard rings with highest possible number of contacts and highest possible width

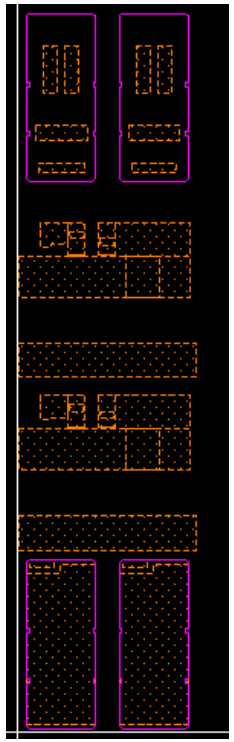




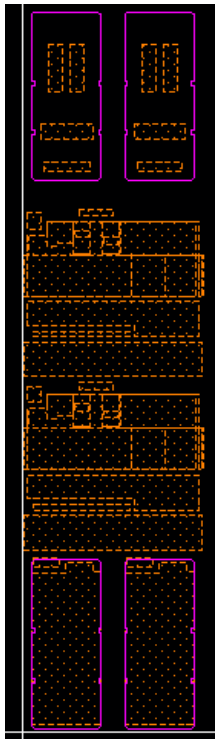
Radiation Hardened I/O Library

- The STMicroelectronics' non-radiation hardened library for DDR was used as starting base and applied revised latch-up rules.
- New developed I/O have same dimensions and pin placement

Non-Hardened I/O

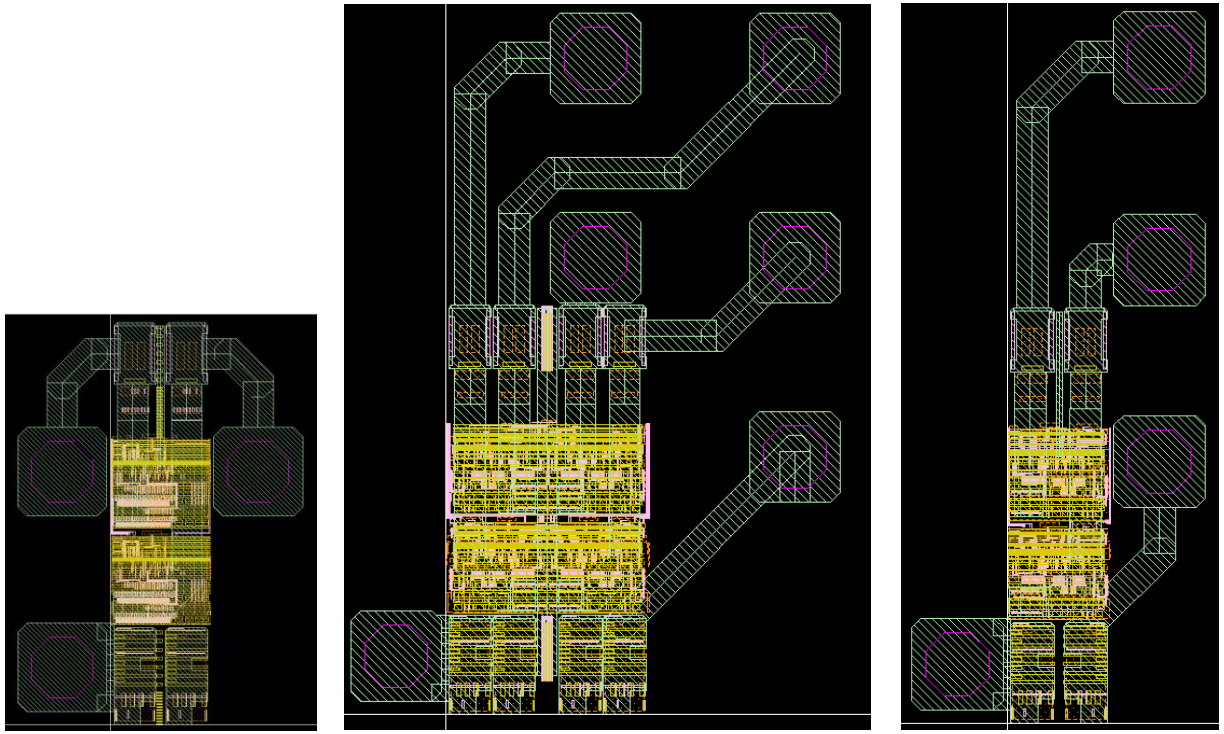


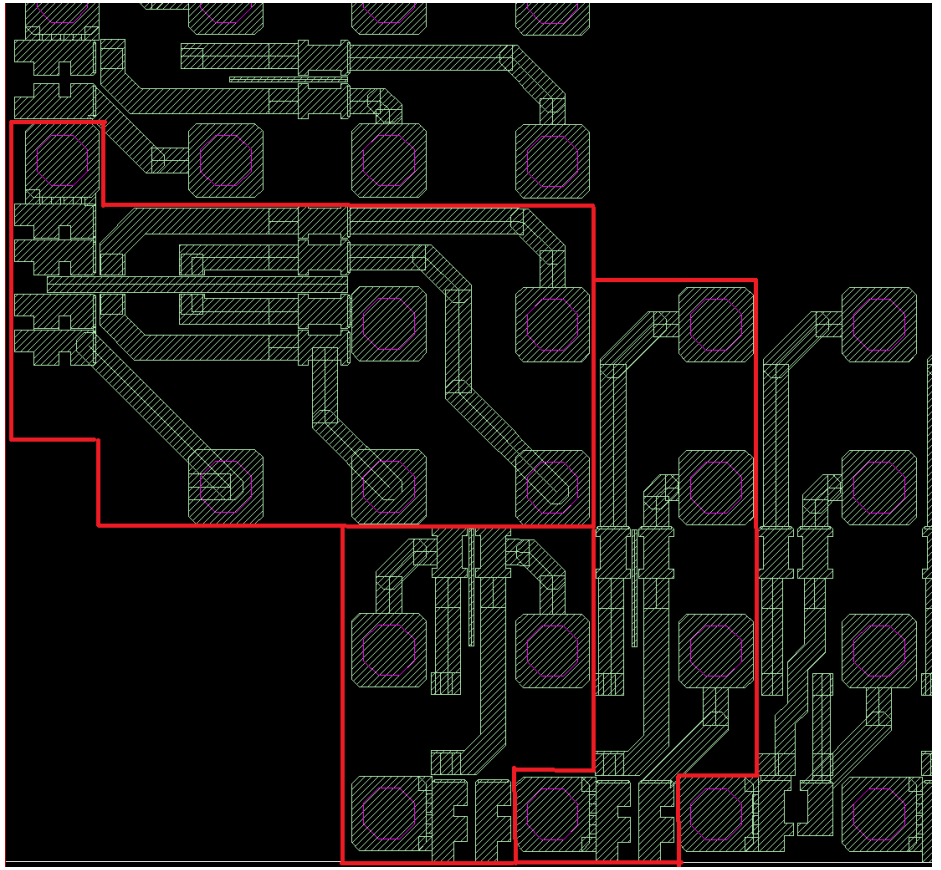
Hardening techniques



Radiation Hardened I/O Library for Flip Chip applications

- Bumps openings as close as possible to the ESD protection diodes
- Bumps placed in 225µm array
- Extra flavour of I/Os for next to corner placement





Summary

- **A radiation hardened PHY for DDR2/3 has been designed**
- **A radiation hardened I/O library is available for DDR2/3 for classical wire bond and Flip-Chip applications**
- **The radiation characteristics of the PHY will be communicated as soon as they become available**

Thank you for your attention!

Questions?