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SLIME

Radhard Clockless I2C Slave for space application

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weeroc

High-end Microelectronics Design

SYSTEM CERTIFICATION ISO 9001 SGS

About Weeroc

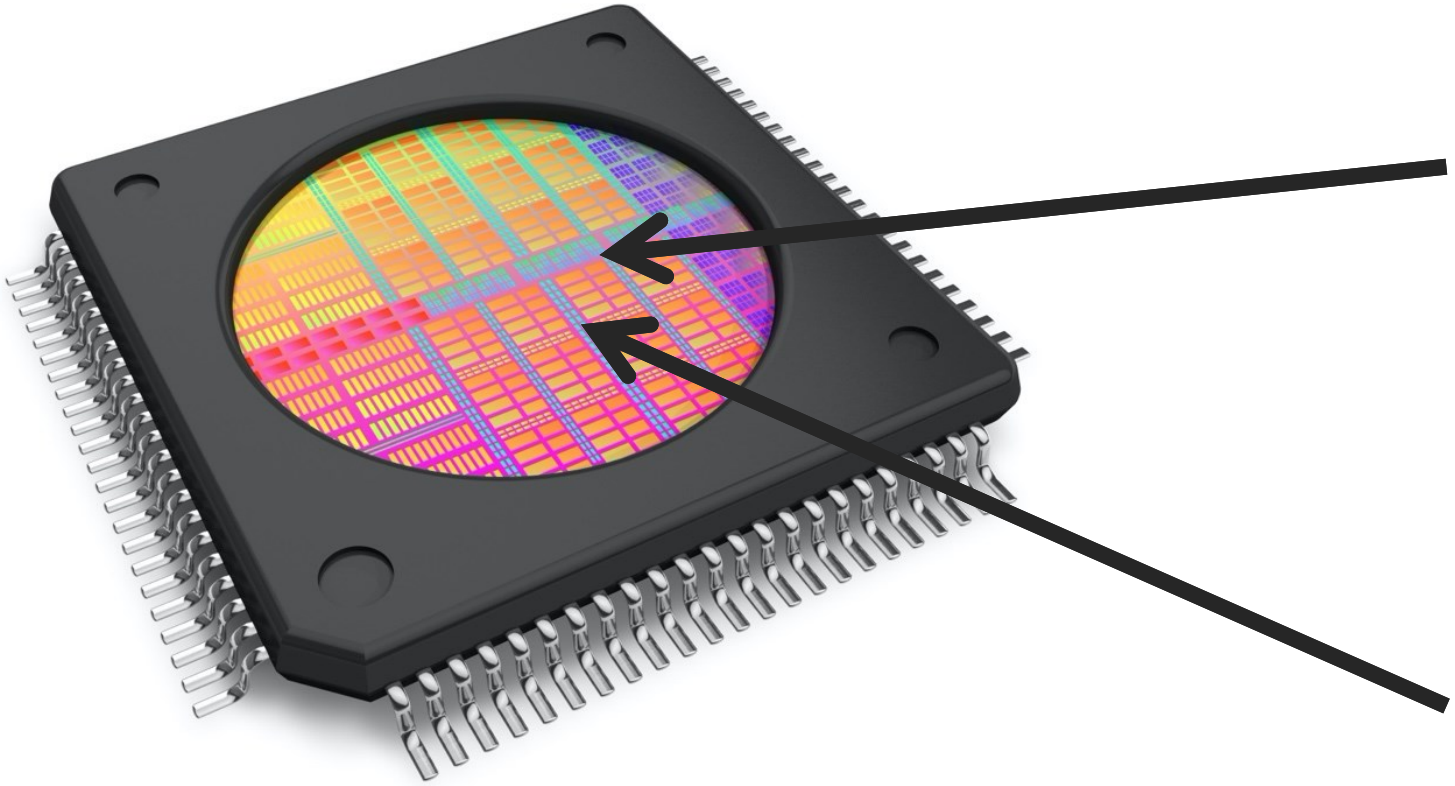
- Fabless semiconductor company
  - We build requirement specification with customers
  - We design and produce ASIC
  - We sell validated and tested ASIC
  - We help integration of our ASIC with our application engineer
  - We design systems using our ASICs
- French Start-up company issued from IN2P3

  IN2P3 : French National Institute for Nuclear Physics and Particle Physics
- Created February 2012 → 10-year old
- ISO9001 certified

Weeroc Activity &Expertise

Design and sell Analogue & mixed microelectronics ASIC
to read-out photodetectors and particle detectors

and for radhard application

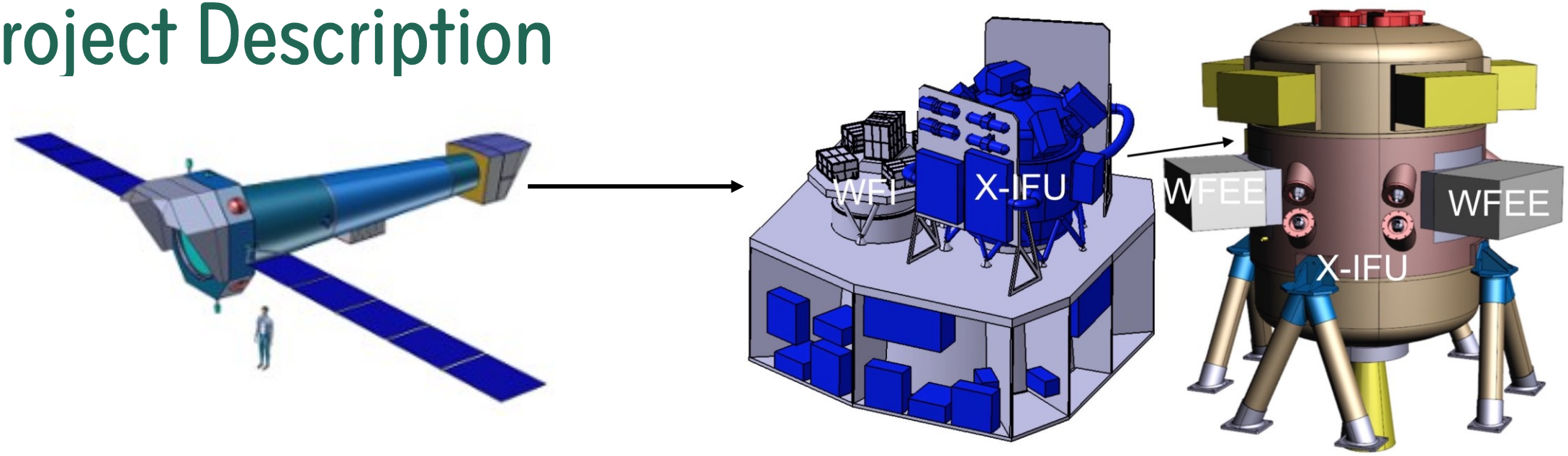


Radhard design

Low-noise, low power, analogue and mixed signal circuits

Particle detection

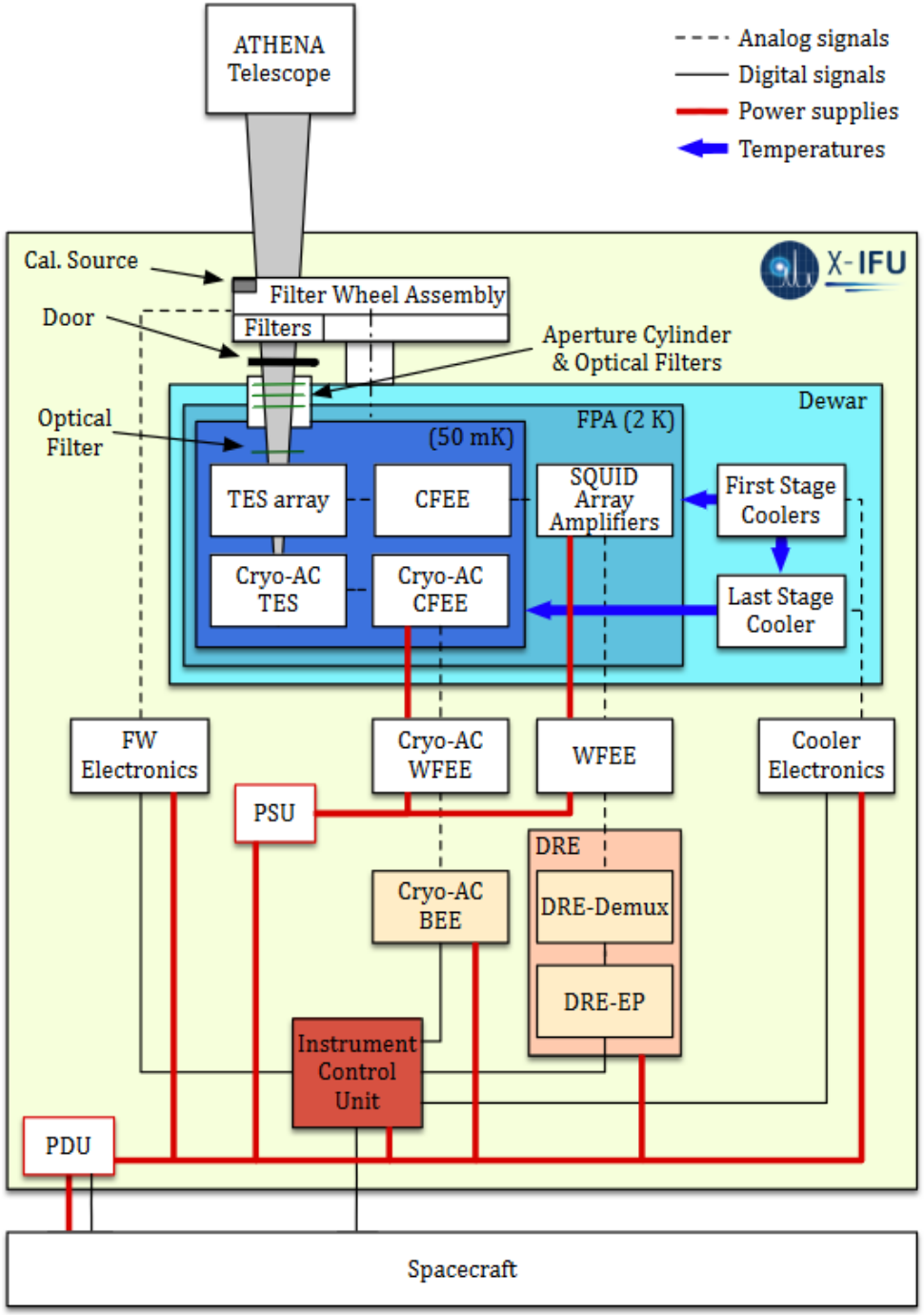
Project Description



- ATHENA: Advanced Telescope for High ENergy Astrophysics
  - Space science program of the European Space Agency (ESA) for the X-ray observatory, launch planned 2031 with a life time of 4 years
- XFEE AwaXe
  - X-ray Integral Field Unit ATHENA Warm ASIC for the X-IFU Electronics

SLIME requirements

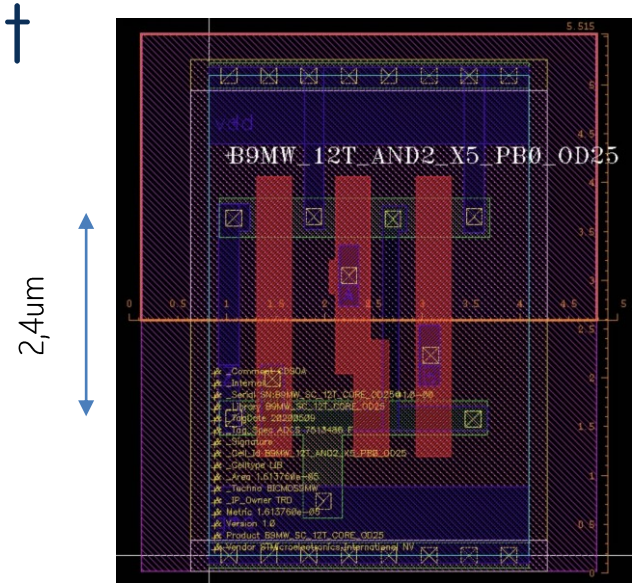
- In the WFEE
- Configuration of SQUIDS/TES
  - Supraconducting detector
  - 50 mK
- Low noise -> clockless
- Config stored for a few days
  - Triplication
- Custom RadHard



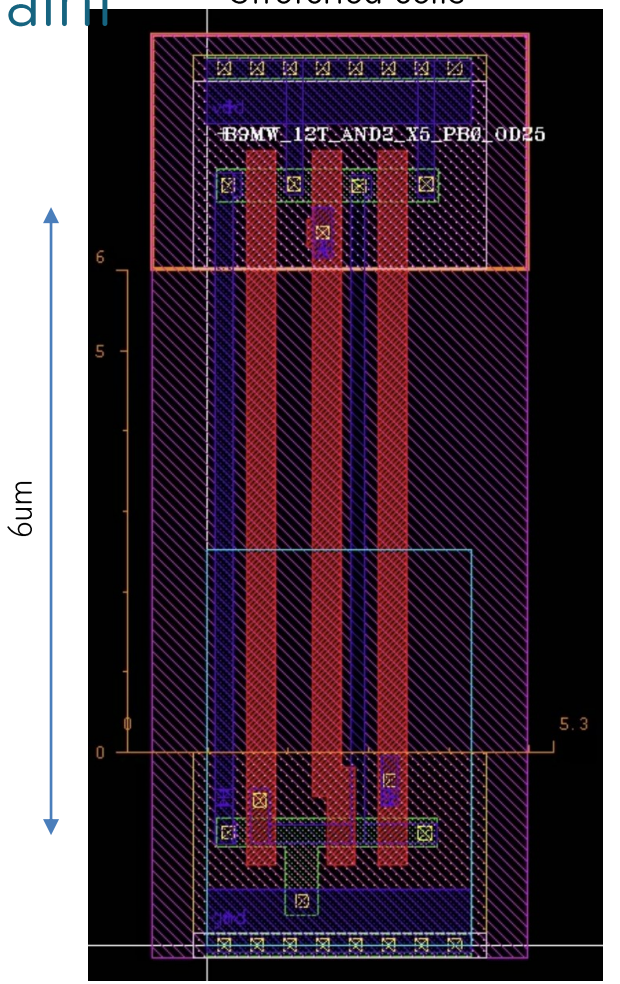
RadHard Digital Library Dev

- ST Microelectronic BiCMOS 130 nm (B9MW)
  - Bipolar transitor required for the low noise constraint
- P+/N+ separation to avoid Latch-up
  - 60 MeV.cm2/mg SEL
- TID : 20 kRad tolerant

Original standard cells

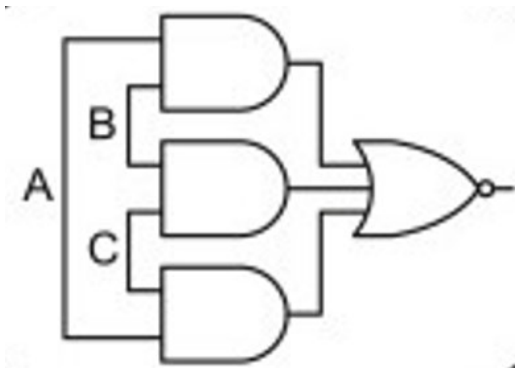


Stretched cells



Configuration register SEU protection

- Configuration registers written every few days
  - TMR only on register
- No internal clock
  - No auto-correction
  - Latched SEU flag to inform master of data corruption
  - Correction will be done at the next write procedure

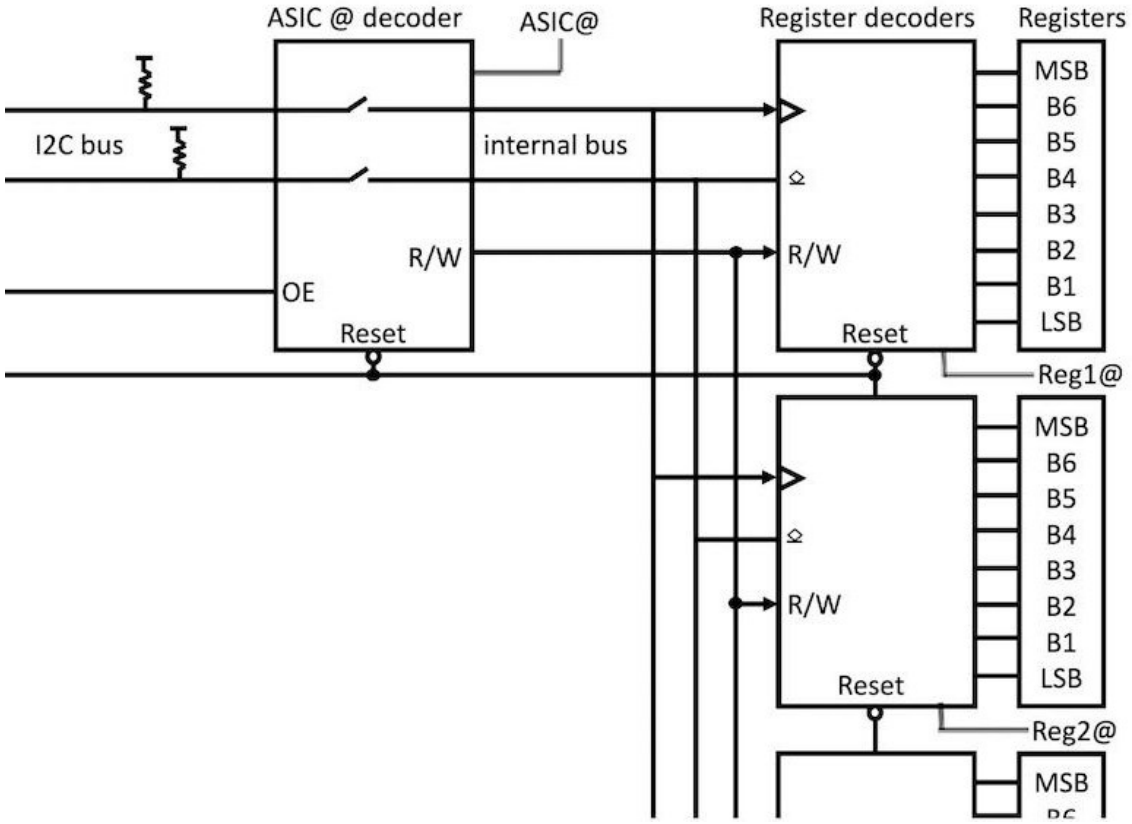


Protocol

- Standard I2C protocol, but…
- Too many devices to fit into I2C address space.
  - The first byte of data is used as an extra address byte.
  - For each ASIC@, there is a sub-module with its own bus.

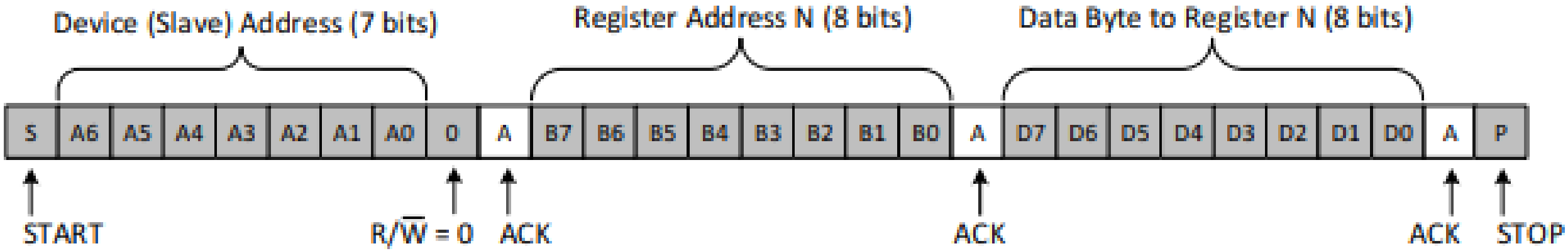
Bus separation

- The device is split into two parts : ASIC@ and REG@.
  - This limits number of active devices.
- The address decoder reads the ASIC@ and disconnects sub-bus if not selected.
- The register stores DATA.



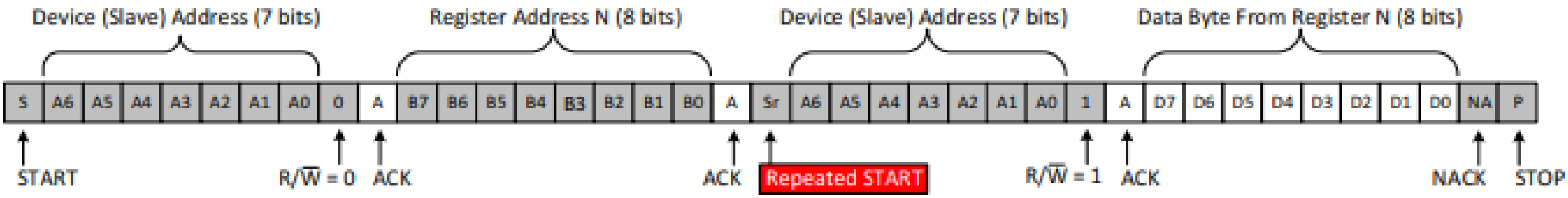
I2C write

- Normal frame when writing : [ASIC@ + REG@ + DATA].



I2C Read

- When reading, the last used register responds.
- Normal frame when reading : [ASIC@+ REG@][ASIC@+ DATA]



Clockless device

- No internal oscillator to reduce power usage and noise.
  - State machines clocked on SCL.
  - START, STOP asserted asynchronously, and used as synchronous reset for the state machines.
  - Device completely quiescent when bus inactive.
  - Auto-correction not safe for data integrity

What Next

- Currently in the Place&Route step
- Mixed-Simulations underway
- Tape-out of digital test vehicle end of June
- Irradiation campaign

Thank you

Thank you

Thank you

Thank you

Thank you