Accomplishing PROMISE, PROgrammable MIxed Signal ASIC Electronics Framework

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Topic:

Analogue intellectual property and re-usability of analogue circuits in space

Radiation-hardened technologies for analogue ICs

PROMISE project, started at the beginning of 2020, has lived by now more than 2 years of harsh but exciting times of successful microelectronics developments. It has crossed by now the equator of its lifetime. During this time most of the IPs have pass a successful CDR, and the CDR of the Pilot Circuit ASIC, integrating all the IPs, is expected by April this year.

The PROMISE project gathers IC experts from 7 European institutions. This project has received funding from the European Union's Horizon 2020 research and innovation program under grant agreement No 870358. It was launched in early 2020 and is planned to run for a total of 4 years. PROMISE stands for PROgrammable MIxed Signal Electronics. It's tailored to bring a flexible mixed-signal ASIC architecture design ecosystem built on a portfolio of silicon qualified hardened IP blocks to the space community. Moreover, the project is intended to provide a flexible mixed-signal ASIC manufacturing and qualification ecosystem. Last but not the least, PROMISE will deliver IP dissemination, commercialization and intellectual property management to allow efficient reuse of the project's outcomes by all the space community, and will provide a full European design environment for new IPs and mid-range ASIC for space applications.

The PROMISE project objectives are to optimize the design cost, shorten schedule and de-risk analogue and mixed ASIC radhard design, manufacturing and qualification according to the needs of the space industry. PROMISE, led by Thales Alenia Space, encompasses diverse European partners, subcontractors, potential users or solution providers, all top actors of the European Mixed Signal ASIC ecosystem. The partners involved are: TASiS (in Spain who leads the project), top level SMEs as ISD (Greece) and MENTA (France), key technological institutes such as IMEC (Belgium), IT (Portugal) and VTT (Finland); and a leading satellite manufacturer as Thales Alenia Space in France.

PROMISE is based on a modular architecture built on the DARE180X/XFAB XH018 0.18 micron Mixed Signal HV CMOS Technology that allows the end users to target both simple and complex applications of Mixed-Signal ASICs such as signal conditioning and acquisition, motion control, signal processing, signal synthesis and others. This architecture pivots around a central eFPGA module that provides extra flexibility during the lifetime of the mixed-signal ASIC.

PROMISE has designed an IP library oriented towards the fast design of mixed-signal ASICs by the suitable aggregation of pre-validated modules with the minimum added specific circuitry. It enables mixed-signal ASIC and ASSP approach. IP reuse will ensure a shortest and secured schedule and de-risk the design hardening for mixed-signal ASIC/ASSP.

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The first population for this library, includes a set of Radiation hardened and reusable analogue, high voltage and digital IPs that covers the most common functions for data acquisition, conditioning, processing and control. This initial portfolio of IPs includes the following functions:

- Digital IPs: Standard digital cells ; Standard digital IOs; Non-Volatile Memory (NVM); Embedded Field Programmable Gate Array (eFPGA) core.
- Analogue IPs: Analogue to Digital Converter (ADC); Digital to Analogue Converter (DAC); Phase Locked Loop (PLL); Low Drop Out (LDO) for digital core; BandGap (BG) with second order temperature compensation; Local Oscillator (LO) with no external component; Power On Reset (POR); High Voltage MOS transistors (HV).

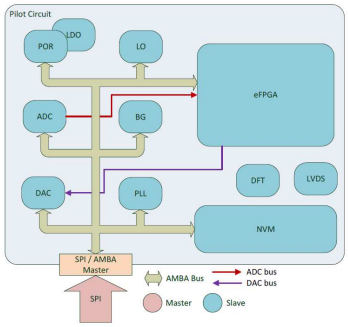
Those IPs are embedded in the Pilot Circuit ASIC for electrical performances and radiation tests. The tests will provide:

- Measured Electrical compliance of the IP blocks through the electrical validation of the Pilot Circuit;
- Get the electrical Safe Operating Area for high Voltage MOS;
- Evaluated Radiation hardness of the IP blocks through the radiation evaluation on the Pilot Circuit.

All IPs shall be compliant with the radiation requirements defined within the project. The target radiation performances to be tested on a PILOT Circuit ASIC are as follows:

- TID: > 100 Krads
- SEL: LET > 60 Mev.cm^2/mg
- SEFI: LET > 60 Mev.cm^2/mg
- SEU: < 10^{-8} event/day/bit

The Pilot Circuit Block diagram is depicted in the figure below:



The ASIC Floor Plan is shown in the figure below. The chip size is limited by the MLM reticle: 21mm x 11mm. The package will be a CQFP-352.

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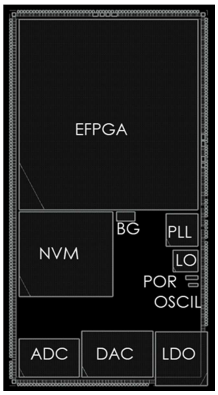

During the conference, the details of the current status of the PROMISE project will be presented, along the planned Electrical and Radiation Testing to be performed after Pilot Circuit ASIC Manufacturing.

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