Accomplishing PROMISE, PROgrammable MIxed Signal ASIC Electronics Framework

AMICSA - June 2nd, 2022

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This project has received funding from the EU Horizon 2020 research and innovation programme under grant agreement No 870358

Agenda

1. PROMISE Project Introduction
2. Pilot Circuit ASIC Architecture and Status
3. IP Library Overview and status
4. Planned Activities
5. Conclusions

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PROMISE Project Introduction

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PROMISE Consortium

- **7 Institutions**
- **6 European countries**
  - Main user (TAS in France and TAS in Spain)
  - Library and IP provider (IMEC)
  - Several IP providers (MENTA, IT, VTT and ISD).
- **Well balanced:**
  - 2 Large Enterprises
  - 1 Academic partner
  - 3 SMEs
  - 1 Research center
- **One Goal: All-European Mixed-signal ASIC for Space applications**

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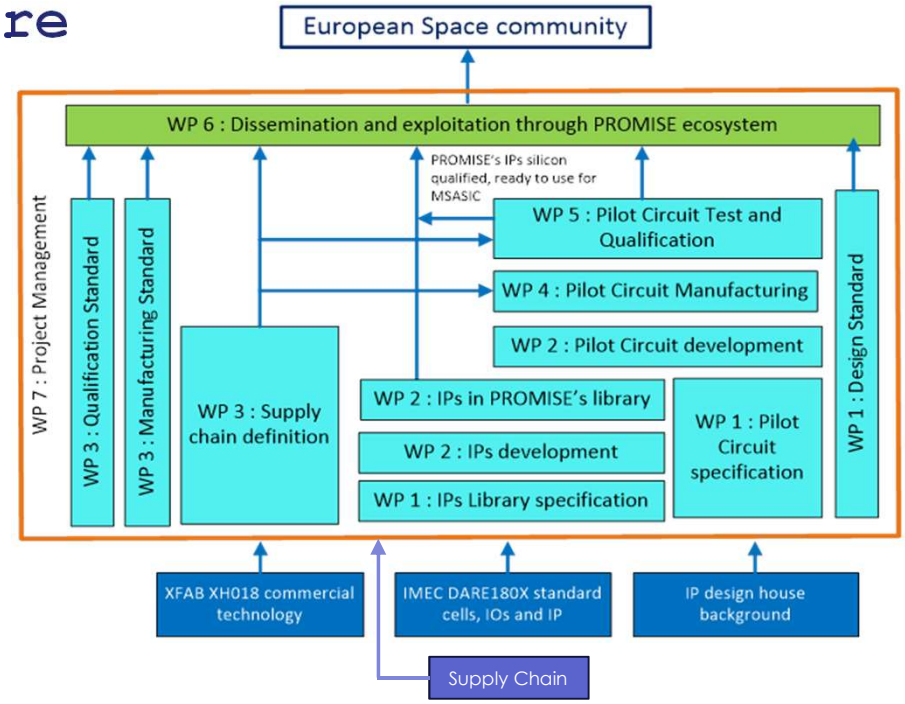
PROMISE Project Structure

- **7 Work Packages led by TAS in Spain, TAS in France, ISD and IMEC**
  - **5 of them technical**
  - **WP6 dedicated to dissemination, communication and exploitation**
  - **Overall project coordination driven from WP7**
    - Project management and Technical coordination
  - **Started in January 2020**
    - Duration: 4 years
  - **PROMISE Webpage:**
    - https://promise-h2020.eu/



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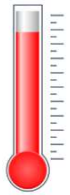
Mission profile

- ✓ **Supplies :**
  - ✓ Low voltage (Digital Core and analog) power supply : 1.8V +/-10%
  - ✓ Digital IOs and Analog power supply : 3V3 -5%/+10%

- ✓ **Junction temperature :**
  - ✓ TJfuncmin=–40°C and TJfuncmax=125°C
  - ✓ TJperfmin=-20°C and TJperfmax=+105°C



- ✓ **Life Time :**
  - ✓ Based on XFAB corners and derating curves : 100khours
  - ✓ No ageing model available

- ✓ **TID :**
  - ✓ 100 krad (tested at low dose rate between 36Rad(Si)/h and 360Rad(Si)/h)

- ✓ **SEE :**
  - ✓ SEL, MBU and SEFI immune up to a LET of 60MeV.cm²/mg at the maximum functional temperature
  - ✓ SEU rate goal less than 10-8 Ev/day/FF (or memory point)
  - ✓ SET error rate at IP level shall be less than 10-8 Ev/day/block on GEO orbit

- ✓ **HV features**
  - ✓ Evaluation for SEGR and SEB safe operating area up to a LET of 60MeV.cm²/mg

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Pilot Circuit Architecture & Status

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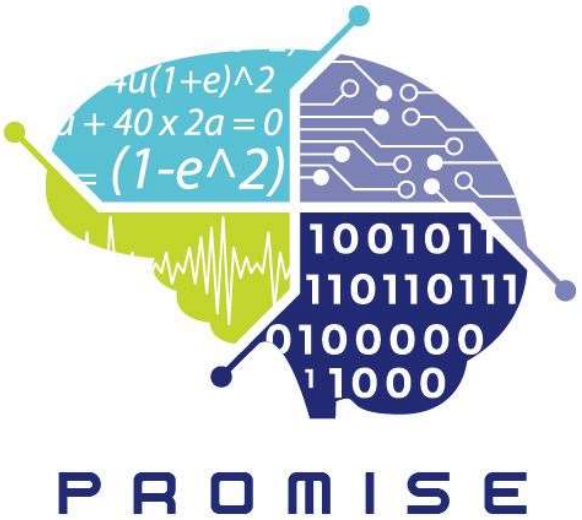
Pilot Circuit Purpose

- ✓ **Design a circuit to integrate IPs designed during PROMISE project**
- ✓ **Support electrical and radiation tests**
  - ✓ For design validation
  - ✓ For silicon qualification
- ✓ **To made qualified and validated IPs available and reusable for the European Space community**



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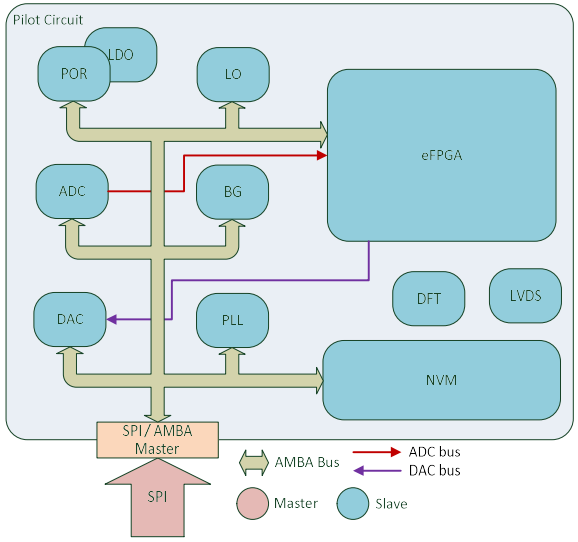
Top level functionalities

- ✓ **POR, BG, LDO and LO for safe powerup of the Pilot Circuit.**
- ✓ **Analog ressources : DAC, ADC**
- ✓ **Standard AMBA bus.**
- ✓ **Digital core and PLL**



- ✓ Hardened Standard Cells (LP and LVT)
- ✓ I/O and Bondpads
- ✓ **eFPGA + NVM, the core of ASSP**
- ✓ HV features test structure
- ✓ Specific test structure for LVDS transceivers
- ✓ **NVM for eFPGA bitstream and configuration.**

- ✓ Analog DFT : monitoring analog by multiplexor accessible through SPI in test mode.
- ✓ Digital DFT (SCAN and JTAG) : covers all digital blocks and eFPGA.

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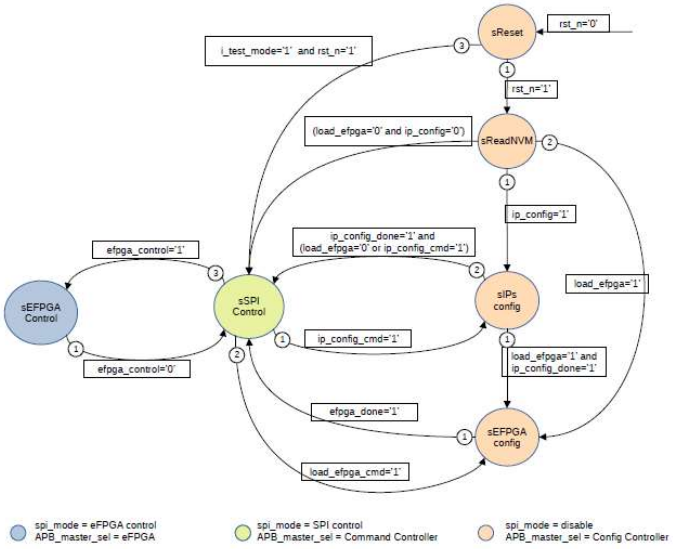
Functional modes

Inputs	125
Outputs	102
Macros	9
Sequential cells	3050
Combinational cells	10319
Scan Chains (~length)	8 (500)
Scan Flip-Flops	3002
ATPG Stuck-at-Faults (coverage)	86288 (95%)
Clock domains	16
Main operating frequency	16MHz



I_EXTERN_CFG_<1:0>	Mode	Comments
00	Normal	eFPGA IO's are routed to external IO pads
01	External eFPGA configuration	eFPGA config signals are routed to external IO pads
10	External NVM programming	NVM programming signals are routed to external pads
11	LVDS RX Fail-Safe status	Output LVDS RX fail-safe status

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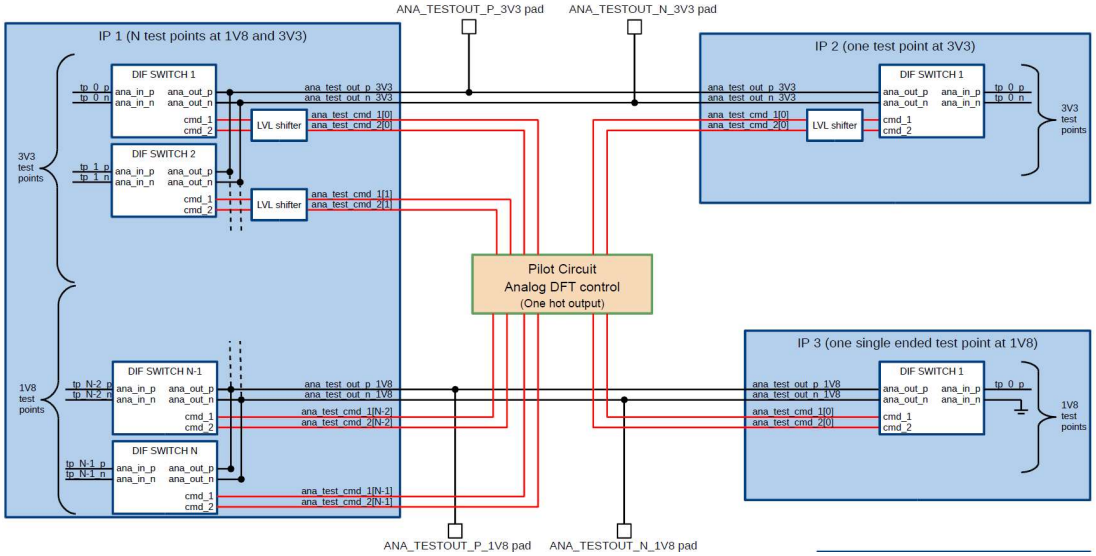
Analog & Digital DFT strategy



Each blue box represents an IP.
All schematics inside a blue box must be implemented inside the corresponding IP.

*** NVM has specific signals for Analog DFT**

DFT Modes

TI_TEST_MODE[2:0]	Mode
000	Functional
001	Test-mode
010	Scan-mode pilot circuit
011	Scan-mode eFPGA compressed
101	Scan-mode eFPGA uncompressed
100	Boundary Scan

- Each IP / TOP has its own SCAN interface:
  - Scan-mode, scan-en are common
- ATPG patterns are generated for each IP / TOP independently
- 8 scan-chains: each ~ 500 flops
- ATE clock frequency:10MHz

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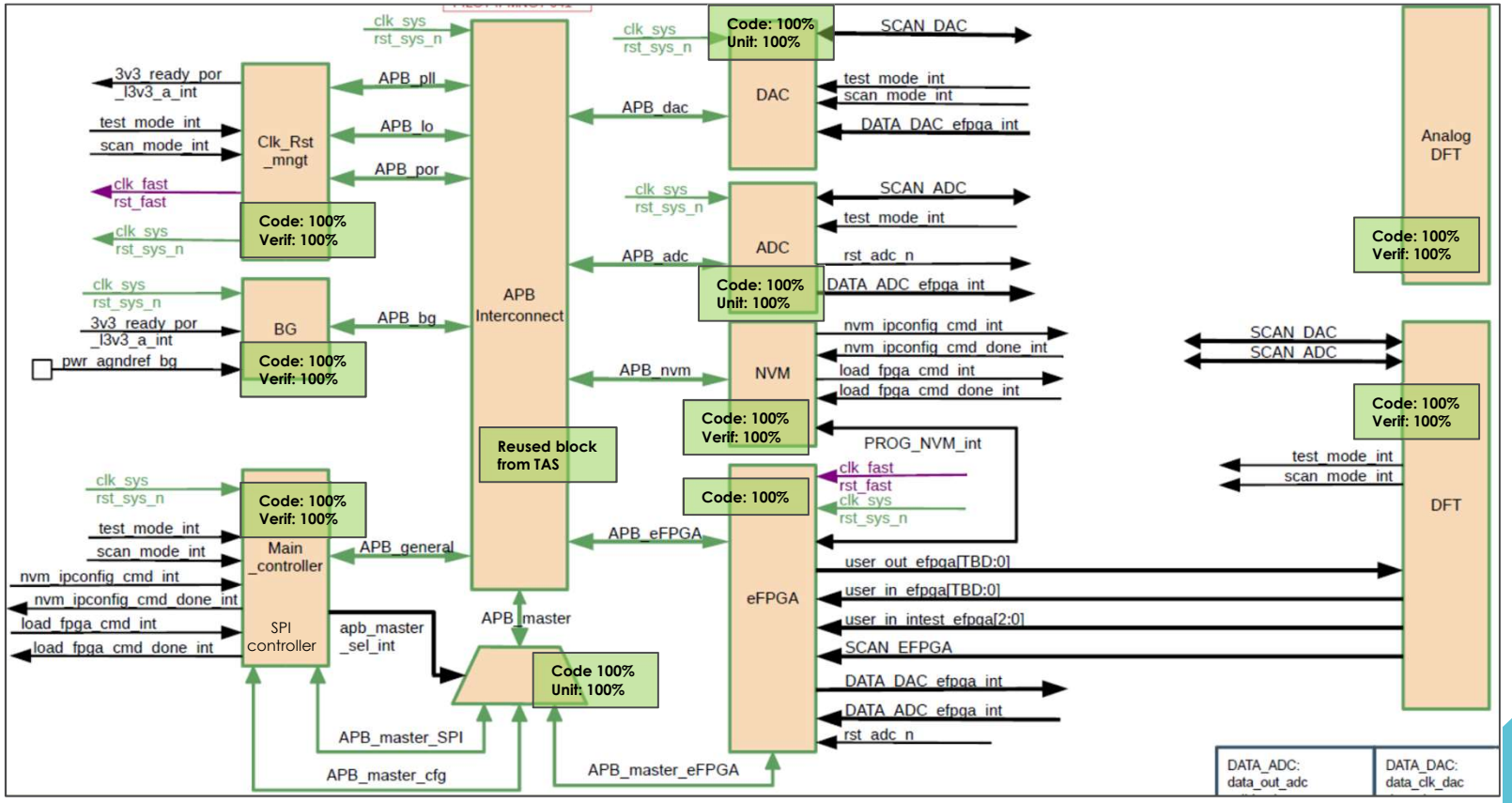
Status

Overall
Code: 100%
Verif: 100%



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IP Library
Overview & Status

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IP eFPGA ID card

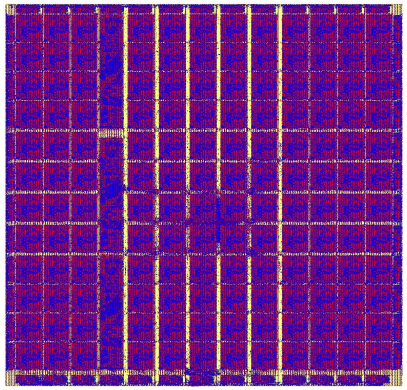
Functional description

- eFPGA IP of ~1750 LC + 3 DSP similar to **Microsemi RTSX32**
- Radiation-hardened
- Based on DARE180X heritage and PROMISE rad-hard standard cells from IMEC
- Specific radiation hardened cells to improve density
- Origami Programmer: Menta state-of-the-art eFPGA EDA RTL to bitstream tool

Main characteristics

- **Equivalent number of logical cells = 1751**
- **Number of DSP : 3 DSP**
- **Pre-adder/Multiplier size : 24 bit**
- **DSP ALU size 48 bits**
- **Number of clocks : 3**

eFPGA IP architecture



eFPGA IP layout

Layout characteristics

- **Silicon area : 8.98 mmX10,12 mm=90.88 mm²**
- **Consumption : bitstream dependant**
- **Static Power : 1 mW**
- **Number of IOs : 391/395 (IN/OUT)**

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IP NVM ID card

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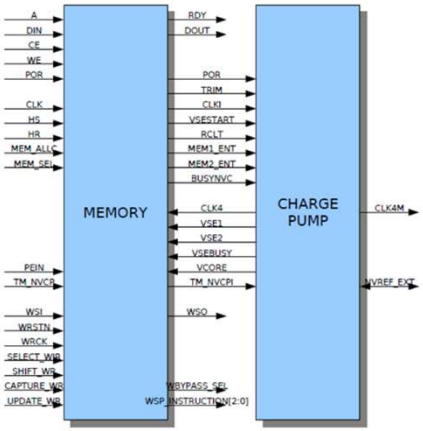
Functional description

- XFAB NVM in XH018 based on SONOS Flash technology
- The Non-Volatile Memory will store the eFPGA bitstream. It can also be used to support the design performance tuning (bandgap voltage, LDO voltage for example) and the circuit configuration..

Main Performances

- NVM size is 64blocks*256words*32bits.
- input clock frequency of 16MHz +/- 10%.
- total current consumption goal < 50 mA
- DVDD=1.8V ±10%, AVDD=3.3V ±10%.



Word, bits	32
Number of Data Words	256x42
Total Number of Words	256x44
Page, Words	8
Pages per Sector	32
Number of Sectors	42+2 inactive
Memory banks,	2
Sectors per Memory Bank	21+1
ECC Bits per Word	8
Total Amount of Memory, bits	360448
Synchronous Parallel Interface	Yes
Data I/O Width, bits	32

Layout characteristics

- Silicon area : 4.5 mm X 5.7 mm = 25.65 mm²

SCHEMATIC NETLIST → LAYOUT → CDR → DATA PACKAGE

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IP ADC ID card

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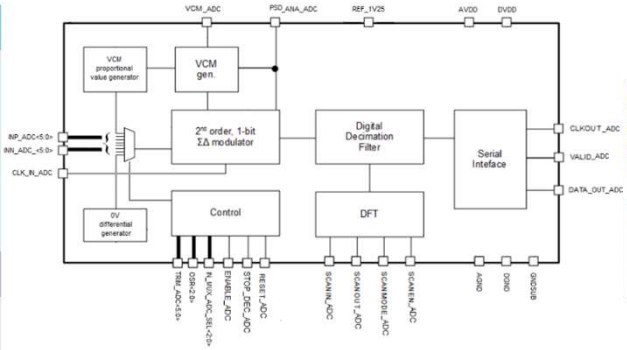
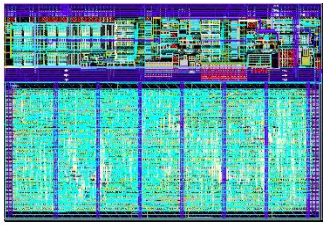
Functional description

- 1-bit ΣΔ architecture
- Differential or single-ended input drive mode
- Trimmable Full Scale Voltage
- Selectable Over-Sampling Ratios





Main Performances

- Sampling rate up to 234 kSps
- Bandwidth from DC up to 50 kHz
- Conversion latency 1.4 ms
- ENOB > 17 bit @ low sampling rates

Layout characteristics

- Silicon area : 3.03mm X 2.04mm = 6.18mm²
- Consumption : 14 mA
- Power : 44.7 mW
- Number of IOs : 39

SCHEMATIC NETLIST → LAYOUT → CDR → DATA PACKAGE

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IP DAC ID card

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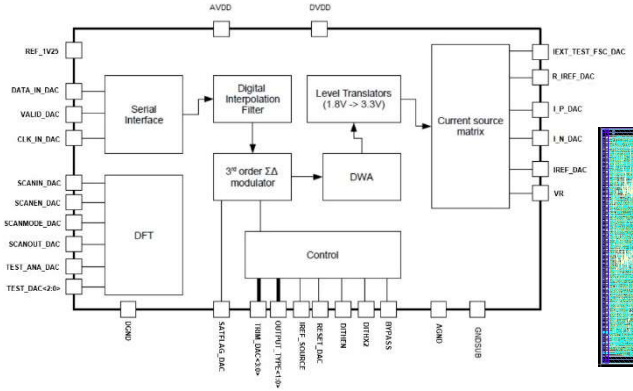
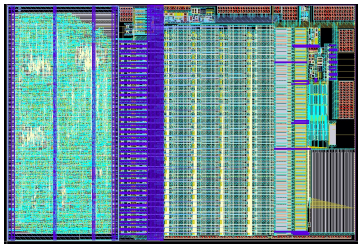
Functional description

- Differential current steering output
- Simple serial input interface
- Trimmable Full Scale Current (5.5mA)
- Selectable Over-Sampling Ratios
- Embedded or external reference

Main Performances

- INL 1 LSB, DNL 0.33 LSB
- Thermal drift 52 ppm/°C
- PSRR > 60 db
- Conversion latency < 4 ms





Layout characteristics

- Silicon area : 3.7 mm X 2.5 mm = 9.25 mm²
- Consumption : 9.4 mA
- Power : 29.52 mW
- Number of IOs : 37

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Status

- ✓ **90% done**
- ✓ **80% CDR done**

IP	SRR (Spec review)	PDR (architecture, schematic and simulation plan)	DDR (Final schematic, simulation at schematic level done)	Layout review	CDR
HVMOS	Done	Done	Done	Done	Done
NVM	Done	Done	Done		
Standard cells	Done	Done	Done	Done	Done
POC	Done	Done	Done	Done	Done
Level shifters	Done	Done	Done	Done	Done
IOs	Done	Done	Done	Done	Done
LVDS	Done	Done	Done	Done	Done
POR	Done	Done	Done	Done	Done
BANDGAP	Done	Done	Done	Done	Done
LO	Done	Done	Done	Done	Done
ADC	Done	Done	Done	Done	
DAC	Done	Done	Done	Done	Done
PLL	Done	Done	Done	Done	Done
LDO	Done	Done	Done	Done	Done
eFPGA	Done	Done	Done	Done	Done
Pilot Circuit	Done	Done	Done		

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PROMISE Project
Planned Activities

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Pilot Circuit Test and Qualification

Final step of the design, production and validation chain

- ❑ Electrical, radiation and silicon qualification tests on the Pilot Circuit
- ❑ Assess the space worthiness of the Pilot Circuit
- ❑ Provide silicon qualification status of PROMISE IPs

Task 5.1**: Test Board Design and Manufacturing** - **IN PROGRESS**

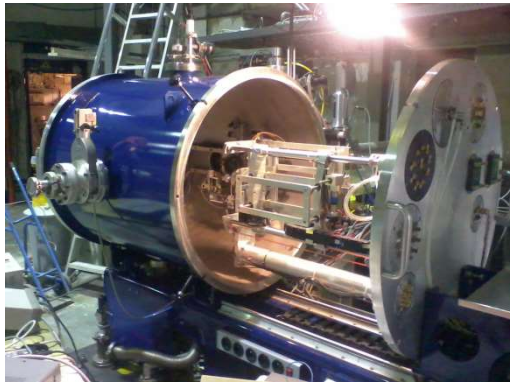
Development of Test setup: all the elements of the ASIC and measure its performances under laboratory, temperature, radiation….

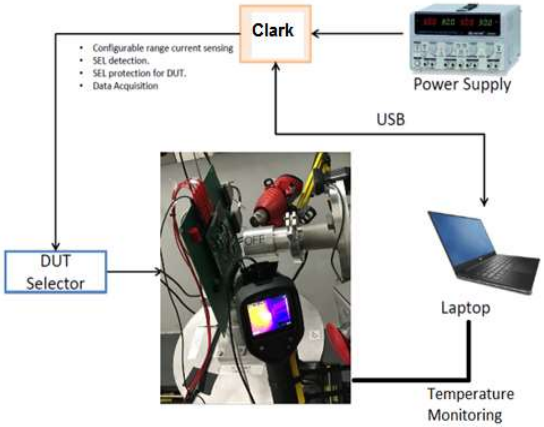
D5.2 : Electrical Validation plan
D5.3 : Radiation Validation plan (TID + SEE)
D5.4 : Test board datapackage

Task 5.2: **Electrical and radiation tests of Pilot Circuit Run 1** - Participants: TASF, MENTA, VTT - **Facilities & beam foreseen by Q2-23.**

Test the electrical and radiation performances consistency with the IPs and Pilot Circuit requirements .

D5.5 : Electrical Validation report
D5.6 : Radiation Validation report





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Task 5.3 Qualification of Pilot Circuit

Leader: TASF/Supply Chain - Participants: VTT, MENTA

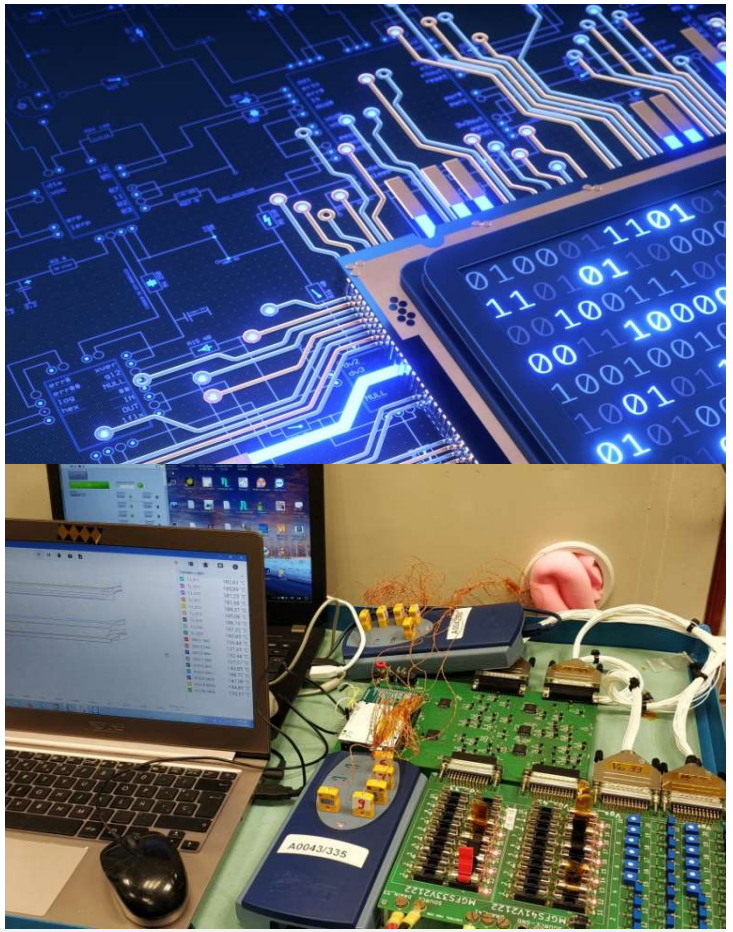
Includes all qualification steps in compliance with the Manufacturing Plan Standard and Pilot Circuit Procurement Specification.

The Pilot Circuit is submitted to the silicon qualification flow.

Qualification foreseen on the Pilot Circuit, after successful validation of the electrical and radiation specification.

For each of these IPs and for Pilot Circuit, its qualification status will include

- usage restrictions and/or recommendations
- production yield
- drift during screening and HTOL.



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PROMISE Project Conclusions

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Conclusions

- ✓ **PROMISE targets to become an ecosystem built around an IP Library qualified for Space usage**
- ✓ **Faster, Cheaper, Lower Risk Mixed Signal ASICs can be manufactured**
- ✓ **Participation is open for End Users, Supply Chain actors, Technology and Design providers**
- ✓ **Contributions and cooperation will build a stronger community and benefit the contributors**
- ✓ **Further IP library details will be shown on final CUG workshop presenting project results & outcomes.**

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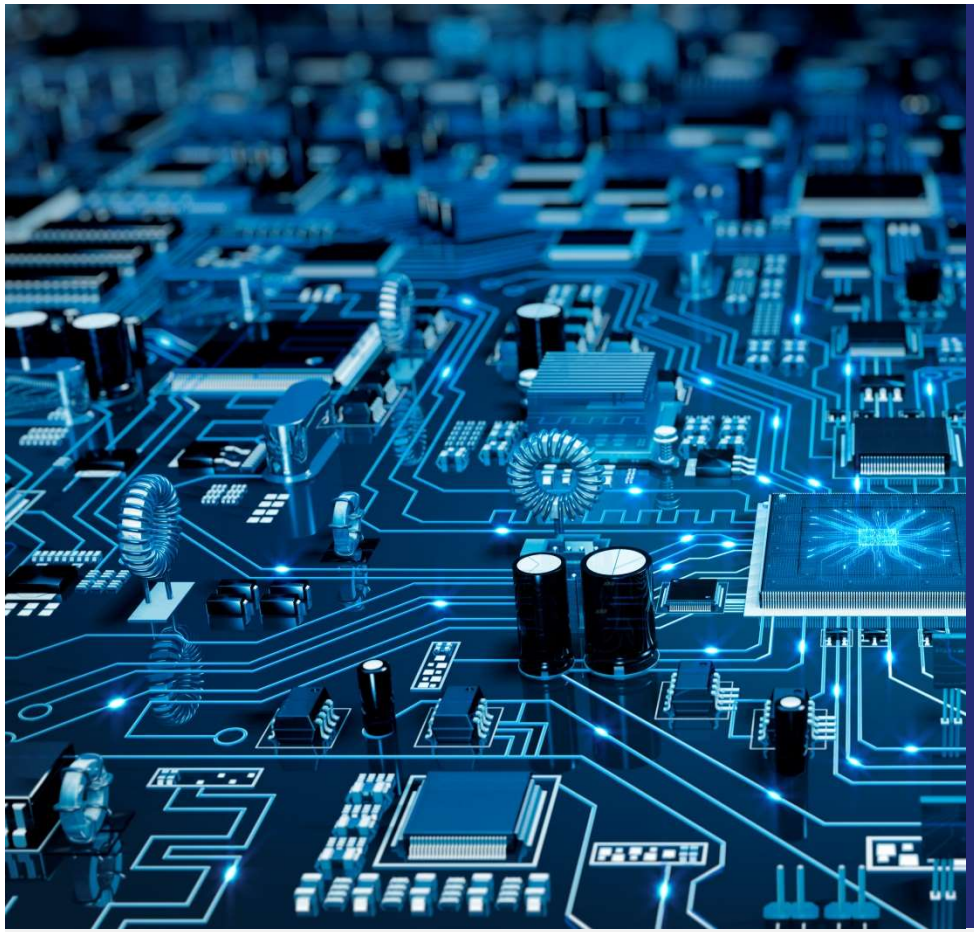

Thank you

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Main achievements

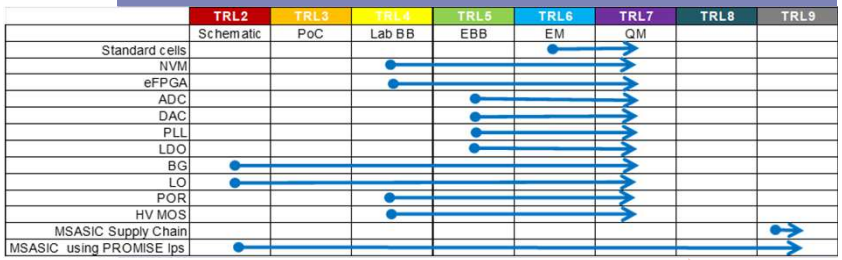
1. Project identity well-defined with a notable impact after press releases in space sector

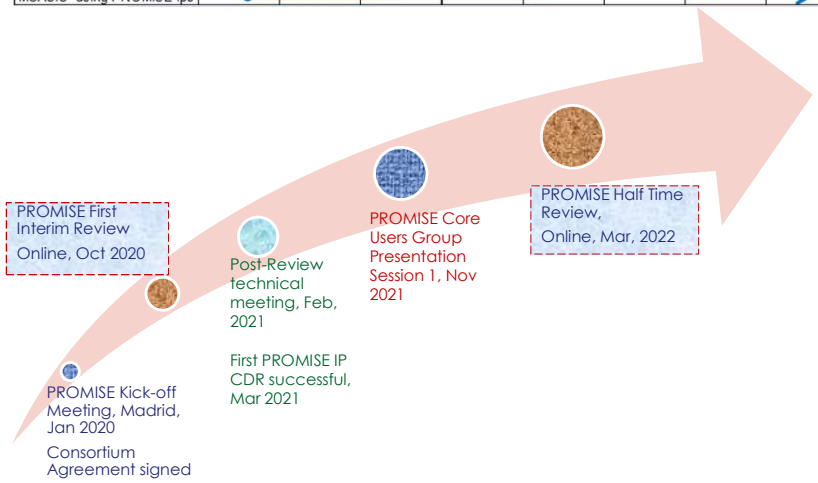
   PROMISE Webpage: https://promise-h2020.eu/

2. ~80% of PROMISE IPs passed their CDR

3. Pilot Circuit DDR successful; CDR in preparation;

4. PROMISE Core Users Group created;





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RTL Verification Plan

- 8 Unitary test benches + 1 Global test bench
- 69 test cases
- Verification status : 100% PASS
- Code coverage : 100% COVERAGE
- Reference document : *[0005-0015514539] PROMISE Pilot Circuit ASIC VERIFICATION PLAN (29/03/2022)*

Coverage Summary by Structure:

Design Scope	Hits %	Coverage %
i_dut	100.00%	100.00%
i_propici_top_0	100.00%	100.00%

Coverage Summary by Type:

Total Coverage: (Filtering Active)					85.88%	100.00%
Coverage Type	**Bins**	**Hits**	**Misses**	**Weight**	**% Hit**	**Coverage**
Statements	2072	2072	0	1	100.00%	100.00%
Branches	1346	1346	0	1	100.00%	100.00%
FEC Expressions	139	139	0	1	100.00%	100.00%
FEC Conditions	281	281	0	1	100.00%	100.00%
FSMs	236	236	0	1	100.00%	100.00%
States	87	87	0	1	100.00%	100.00%
Transitions	149	149	0	1	100.00%	100.00%

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IP BG ID card

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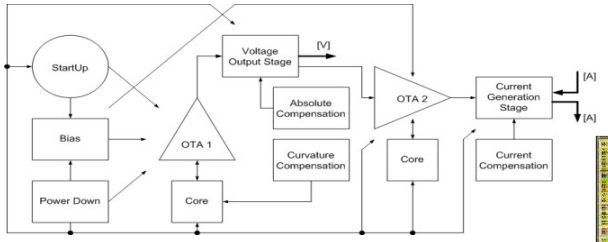
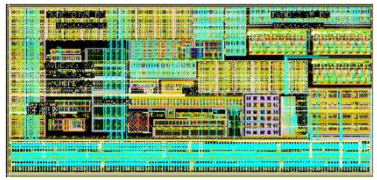
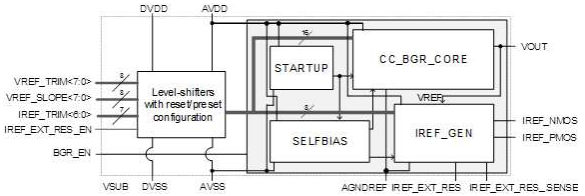
Functional description

- Stable output voltage (1.25 V) – 1.0 to 1.5 - 8 bit trimming with a 0.2 % sensitivity LSB
- TC below 6 ppm/°C over PVT corners with a current consumption of 1 mA
- Second order compensation and radiation hardening
- External resistor compatibility and internal trimmer for current reference (20 µA) – 18 µA to 22 µA – 1 bit select and 7 bit trimming for both NMOS and PMOS loads
- SET free







Main Performances

- Output Reference [V] = 1.25
- Output Current [µA] = 20
- Current Consumption [mA] = 1
- Max Temperature Coefficient [ppm/°C] = 6
- Min Power-Supply Rejection Ratio [dB] = 60

Layout characteristics

- Silicon area : 0.925 mm X 0.435 mm = 0.4 mm²
- Consumption : 1 mA
- Power : 3.3 mW
- Number of IOs : 15 (12 × 1bit + 3 × 8bit)

SCHEMATIC NETLIST → LAYOUT → CDR → DATA PACKAGE

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IP LDO ID card

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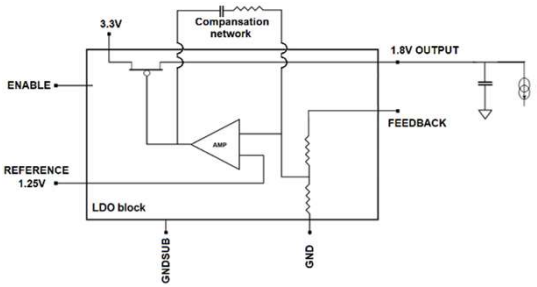
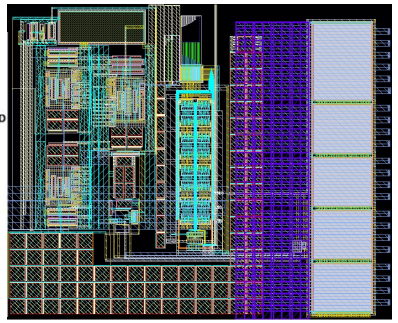
Functional description

- Low drop out 1.8V output voltage from 3.3V power supply
- High current output
- Trimmable output voltage
- Short circuit protection
- SET free





Main Performances

- Output current - up to 500 mA
- Settling time < 140 µs
- Output ripple during load transients / power on / reset < 6%

Layout characteristics

- Silicon area : 0.67mm X 0.875mm = 0.59mm²
- Consumption : 2.24 mA
- Power : 7.4 mW
- Number of IOs : 9

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IP POR

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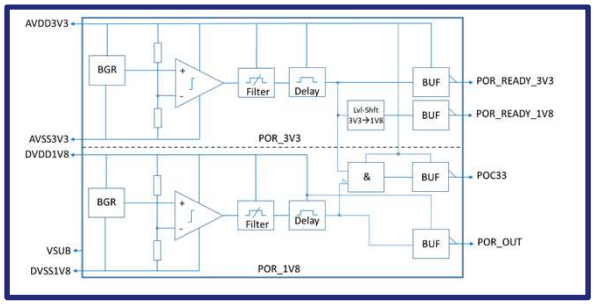
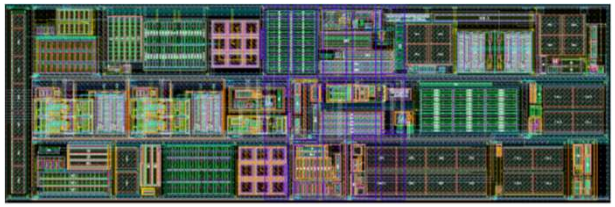
Functional description

- Two independent POR devices supporting 3.3V/1.8V power supply (PS) domains
- BG voltage reference for accurate POR signal generation
- Delay added before POR signal released
- Undervoltage pulse filter
- SET free

Main Performances

- Valid PS voltage ranges = 3.3V-5%/+10% and 1.8V ±10%
- POR released/undervoltage corners = 3.1V/2.9V and 1.60V/1.52V
- Compatible with PS rise times = 10ns…100ms
- Min POR delay = 100 µs
- UV pulse filter = 10 ns





Layout characteristics

- Silicon area : 641µm x 209µm
- Consumption : 0.3 mA
- Power : 1 mW
- Number of IOs : 17

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IP LO ID card

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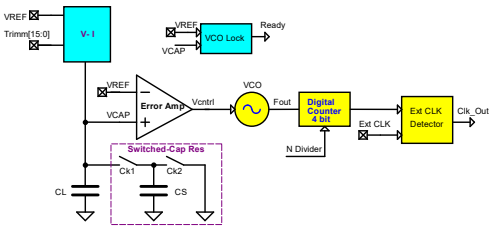
Functional description

- FLL based 16MHz clock generator
- Wide range Temperature compensation -40ºC to +125ºC
- Radiation hardened
- Low Jitter
- SET free

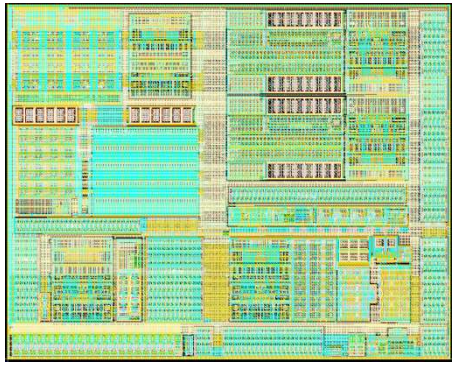
Main Performances

- Output clock frequency = 16 MHz
- Temperature coefficient < 50 ppm/ºC
- Low jitter < 15ps
- Fast power-up time < 30us
- External clock detector

Block Diagram



Layout



Layout characteristics

- Silicon area : 1.26 mm X 1 mm = 1.26 mm²
- Consumption : 5.7 mA @ 3.3V
- Power : 18.81 mW
- Number of IOs : 32

SCHEMATIC NETLIST → LAYOUT → CDR → DATA PACKAGE

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IP PLL ID card

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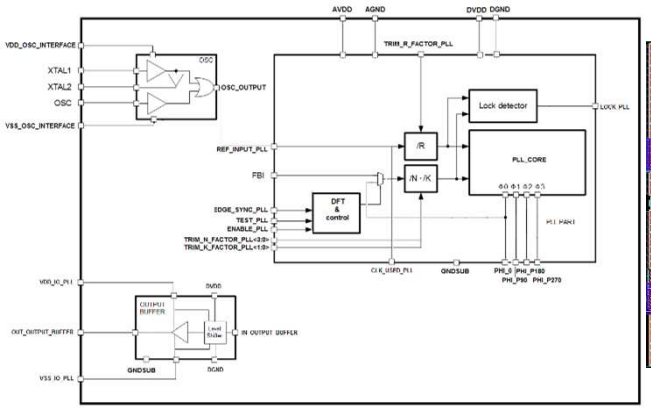
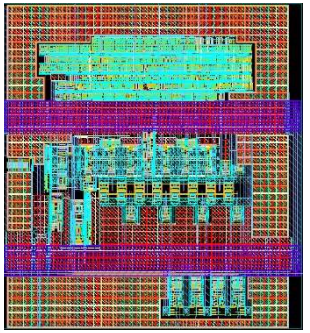
Functional description

- Programmable output frequency range 25MHz up to 200MHz
- 4 phases available (0°, 90°, 180°, 270°)
- Reference clock Digital LVTTL clock, Crystal oscillator or sine wave (from 8 MHz up to 50 MHz)
- Selectable positive or negative edge synchronization
- Can drive outside ASIC capacitive loads up to 20pF





Main Performances

- Period jitter <32 ps peak-to-peak @ 200MHz
- Lock time < 63 µs

Layout characteristics

- Silicon area : 1.6 mm X 1.74 mm = 2.78 mm²
- Consumption : 42 mA (main PLL block)
- Power : 135 mW (main PLL block)
- Number of IOs : 32

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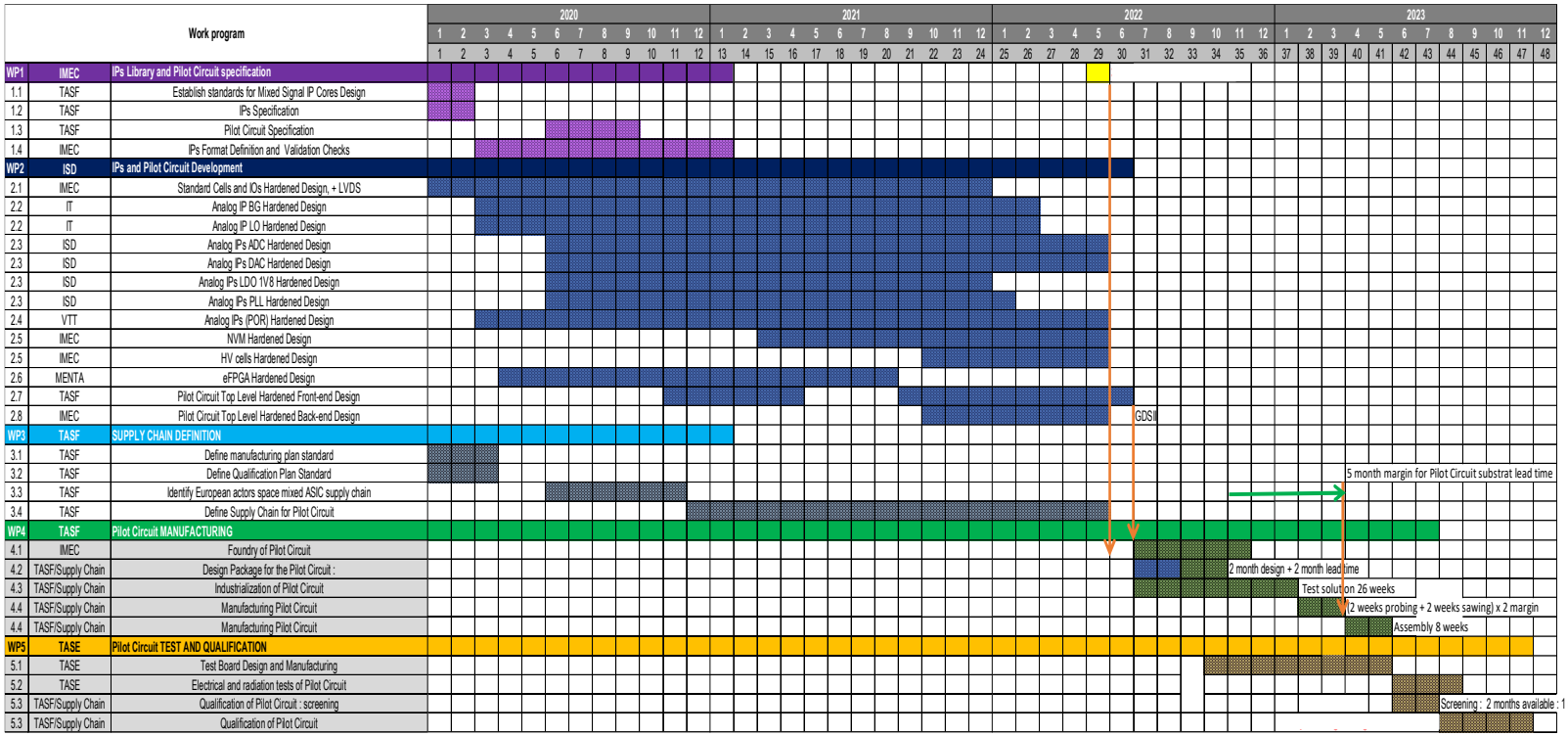
Next Steps (2/2)



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