Accomplishing PROMISE, PROgrammable MIxed Signal ASIC Electronics Framework

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***Abstract*—This paper presents the activities, current results and status of the PROMISE (PROgrammable MIxed Signal Electronics) project which started at the beginning of 2020 . The project has received funding from the European Union's Horizon 2020 research and innovation program under grant agreement No 870358. It's tailored to bring to the space community a flexible, cost competitive mixed-signal ASIC architecture design ecosystem built on a portfolio of silicon qualified hardened IP blocks. It includes analogue IPs such as ADC, DAC, PLL, LDO, BG, LO, POR and HV MOS transistors. A digital embedded FPGA core provides a flexible programmable element and an NVM permits reconfiguration abilities without the need of using an external memory.**

All these elements are included on the PILOT Circuit ASIC that will be submitted to electrical validation and radiation testing as part of the qualification process of these basic elements for their future use as building blocks.

Keywords—Analogue IP, Embedded FPGA, Mixed Signal, PROMISE, ASIC, ASSP, Radiation hardening, eFPGA, Non Volatile Memory, ADC, DAC, PLL, LDO, BANDGAP, Local Oscillator, Power On Reset

I. INTRODUCTION

PROMISE project [1], started at the beginning of 2020, has lived by now more than 2 years of harsh but exciting times of successful microelectronics developments. It has crossed the equator of its lifetime given its planned total duration of 4 years During this time the IPs have successfully passed their CDRs whereas the Pilot Circuit ASIC CDR, integrating all the IPs, is planned for the 2nd half of 2022.

The PROMISE project gathers IC experts from 7 European institutions. This project has received funding from the European Union's Horizon 2020 research and innovation program under grant agreement No 870358. PROMISE stands for PROgrammable MIxed Signal Electronics and is tailored to bring a flexible mixed-signal ASIC architecture design ecosystem built on a portfolio of silicon qualified hardened IP blocks to the space community. Moreover, the project is intended to provide a flexible, cost competitive mixed-signal ASIC manufacturing and qualification ecosystem. Last but not the least, PROMISE will deliver IP dissemination, commercialization and intellectual property

management to allow efficient reuse of the project's outcomes within the space community and will provide a full European design environment for new IPs and mid-range ASIC for space applications.

The PROMISE project objectives are to optimize the design cost, shorten schedule and de-risk analogue and mixed ASIC radhard design, manufacturing and qualification according to the needs of the space industry. PROMISE, led by Thales Alenia Space, encompasses diverse European partners, subcontractors, potential users and solution providers, all top actors of the European Mixed Signal ASIC ecosystem. The partners involved are: Thales Alenia Space in Spain (who leads the project), top level SMEs as ISD (Greece) and MENTA (France), key technological institutes such as IMEC (Belgium), IT (Portugal) and VTT (Finland); and a leading satellite manufacturer as Thales Alenia Space in France.

PROMISE is based on a modular architecture built on the DARE180X/XFAB XH018 0.18 micron Mixed Signal HV CMOS Technology that allows the end users to target both simple and complex applications of Mixed-Signal ASICs such as signal conditioning and acquisition, motion control, signal processing, signal synthesis and others. This architecture pivots around a central eFPGA module that provides extra flexibility during the lifetime of the mixed-signal ASIC.

II. PROMISE MIXED SIGNAL ECOSYSTEM

PROMISE has designed an IP library oriented towards the fast design of mixed-signal ASICs by the suitable aggregation of pre-validated modules with the minimum added specific circuitry. It enables mixed-signal ASIC and ASSP approach. IP reuse will ensure the shortest and secured schedule and de-risk the design hardening for mixed-signal ASIC/ASSP.

The first population for this library, includes a set of radiation hardened and reusable analogue, high voltage and digital IPs that covers the most common functions for data acquisition, conditioning, processing and control. This initial portfolio of IPs includes the following functions:

- Digital IPs: Digital standard cells; Analog and digital IO cells; Non-Volatile Memory (NVM); Embedded Field Programmable Gate Array (eFPGA) core.
- Analog IPs: Analog to Digital Converter (ADC); Digital to Analog Converter (DAC); Phase Locked Loop (PLL); Low Drop Out (LDO) for digital core; BandGap (BG) with second order temperature compensation; Local Oscillator (LO) with no external component; Power On Reset (POR); High Voltage MOS transistors (HV).

Those IPs are embedded in the Pilot Circuit ASIC for electrical performances and radiation tests. The tests will provide:

- Measured Electrical compliance of the IP blocks through the electrical validation of the Pilot Circuit;
- The electrical Safe Operating Area for high Voltage MOS;
- Evaluated Radiation hardness of the IP blocks through the radiation evaluation on the Pilot Circuit.

All IPs shall be compliant with the radiation requirements defined within the project. The target radiation performances to be tested on the PILOT Circuit ASIC are as follows:

- TID: > 100 krads
- SEL: LET > 60 Mev.cm^2/mg
- SEFI: LET > 60 Mev.cm^2/mg
- SEU: < 10^{-8} event/day/bit

The following table summarizes the IP developers:

TABLE I. IPS AND OWNERS

Company	Function/IP
MENTA	eFPGA
IMEC	NVM, digital libraries and LVDS IOs
ISD	ADC, DAC, PLL, LDO
IT	Local Oscillator, Bandgap
VTT	Power On Reset
TAS-France	Pilot Circuit Front-end and Synthesis
IMEC	Pilot Circuit Back-end and HVMOS test vehicle
TAS-Spain	User application in eFPGA

III. PROMISE PILOT CIRCUIT ASIC ARCHITECTURE

The PROMISE Pilot Circuit ASIC is the demonstrator for the ASSP approach enabled by the radiation hardened PLL, eFPGA and NVM. The Pilot Circuit Block diagram is depicted in the figure below:

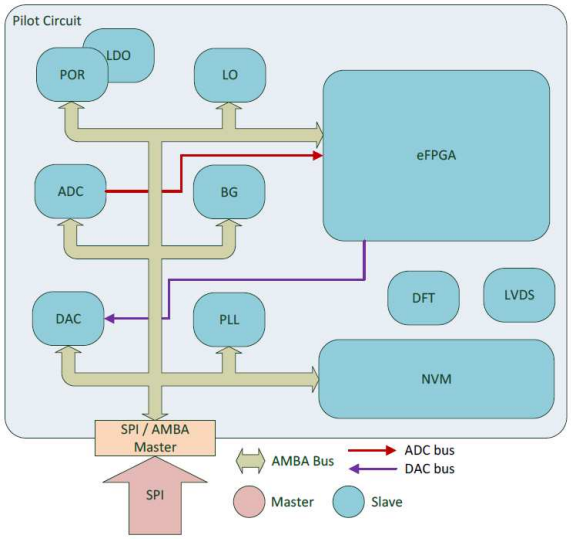

Fig. 1. PROMISE Pilot Circuit diagram

As presented, PROMISE Pilot Circuit instantiates the IPs designed by the PROMISE Consortium in an architecture that allows its usage for operational missions. The digital core has been designed using the radiation hardened DARE180XH standard core, level shifters and IO libraries.

The POR, Bandgap, LDO and Local Oscillator ensure the safe power up of the circuit. ADC and DAC are intended to

This project has received funding from the European Union's Horizon 2020 research and innovation program under grant agreement No 870358

provide analogue resources for housekeeping acquisition and sensor or actuator biasing. SPI bus provides a user interface, connected to the internal AMBA bus. The NVM embeds Pilot Circuit configuration bits and the eFPGA bit stream. The eFPGA provides GPIO interfaces, including LVDS IOs for characterization. Standard digital DFT (SCAN) is implemented and internal analogue points are available through a specific analogue test bus per power domain (3V3 and 1V8).

All IPs are accessible and operated individually to ease the debug and characterization tests. The Pilot Circuit also embeds high voltage test features (MOS, Bipolar and diodes).

The PROMISE Pilot Circuit will be manufactured by XFAB foundry using a Multi-Layer-Mask reticle and will be packaged in an organic BGA or as chip on board.

The ASIC Floor Plan is shown in the figure below. The chip size is limited by the MLM reticle: 21mm x 11mm.

Fig. 2. PROMISE Pilot Circuit package

The PROMISE Pilot Circuit ASIC DDR was performed in May 2022 and CDR is expected in the 2nd half of 2022.

IV. IP LIBRARY OVERVIEW

A. eFPGA IP

Menta is a proven eFPGA pioneer whose design-adaptive standard cells-based architecture and state-of-the-art tool set provides the highest degree of design customization, best-in-class testability and fastest time-to-volume for SoC design targeting any production node at any foundry.

For PROMISE, Menta is providing a radiation hardened embedded FPGA (eFPGA) IP [2], that is integrated into PROMISE ASIC, enabling hardware re-configurability in the field.

After a first successful phase of collaboration with IMEC, that led to a set of optimized radiation hardened standard cells for best PPAs (Power, Performances, Area), Menta has successfully delivered, on schedule to the PROMISE project, its radiation hardened embedded FPGA (eFPGA) closing CDR (Critical Design Review) Milestone. The IP with the following characteristics is now integrated in the PROMISE Pilot Circuit.

- eFPGA IP of 1750 LC (capacity similar to Microsemi RTSX32) + 3 additional DSP
- IP technology is XFAB 180 nm (XH018)
- Radiation -hardened
- eFPGA IP is designed 100% using DARE180X heritage and PROMISE rad-hard standard cells designed by IMEC.

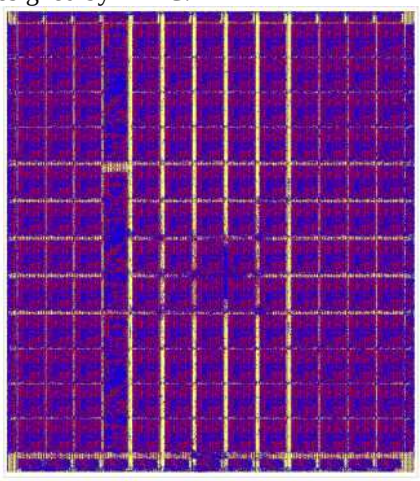

Fig. 3. PROMISE eFPGA IP top level GDSII

B. Non-volatile memory IP

Non-volatile memory (NVM) macros are widely used in digital circuits in order to store instructions, user data or any configuration data. In PROMISE, the NVM macro keeps the user defined FPGA configuration data. FPGA consists of multiple LUT instances. In general, every LUT has configuration signals, which define the logic function a LUT performs. At the same time the set of those configuration signals defines a particular user functionality of FPGA. In PROMISE FPGA, the configuration data are uploaded at power up from the NVM to the LUT registers. Obviously NVM has a data capacity equal to the amount of FPGA configuration signals plus redundancy bits required by the radiation hardening technique.

NVM macro designed in PROMISE is based on SONOS cell of E2PROM type offered within 180 nm HV CMOS process. This cell promises a satisfying level of robustness against TID effects. E2PROM type write/erase operations provide reliable data retention parameters. The cell endurance (amount of erase/write cycles) is worse than in FLASH cell type, but the target application does not require high endurance. NVM memory is hardened against SEL and SEU/SET by use of standard DARE RH mitigation methods. On top of that, error correction codes (ECC) with single error correction double error detection (SECDED) capabilities is implemented as SEU mitigation method. ECC improves also the general read robustness of NVM and thus is highly required in space applications. Different types of error correction codes are described in detail in [3]. As a result, the NVM macro will operate as a robust and radiation hardened data storage IP.

NVM macro has got 344 kbits user data capacity and is organized with 32 bit data words, where 24 bits are user data and 8 bits are ECC. It's split in 2 banks with 32x22 pages. Every page consists of 8 words. The memory organization parameters are provided in TABLE II. NVM has got standard synchronous parallel user interface which simplifies read operations. NVM has got a built-in Charge Pump, as well as all control logic to perform erase/write operations following a user instruction. Various test modes are implemented in NVM macro to support a production test flow. Power down mode is another memory feature which

allows to reduce the overall system power consumption once configuration data are uploaded. The memory macro requires 2 supply voltages: 1,8V and 3,3V with ± 10% tolerance.

TABLE II. NVM IP general parameters

Word, bits	32
Number of Data Words	256x42
Total Number of Words	256x44
Page, Words	8
Pages per Sector	32
Number of Sectors	42+2 inactive
Memory banks,	2
Sectors per Memory Bank	21+1
ECC Bits per Word	8
Total Amount of Memory, bits	360448
Synchronous Parallel Interface	Yes
Data I/O Width, bits	32

The NVM CDR is foreseen in June 2022.

C. Digital Libraries

Digital libraries in DARE180XH platform [4] support the implementation of mixed-signal designs for space applications in the low-power XFAB 0.18µm commercial technology. Special layout techniques are employed to reach TID tolerance over 100 krad as well as SEL hardening against events over 60 MeV/cm^2.mg. SEE hardening can be achieved at system level by combining SEU-hardened architectures and hardened-by-drive-strength cells available in libraries using unique design methodologies.

DARE180XH features extensive standard cell libraries in low-power and low-Vt device flavours, multi-domain I/O library for analog and digital interface and a range of SRAM memory blocks. Recent developments include optimization of SEU-hardened DICE cells to tackle charge sharing effects under transient events, additional 1.8V analog I/O cell configurations, a distributed power-on-control mechanism in I/O cells and a new power management kit (PMK) library to enable interfacing 3.3V logic from mixed-signal IP and 1.8V standard core logic.

DARE180XH LVDS library includes receiver and transmitter cells to enable the implementation of high-speed data links reaching up to 700 Mbit/s. LVDS interface cells are fully cold-spare compliant as required by most space applications. Both can be biased either in current mode or in voltage mode, supporting small and large number of LVDS instances with optimal power requirements. The LVDS receiver also features a fail-safe output that can be used to detect faulty conditions in transmission lines, such as short and open circuit. Both transmitter and receiver cells have been designed to be SET free up to 60 MeV.cm^2/mg and SEL free up to 80 MeV.cm^2/mg.

D. 24 bit ADC IP

The system block diagram is shown in Fig. 4.:

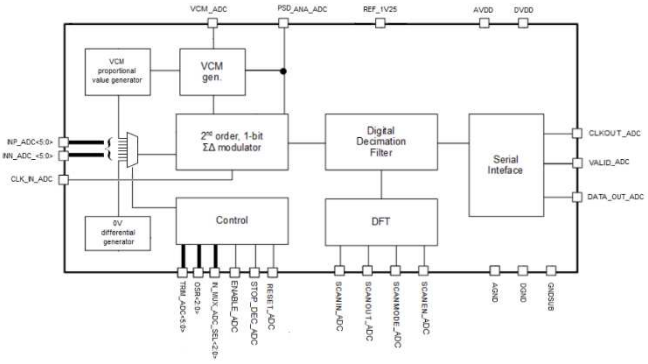

Fig. 4. 24 bit ADC block diagram

The ADC architecture is based on a second-order, discrete time (switched capacitor) Sigma-Delta modulator with 1-bit quantizer [5]. The ADC has 6 differential multiplexed inputs that enable interleaved data acquisition and two dedicated inputs for offset and gain correction. The full-scale input voltage range is a multiple of the 1.25V bandgap generated reference voltage and equal to ± 2.5V, which can be trimmed externally at 6 bit resolution The differential input voltage is modulated by the ΣΔ modulator operating at a maximum frequency of 15MHz with selectable Over Sampling Ratios from 64x up to 2048x. The output data are provided through an SPI like 3-wire synchronous digital interface in signed binary format.

The targeted main specifications are listed in TABLE III.

TABLE III. ADC TARGETED SPECIFICATIONS

Conditions	***Conditions***	***Value***	***Units***
Full scale range (FSR)		±2.5	V
Analog input bandwidth	OSR = 256x	<40	kHz
Offset		<1%	FSR
INL		<1.5	LSB
DNL		<1	LSB
Gain Error		<0.25%	FSR
ENOB	At 256 ksps	15	bits
Power consumption	At fclk=15MHz	37	mW

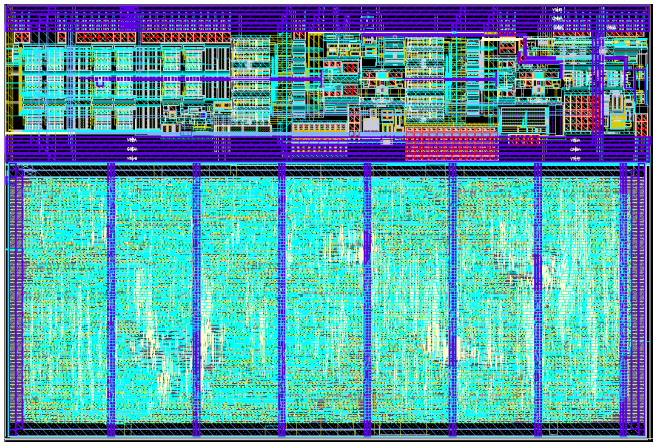

Fig. 5. ADC layout view

The ADC dimensions are 3.025mm x 2.036mm. The ADC is in the final design verification stage.

E. 24 bit DAC IP

The Digital-to-Analog converter is a current-steering, low-noise circuit optimized to operate in the frequency range between DC and 50kHz [5]. The DAC receives 24-bit sampled data in a synchronous serial format and converts it into a differential current analogue signal. It uses a third-order multi-bit Sigma-Delta modulator. The embedded interpolator follows a multiple-stage architecture and consists of an FIR equi-ripple low-pass filter followed by two cascaded stages of Half-band equi-ripple filters. The last stage is a programmable SINC filter, which provides variable interpolation ratios allowing sampling rates as high as 310kHz. The system operates on a single clock domain, which is provided externally. The output current matrix features a Return-to-Zero (RTZ) technique to improve the linearity by ensuring that each elementary current source is zeroed, regardless the data value of the sample sequence. The internal reference current can be trimmed to achieve accuracy of less than 1 % of the Full Scale Current (5.5mA). The use of an external current reference is supported as an optional feature. The reconstruction filter and the I/V converter are realized externally to aid the design flexibility and device integration according to the target application requirements. The system block diagram is shown in Fig. 6

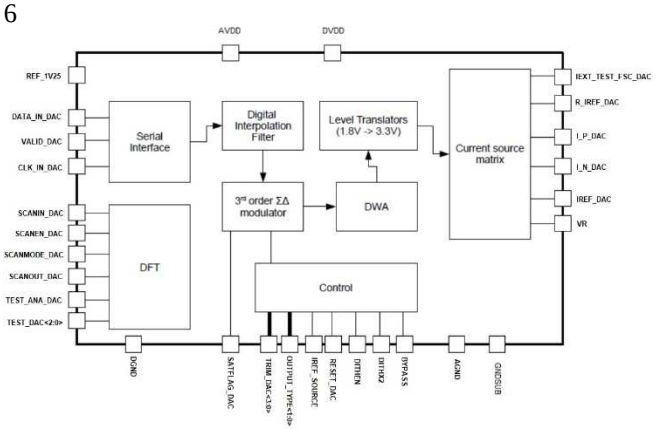

Fig. 6. DAC block diagram

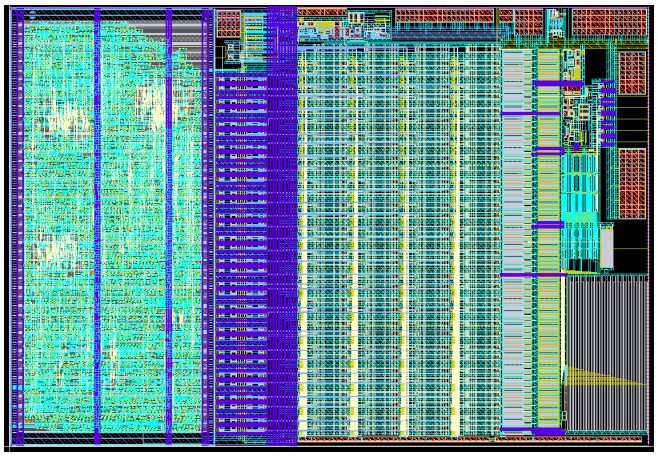

Fig. 7. DAC layout view

The dimensions of the DAC are 3.577mm x 2.456mm. The final design verification stage is successfully finished and the design is closed through a successful CDR.

F. PLL IP

The system block diagram is shown in Fig. 8

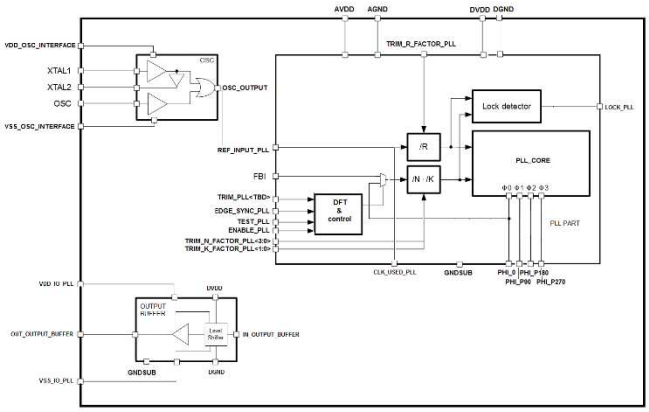

Fig. 8. PLL block diagram

The PLL is built around a multi-phase VCO core capable of generating very stable clock signals up to 200MHz in frequency that are locked in phase to an externally provided clock, or to an ASIC's internal generated, clock reference source running at a much lower frequency [5]. The external reference clock input maybe directly interfaced to a 3.3 LVTTL digital source or a sine wave oscillator in the frequency range between 8 MHz and 50 MHz. Alternatively, the reference clock can be locally generated by a quartz crystal attached directly to the crystal interface input of the PLL using a minimum number of external components. The supported reference clocks are from 8 MHz up to 50 MHz. The PLL can generate simultaneously four different phased clocks signals at 0º, 90º, 180º and 270º phase shift related to the rising or falling edge of the reference clock.

The peak-to-peak jitter is 31ps at 200MHz. The PLL start-up time, until the Lock flag is asserted is 70µs.

Also, a CMOS output buffer is designed, to be able to drive 50Ω transmission lines at 3.3V LVCMOS/LVTTL levels through external source series resistive termination. The jitter after the buffer is 39ps and the current consumption is 45mA when driving a capacitive load of 20pF at 200MHz.

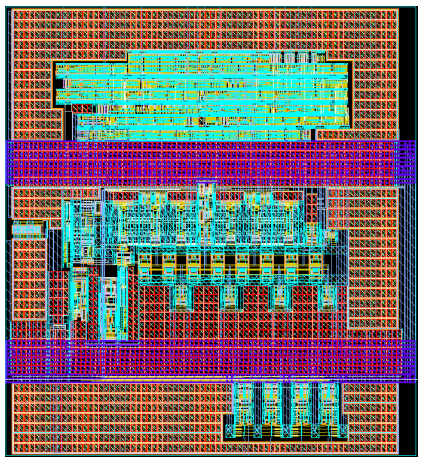

Fig. 9. PLL layout view

The dimensions of the PLL are 1.594mm x 1.739mm. The PLL design has finished

G. 1.8V LDO IP

The system block diagram is shown Fig. 10.:

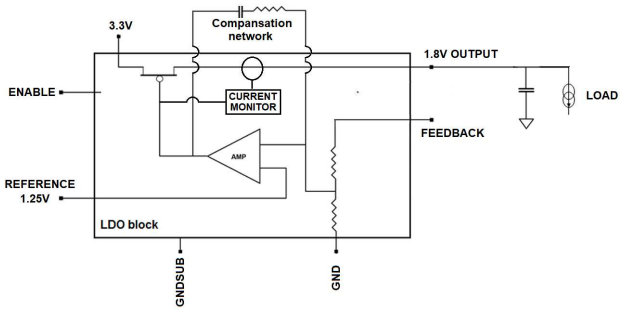

Fig. 10. LDO block diagram

The LDO generates from the 3.3V supply rail the lower 1.8V supply voltage needed by the digital circuits within the ASIC [6]. Its output voltage can be fine-tuned through an external digital discrete interface at 4 bits resolution. It can provide up to 500mA to the digital circuits and includes short circuit protection.

The output voltage of the LDO never exceeds ± 10% of its nominal value, even during extreme load transient conditions including 0-100% output load steps and system resets. During start-up the built-in soft start operation is activated to reduce the in-rush current transient. The feedback monitoring resistor divider is not tied internally, but is free for the back-end engineer to be connected in the ASIC for more accurate load regulation.

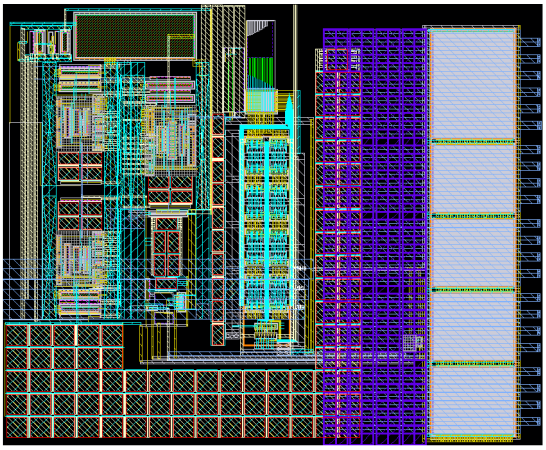

Fig. 11. LDO layout view

The dimensions of the LDO are 795µm x 673µm. The LDO design is finished.

H. Bandgap IP

Bandgap Voltage Reference (BGR) circuits are widely used in analog and mixed-signal IPs, in pilot circuits, balancing proportional-to-absolute temperature and complementary-to-absolute temperature voltages, in order to deliver a stable and temperature-independent output voltage [7].

In PROMISE, the BGR has a 2nd-order curvature compensation and is capable of delivering, not only a stable output voltage, but also current sourcing for N-type and P-type loads through internal resistors or, optionally, through an external precision resistor.

The BGR design includes 8-bit trimming resistive ladders for post-fabrication calibration of temperature compensation slope, absolute output voltage and absolute output current. The applied technique is essential to perform in all the special conditions that characterize the space environment, while considering process, voltage and temperature variations, as well as the impact of Single-Event Transients (SETs) and Total Ionizing Dose (TID) [8][9].

The BGR block diagram is shown in Fig. 12.

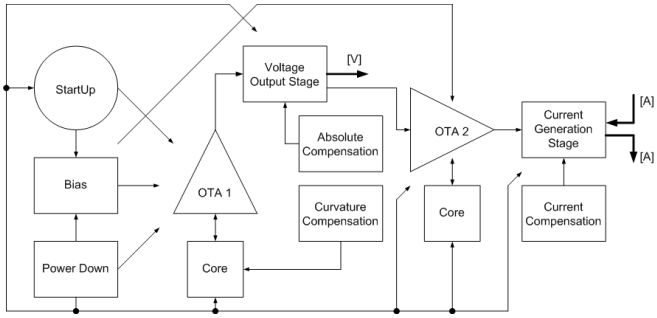

Fig. 12. Bandgap block diagram

The circuit was designed in a 180 nm Silicon-on-Insulator CMOS technology, using hardening by design techniques.. A temperature coefficient better than 8 ppm/°C (6 Ω/bit) over an extreme temperature range of -40 to 125 °C has been achieved in simulation, with a 1.25 V output voltage and 20 µA output currents after calibration, draining less than 1 mA from a 3.3 V source, as outlined in TABLE IV.

TABLE IV. BANDGAP SIMULATION RESULTS SUMMARY

Output Reference Voltage[V]	Ouput Reference Current [µA]	Analog Supply Voltage [V]	Digital Supply Voltage [V]	Current Consumption [mA]	Temperature Coefficient [ppm/°C]	Power-Supply Rejection Ratio [dB]
1.25	20	3.3	1.8	< 1	< 8	> 60

The BANDGAP has successfully passed its CDR..

I. Local Oscillator IP

Quartz crystal (XTAL) resonator and crystal oscillator (XO) are widely used as a frequency reference in numerous applications. Despite XTALs and XO being excellent frequency references due to the intrinsic high quality (Q) factor, high frequency accuracy and low frequency temperature coefficient, both of those oscillator's blocks are difficult to integrate. The alternative solution is to use high-Q MEMS resonators integrated in a microelectronic process technology, which will replace XTAL. However, it is still challenging to integrate into a CMOS technology due to difficulties with extra masks cost, packaging and process integration, poor power handling and limited frequency trimming. Considering those challenges, the design of an integrated oscillator, which can replace in part a crystal oscillator, is proposed.

The proposed oscillator uses a frequency-locked loop (FLL) [10] to keep the output frequency within the specification range of +- 50ppm/ºC. The top cell is able to generate an output frequency of 16MHz. Temperature compensation is achieved by using two series resistors with opposing temperature coefficients. The resistors are used in the V-I converter to generate a compensated reference current. The Vref is an external bandgap voltage.

The design includes 16-bit trimming for post-fabrication calibration in temperature compensation, and absolute output frequency. The applied technique is essential to perform with all the special conditions that characterize the space environment, while considering process, voltage and

temperature variations, as well as the impact of Single-Event Transients (SETs) and Total Ionizing Dose (TID). The LO block diagram is shown Fig. 13.

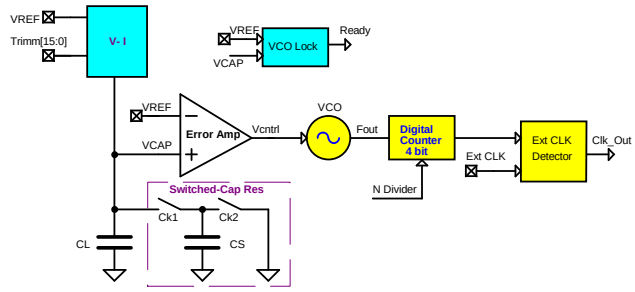

Fig. 13. Local Oscillator block diagram

The circuit was designed in a 180 nm Silicon-on-Insulator CMOS technology, using hardening by design techniques. A temperature coefficient better than 50 ppm/°C over an extreme temperature range of -40 to 125 °C has been achieved, with a 16MHz output frequency after calibration, draining less than 10 mA from a 3.3 V source, as outlined in next table :

TABLE V. LOCAL OSCILLATOR SIMULATION RESULTS SUMMARY.

Input Reference Voltage [V]	Output Frequency [MHz]	Analog Supply Voltage [V]	Digital Supply Voltage [V]	Current Consumption [mA]	Frequency stability [ppm]	Jitter [pS]
1.25	16	3.3	1.8	< 10	<5000	<15

The Local Oscillator has successfully passed its CDR.

J. POR IP

Power On Reset (POR) generates a reset signal when power is applied to the ASSP device. It ensures that the device starts operating in a known state [11]. POR also monitors power line and generates a reset signal when the supply voltage falls below under-voltage threshold.

POR IP includes unique features such as two independent POR blocks, one for 3.3V analog and one for 1.8V digital power domain. Both POR blocks include bandgap reference voltage source and comparator for accurate power supply voltage level and under-voltage condition detection. POR is compatible with power supply's rise times from 10ns to 100ms. Internal delay generator ensures that POR state is always active at least 100µs. Under-voltage conditions shorter than 10ns are filtered out. POR is functional from -40°C to 125°C. Typical current consumption is 180µA.

POR IP is SET immune up to 60 MeV.cm^2/mg. Radiation hardening is achieved by design, utilising existing radhard DARE180X library, pulse filtering and using logic gates that minimize the SET generation or propagation in the most vulnerable nodes.

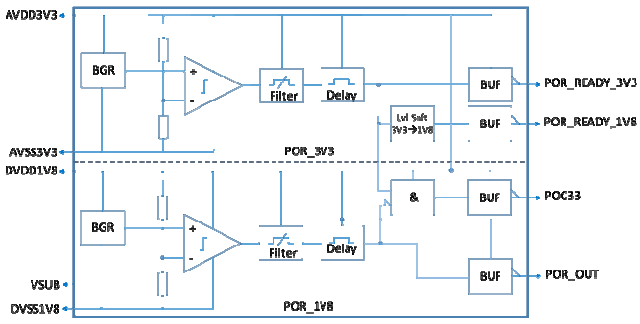

Fig. 14. POR IP block diagram.

POR post-layout simulation results are outlined in the table VI:

TABLE VI. POR SIMULATION RESULTS SUMMARY.

Analog Supply Voltage (3.3V)	3.14…3.63	V
Digital Supply Voltage (1.8V)	1.54…1.98	V
Minimum POR active state duration	105	□s
POR released voltage (3.3V/1.8V)	3.05/1.59	V
Undervoltage threshold (3.3V/1.8V)	2.95V/1.54	V
Current consumption (typ)	180	□A
Temperature range (functional)	-40…+125	°C

The dimensions of the POR IP are 641µm x 209µm.

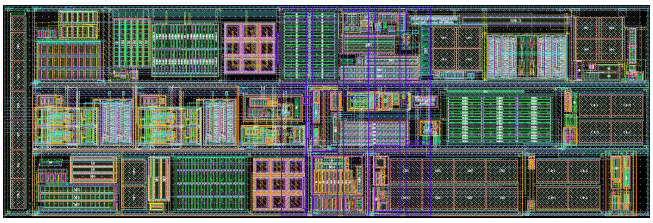

Fig. 15. POR layout view

The Power On Reset is at CDR stage.

V. PROMISE PROJECT STATUS AND PLANNED ACTIVITIES

At this point most of the IPs have successfully passed their CDR. By summer 2022 it is expected to reach a 100% coverage on IP CDRs. The Pilot Circuit ASIC has successfully passed the DDR and a Silver logic level netlist has been transferred to IMEC for layout. Delivery of the Golden netlist will be performed in June 2022 and CDR will take place during Q3 2022. Arrival of ASIC samples is expected by the end of 2022. The supply chain has been defined and Qualification Plan and Procurement Specification are already available.

Design and manufacturing of Test Evaluation Boards for performing Electrical Validation and Radiation testing is on-going. Test Boards manufacturing and its associated test bench will be performed in parallel to ASIC prototype manufacturing. Electrical and Radiation Validation plans are under elaboration. After ASIC samples reception, electrical testing and circuit characterisation shall be performed. If successful, radiation tests will be performed including TID and SEE effects. These activities are foreseen to take place in Q2 2023.

In the 2nd stage, Silicon Qualification Tests shall be performed, as described in Fig. 16. Qualification tests shall

include 4000 Hours High-Temperature Operating Life, NVM Data retention with at least 20 years target, and program endurance with 10000 Program/Erase target. Data retention and endurance shall be guaranteed, for both cases in the operating range from -40ºC to 125ºC.

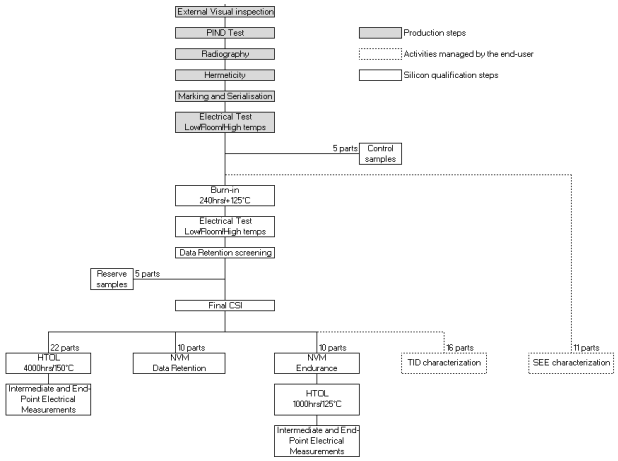

Fig. 16. Silicon Qualification Test program.

For each of the IPs and the Pilot Circuit ASIC, qualification status will include:

- Usage restrictions and/or recommendations
- Production yield
- Drift during screening and HTOL.

In parallel to design activities a PROMISE Core Users Group (CUG) has been established with more than 30 members external to the project. A first meeting took place in November 2021 with the participation of more than 40 potential users. The status of the project, including main milestones, achievements and activities, were presented. CUG members will be able to follow the developments on the project in the upcoming sessions planned for Q4 2022 and Q2 2023.

VI. Conclusions

PROMISE project is on the right track to provide to the European Space Industry a Radiation Hardened Mixed Signal ASIC design ecosystem, fully based on European Suppliers and is ready to launch the PROMISE Pilot Circuit ASIC populated with the first set of IPs developed in the frame of the project. This device will serve as qualification vehicle but has been designed to be as well a functional device of future space data acquisition and processing units.

Pilot Circuit and IP implementations have met the specification requirements, defined at the beginning of the project, according to the verification results obtained.

Pilot Circuit ASIC manufacturing will take place during the 2nd half of 2022 and Electrical Test Validation and characterisation will be performed between end of 2022 and beginning of 2023. This step will be followed by TID and SEL radiation testing foreseen by Q2 2023.

A PROMISE Core Users Group has been set up, and validation and characterisation results from electrical and radiation testing will be presented in future meetings. This group is open to the participation of any potential end user or contributor to the future PROMISE library of IPs.

Once this stage is completed, a library of PROMISE compatible IPs will be available for the users to speed up their design process. This library as well as the entire PROMISE ecosystem shall be accessible to the entire space community speeding up the Mixed Signal ASIC design process and reducing the overall manufacturing cost. Further details on this library and how to access it will be delivered in a final workshop where project results and outcomes will be presented.

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