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Validation, characterization and irradiation testing of the DARE65T platform

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DARE65

RAD HARD DESIGN PLATFORM

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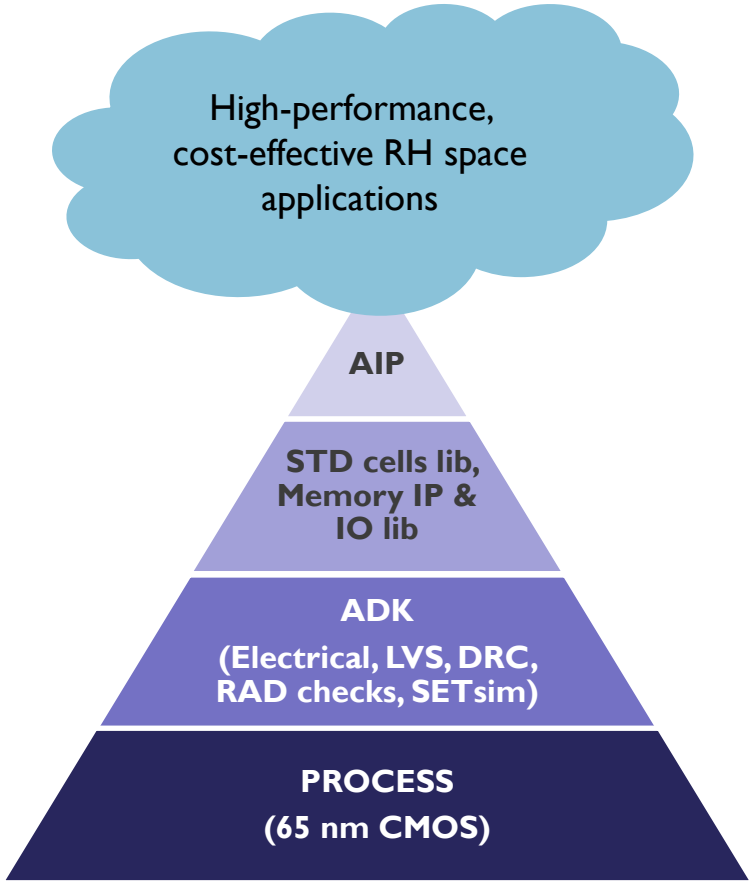
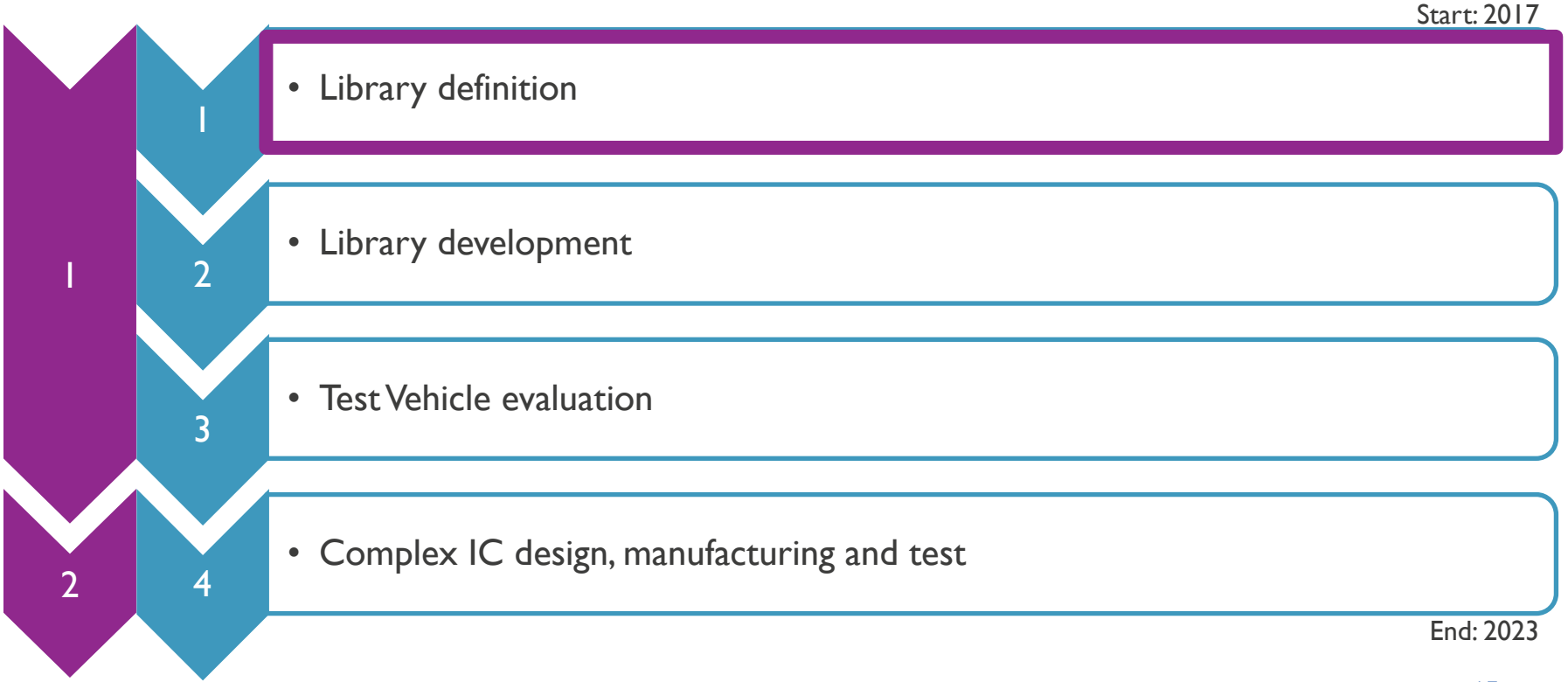


ESA DARE65 project phases

Phases and tasks



Process

- Commercial 65 nm LP process
  - Deep Nwell option
  - MOM or MIM capacitors
  - Dual gate oxide process 1.2V (core) / 2.5V(IO)
  - Multiple VT (high VT, standard VT, low VT)
  - 6 or 9 Cu metal layers
  - RDL available for Flip-chip (Al metal layer)

Operating conditions & Hardness target

Parameter	Min	Typ	Max
Core voltage, V	1.08	1.2	1.32
IO voltage, V	2.25	2.5	2.75
Temperature, ^{0}C	-40	25	125
TID, krad	100	300	
SEL, MeV.cm^2/mg	70		

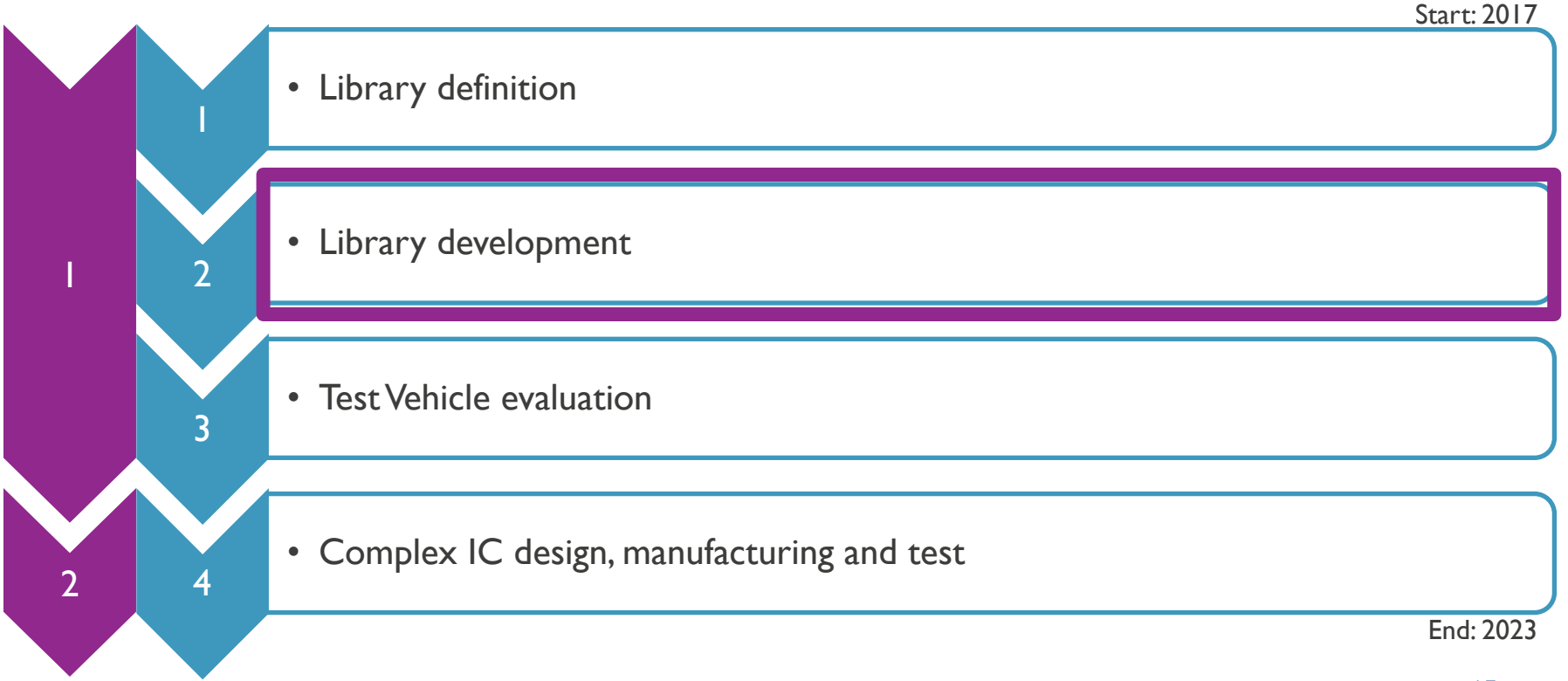
Target SEU, SET hardness levels

Parameter	Min	Typ	Max
High, MeV.cm^2/mg	65		
Medium, MeV.cm^2/mg	40		
Low, MeV.cm^2/mg	25		

- Actual levels to be confirmed after irradiation testing

ESA DARE65 project phases

Phases and tasks



Standard cell library

DARE65T_CORE

- Multi-VT (HVt, SVt, LVt) support
- digital/analogue-on-top & design flow support
- 12 track library – 0,2 um pitch
- Raw gate density ~344 kGates/mm^2

- SET & SEU hardened cells for clock & reset tree
- SET hardened combinational cells
- SEU hardened flipflops and latches (DICE)

Type	#
Non-SET hardened combinational cells	52
SET hardened combinational cells – Low	7
SET hardened combinational cells – Medium	7
SET hardened combinational cells – High	7
Non-SET hardened sequential cells	9
SEU hardened sequential cells	5
ANTENNA cells	1
TIEH and TIEL	2
Non-SEU hardened clock gating cells	1
SEU hardened clock gating cells	3
Filler cells	8
Total	**102**

IO libraries (1)

Library	Main features
DARE65T_IO	• Uni- and bidirectional LVCMOS cells • cold-spare functionality • slew rate control • programmable drive strength, pull up/down • supports 1.8/2.5V & 3.3 V supply voltage • ESD: 2 kV HBM • Breaker, filler, corner cells • flip-chip support (RDL)
DARE65T_LVDS	• Transmitter and receiver IO cells • based on 2.5 V overdrive 3.3V transistors • 2.5 and 3.3 V voltage supply • up to 400 Mbps (200 MHz)

IO libraries (2)

Library	Main features

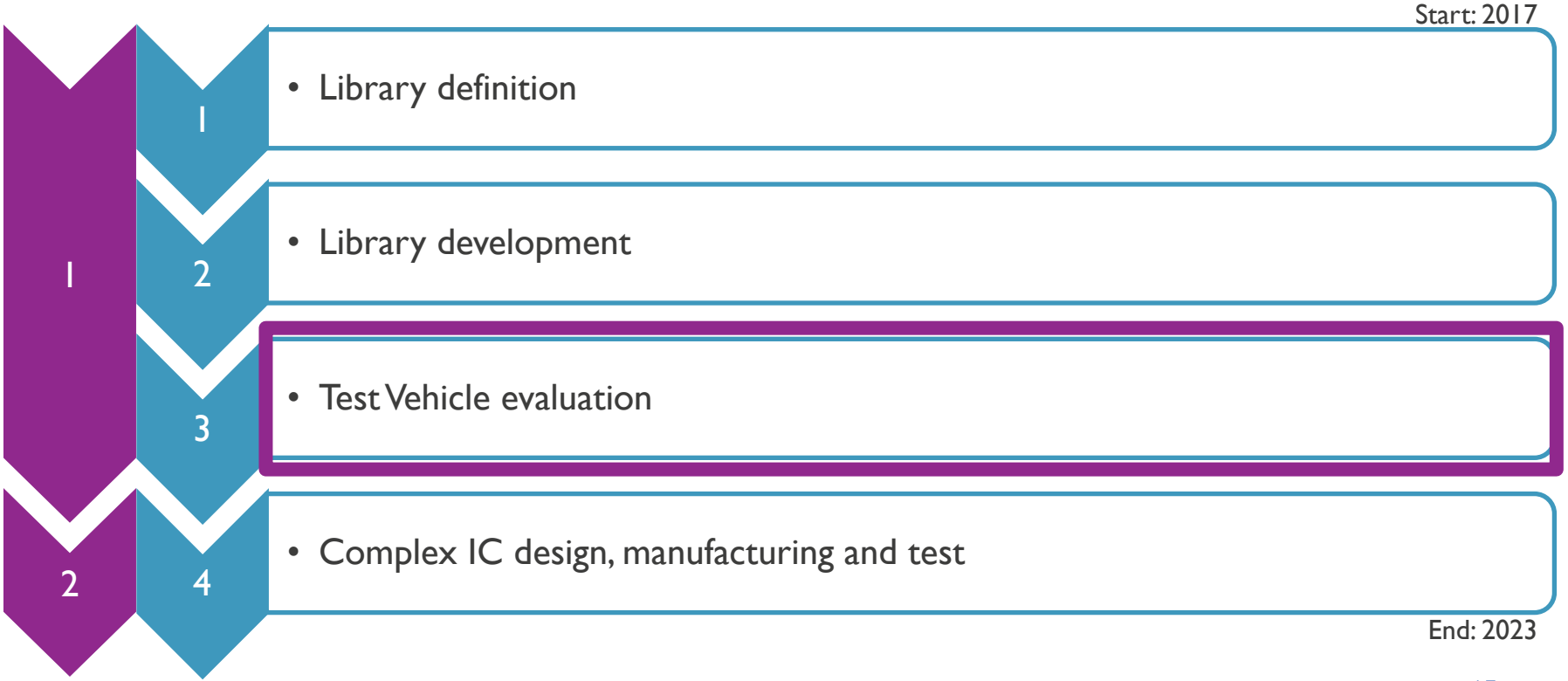
DARE65T_SSTL	• SSTL18 cells - single ended and differential receiver and transmitter
	  • 1.8V ± 5% supply voltage
	  • DDR2-800 support
	• SSTL15 cells - single ended and differential receiver and transmitter
	  • 1.5V ± 5% supply voltage
	  • Impedance calibration support
	  • DDR3-800 support

Analogue IPs

Library	Main features
DARE65T_PLL	• 25-100 MHz reference frequency • 6.25-1200 MHz output frequency • Supply voltage 1.2V
DARE65T_IVREF	• 1.2V and 2.5 supply voltages • 0.6V voltage reference output • 10uA output current reference output • Accuracy (before trimming) ± 2,5 %
DARE65T_ADC	• 10 bit resolution • Integrated temperature sensor • Supply voltage 1.2V
DARE65T_IDAC	• 12-bit Current DAC at 10MHz • Supply voltage 1.2V

ESA DARE65 project phases

Phases and tasks

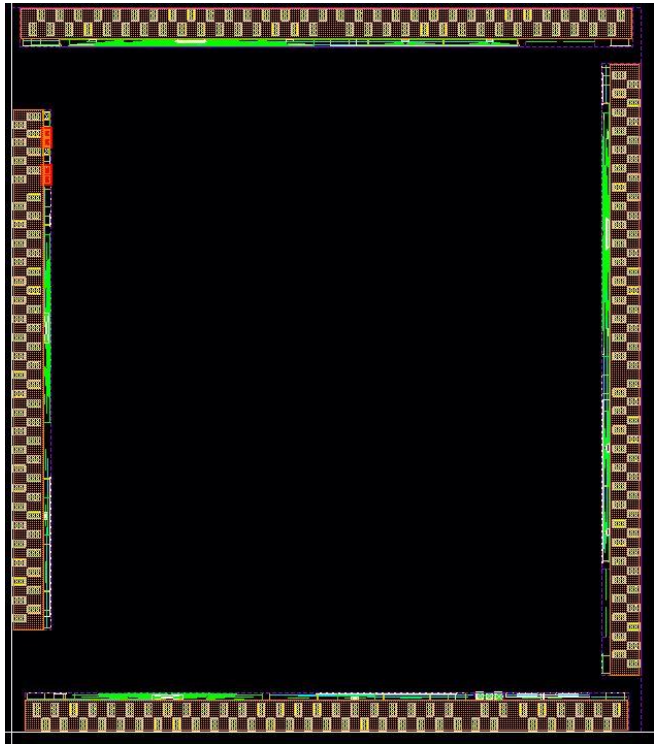


Goal

- 65nm technology evaluation (“TV_DEV”)
  - Characterize devices
  - Evaluate technology TID robustness
- DARE65 library evaluation (“TV_LIB”)
  - Functional verification of library cells
  - Electrical characterization of all IO and analog IPs
  - Irradiation evaluation of all library cells
    - TID: characterize up to 300krad (Co^{60})
    - SEE: up to 65 $MeVcm^2/mg$ through SEL testing, SEU testing and SET testing

TV_DEV

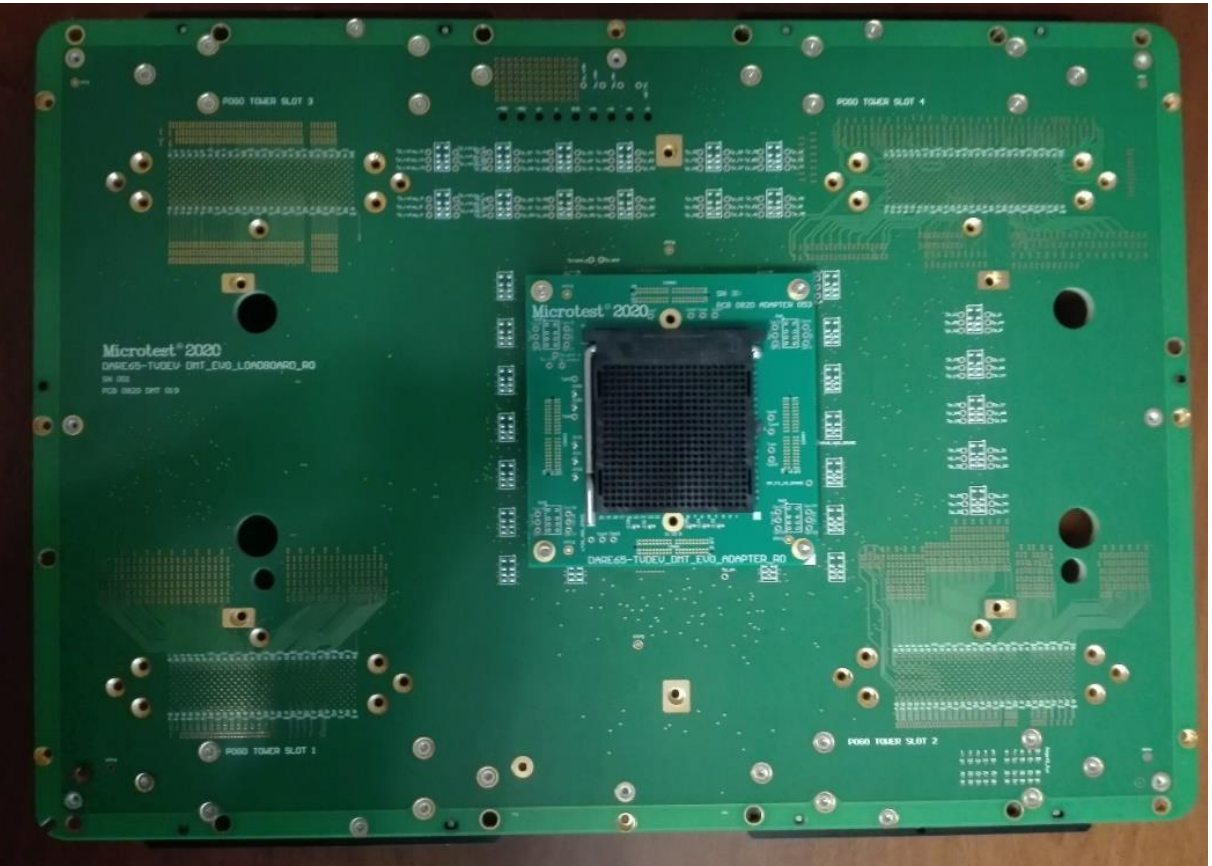
Technology characterization under TID

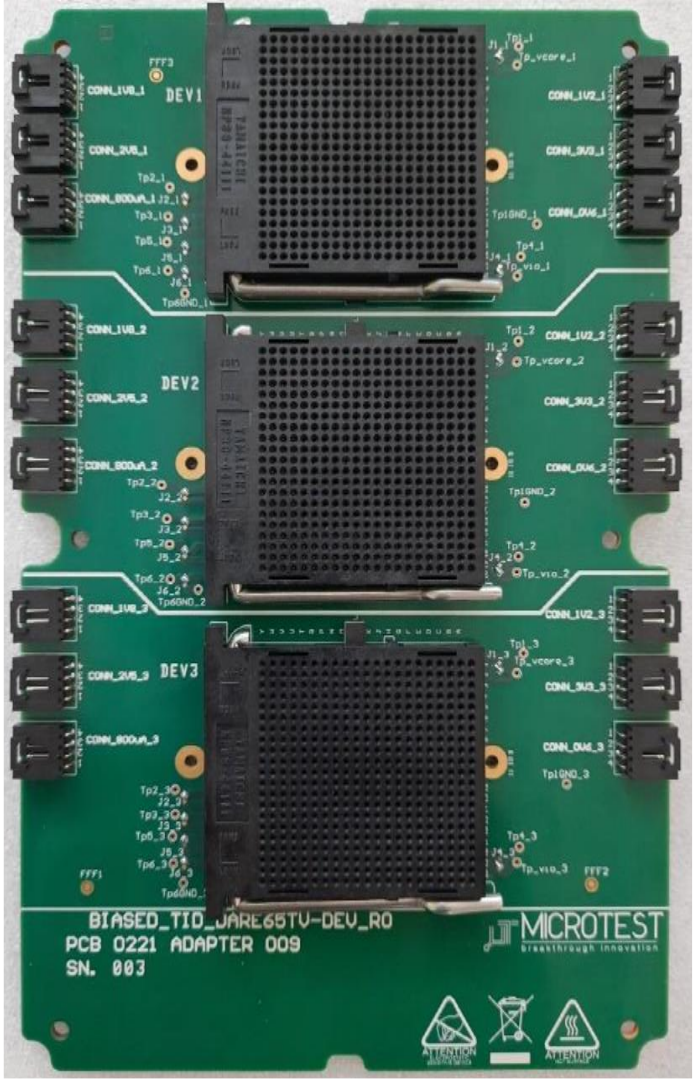


- Outer IO ring bonded directly to
  - Transistor arrays
  - Bipolar transistor arrays
  - Diodes
  - Resistors
  - Capacitors
- Left/right side: cells with no ESD protections
  - Allows for accurate leakage measurements
- Top/bottom side: cells with ESD protections
  - Backup scenario if non-ESD protected cells are damaged due to handling during debugging

TV_DEV

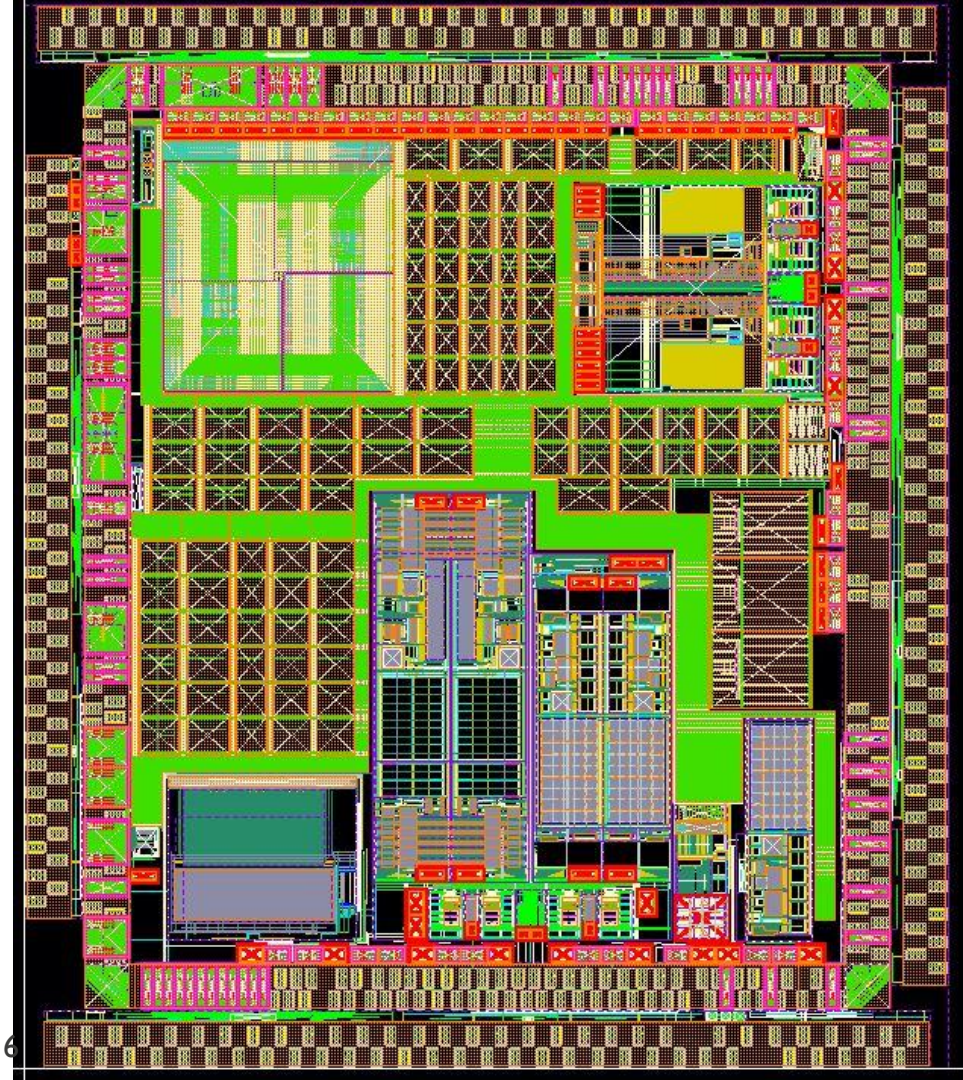
Test hardware – characterization board and TID board





TV_LIB
Design

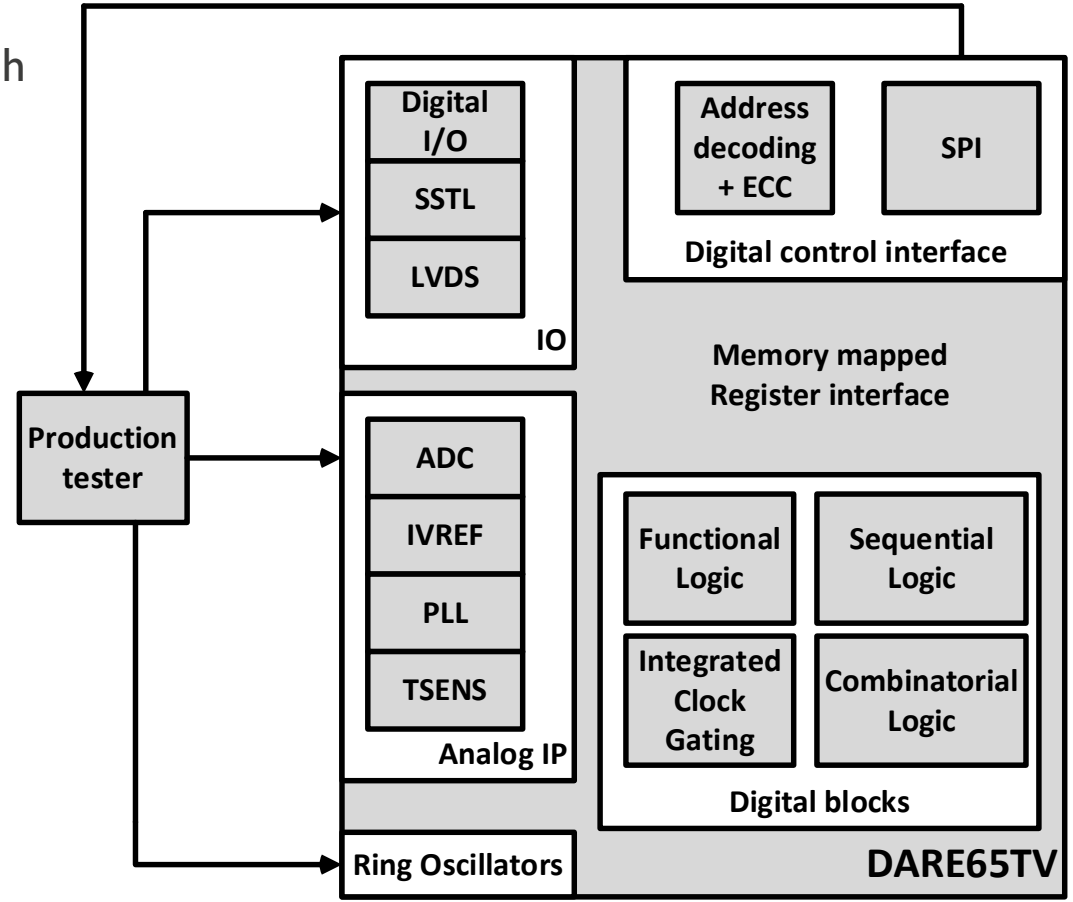
- Inner IO ring bonded to Analog-on-Top design
- All DARE65T IPs instantiated at least once
- Dedicated SEE test structure per IP
- All digital IP interfaces are memory mapped in an SPI control interface
  - For debugging, characterization and real-time readout during SEE



TV_LIB

Characterization test setup and approach

- Tester prepares analog inputs
- Tester executes digital test patterns (SPI transactions) and matches output values with expected values
- If miscompare: report failing cycle
- Map failing cycle to corresponding SPI transaction and identify failing bits in transaction
- Map bit of accessed register to actual IP pin
- During pattern execution: perform analog measurements (supply consumption, analog output values, leakage, ...)



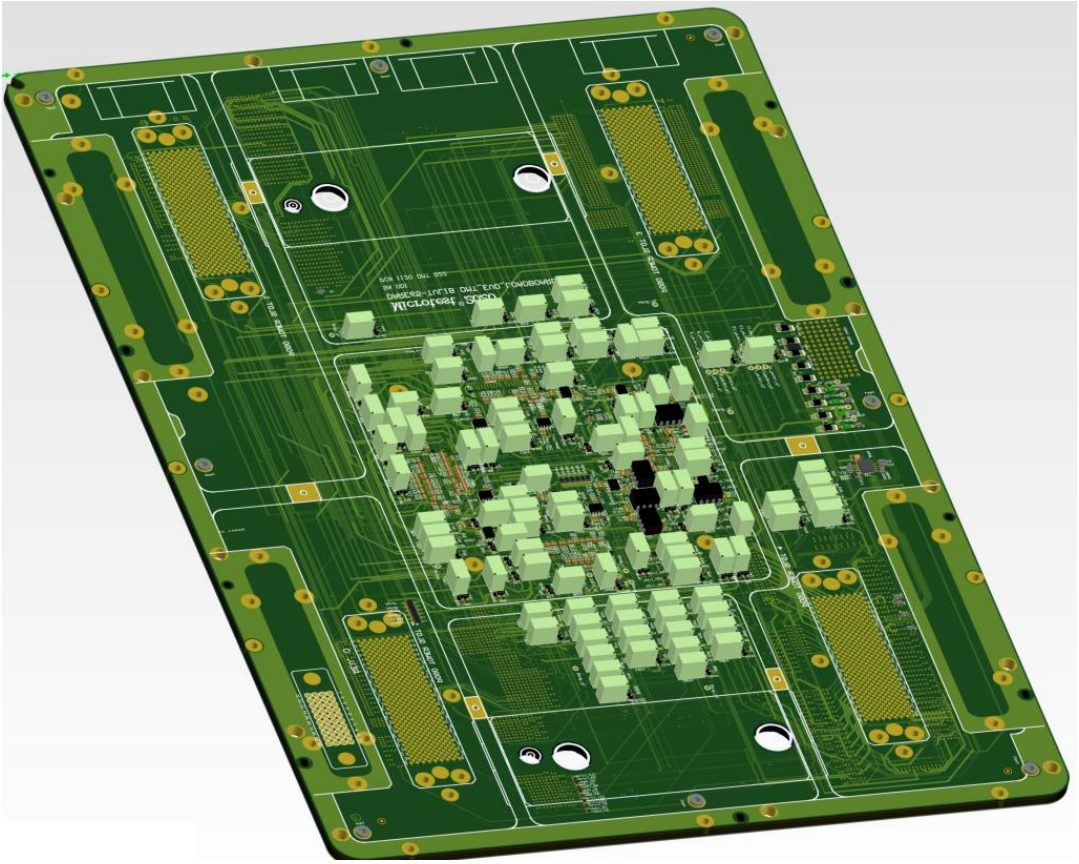
TV_LIB

SEE test setup and approach

- Similar to characterization:
  - Tester initializes device with proper SPI sequence (through pattern)
  - Beam on
  - Tester reads specific registers every 10ms to sample SET/SEU data and reports failing cycles
  - Beam off
  - Tester reads all internal state and reports failing cycles
  - Offline: map failing cycles to failing IP pins (see previous slide)

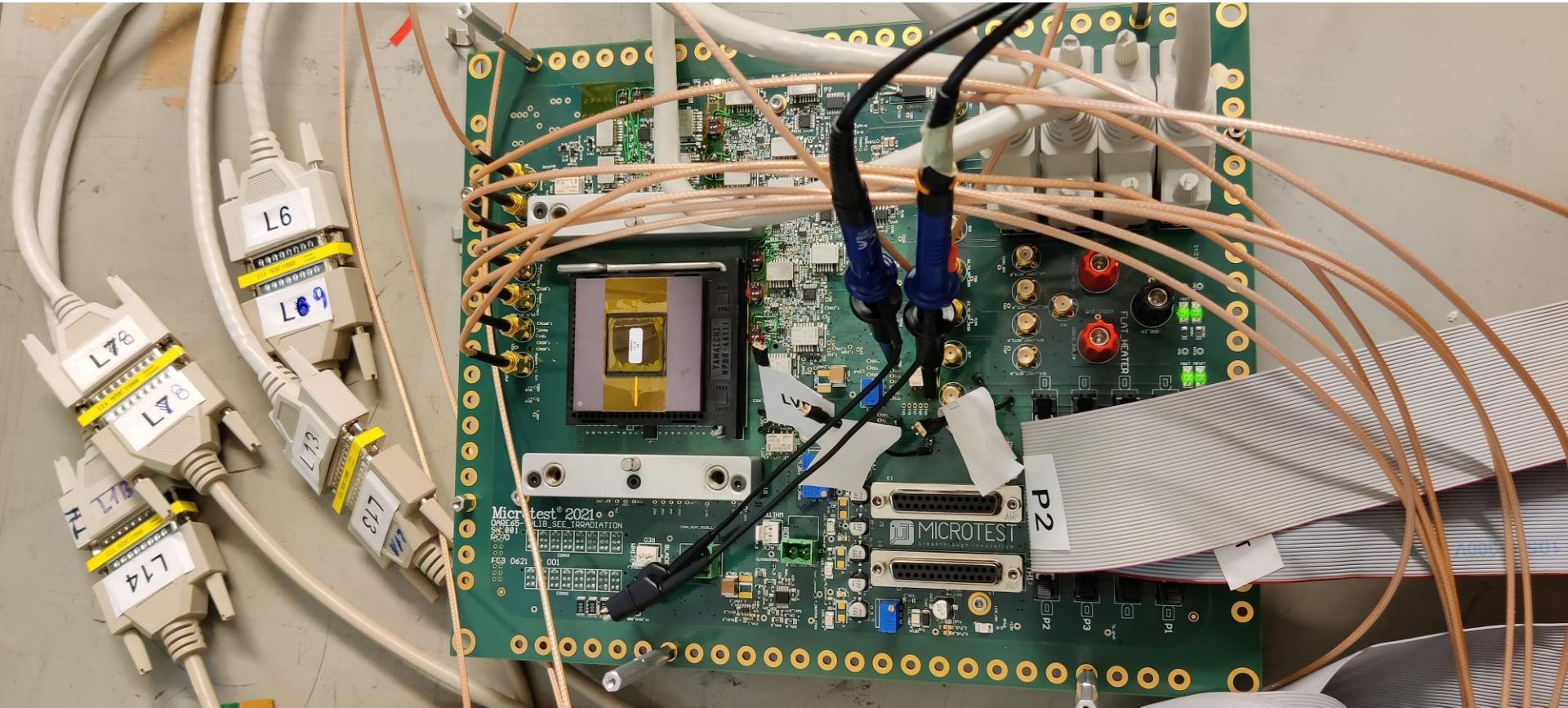
TV_LIB

Test hardware – characterization board and TID board



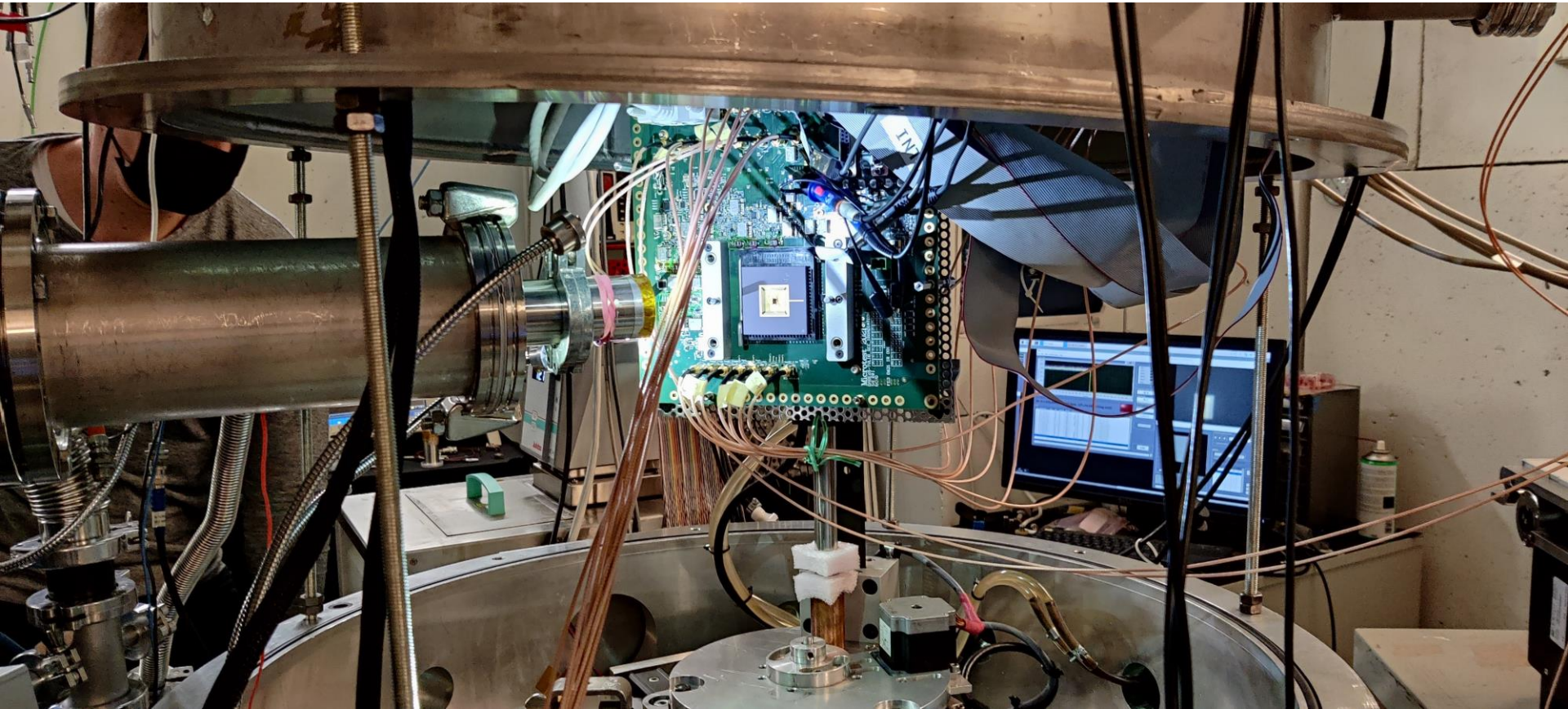
TV_LIB

Test hardware – SEE board



TV_LIB

SEE setup



Test results

TV_LIB SEE testing

- 3 samples tested
- 4 ions and tilting to get 6 LET levels per sample (7 to 65MeV)
- 5 configurations per LET level per sample:
  - 3 configurations for digital cells (DFF, XICG, combinatorial cells)
  - 2 configurations for analog cells (IO, ADC, IDAC, IVREF, PLL)
- ~90 runs in 3 days (48 hrs beamtime)
- => massive amount of data to process

Test results

TV_LIB characterization

- Extensive characterization program
  - More than 60k measurements to characterize all IPs
  - ~20 (P)VT conditions to be characterized
    - P = fixed (MPW)
    - V = [Vmin, Vtyp, Vmax]
    - T = [-40, -20, 0, 25, 50, 75, 100, 125]
  - 10-20 devices to be characterized in June
  - => huge amount of data expected

Conclusion

- DARE65 libraries have been developed, validated and irradiated
- Irradiation results will be available before Q3

- DARE65 datasheets and irradiation results can be accessed under NDA

Future work

Other IPs

Library	Main features
DARE65T_DPRAM	• True DPRAM (both ports support read and write) • Available as hard macro blocks in 5 configurations (512x40 up to 8192x40) • Up to 350MHz
DARE65T_SPRAM compiler	• Highly configurable: 32 up to 32k rows, 8 up to 64 columns, byte lane WE control, column multiplexing • Optional guard ring generation (e.g. power supply isolation for Iddq testing without impacting rad hardness)
DARE65T_DDRPHY	• DDR3.0 PHY with up to 1200 Mbit/s data rate • Embedded DLL and impedance calibration support • Up to 96 bit data, up to 8 ranks • Integrated bump grid • Fully compatible with Cobham Gaisler FTADDR DDR2/3 controller

- SRAMs are under evaluation in a second test vehicle
- DDRPHY is under development during DARE65 Phase2: "Complex IC design, manufacturing and test"

DARE65 access

- Platform launch once SRAM irradiation results available (early 2023)
- Early access may be requested
  - https://dare.imec-int.com/en/home

Thanks for attending

Questions?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