Validation, characterization and irradiation testing of the DARE65T platform

VAN DE BURGWAL, Marcel; BOUFOUSS, El Hafed; VIGNON, Bastien; BERTI, Laurent; THYS, Geert, KAKOULIN, Michael

(ASIC Design group, IC-Link IMEC, Leuven, Belgium)

***Abstract*—DARE65T is the new 65nm–based successor to the existing DARE180 rad-hard platforms. This article describes the test vehicle developed to validate, characterize and test the library cells. In particular, the test approach and dedicated test structures for SEE testing are discussed. TID testing was performed until 300 kRAD and SEE testing was performed until 75+ MeV· cm^2/mg for SEL and 65+ cm^2/mg for SET/SEU testing.**

Keywords—DARE65T, characterization, SEE, TID

I. Introduction

The DARE65T platform is an analog/mixed signal RAD-hard platform based on a commercial 65nm mixed signal low power technology. It includes an extensive variety of library cells like standard cells, IO, Single and Double Port RAM, PLL, ADC, DAC and IVREF, bringing the first advanced node sibling to the DARE platform family.

This paper introduces a test vehicle, developed to validate functionality, perform electrical characterization and ultimately perform irradiation testing (SEE and TID) to confirm the radiation hardening techniques applied during the library design phase.

The test vehicle contains test circuits to allow for analysis of TID effects on standard technology devices, and circuits for validation, characterization and irradiation testing of the library cells, both in SEE and TID.

Electrical validation and characterization includes the parameter measurement of every device and library cell. For TID, parameter drift up to 300 kRAD was measured before, during and after the campaign while the supply current of many individual power domains was monitored accurately, according to ESCC standard specifications [1]. In SEE, heavy ion particle strike effects were monitored for all library cells to confirm critical threshold and cross-section figures over a range up to 65 MeV·cm2/mg for SET and SEU effects, and up to 75 MeV·cm2/mg at a temperature of 125°C for SEL effects, complying with ESCC standard specifications [2]. Also here, individual power domains were monitored accurately. To get a detailed understanding of SEE impact on the standard cells, specific test structures were developed that allow for 10ms periodic sampling and capturing radiation effects, reducing the risk of multiple heavy ions affecting the same cell to less than 5% while reaching a total fluence of at least 1e7 particles/cm^2. In total 98 standard cell variations were selected (gate length 60 and 70nm, Vt threshold LVT/SVT/HVT and drive strength up to x16) . These circuits allow for counting the number and measure the duration of SEE effects. For each of the analog/mixed signal library cells a dedicated test circuit was designed to detect SEE effects. These cells and circuits were instantiated 1 or 2 times only, as their sensitive area is much smaller with respect to the physical area, so SEE analysis was restricted to specific parameters only.

The die was assembled in a CPGA-256 package, which is among the highest pin count standard packages generally available. Nevertheless, as the number of digital control and monitoring pins to all test structures and library cells goes far over 1000, a pin multiplexing strategy was implemented with a radiation hardened SPI interface. A regular production tester was employed to operate the digital pins through the SPI interface every 10 ms.

In parallel, it stimulates and measures the analog signal and supply pins directly connected to all analog blocks. Oscilloscopes were used to acquire waveforms of various analog interfaces and to detect SET pulses propagating from silicon to PCB.

In total over SEE 90 runs were performed for 3 samples, 6 LET levels and 5 test cases in the course of 3 days.

This article presents details about the test vehicle architecture, test circuits and approach to perform validation, characterization and irradiation tests.

II. Measurement approach

The main purpose of the test chip is to acquire test results on the DARE65T technology, to evaluate and characterize the libraries on silicon and to confirm the radiation effects mitigation approach implemented.

A. Characterization

1) Technology Characterization

Various instances of regular transistors, bipolar transistors, diodes, resistors, and capacitors were selected to get a good understanding of the 65nm mixed signal low power technology and TID effects on this process. The following parameters were obtained:

- Transistor arrays: NMOS: $I_{DS}(V_{GS})$ curve, PMOS: $I_{SD}(V_{SG})$ curve
- Bipolar transistor arrays: $V_{BE}(I_E)$ curve
- Diodes: reverse current (leakage)
- Resistors: resistance over voltage
- Capacitors: leakage

Making accurate leakage measurements on individual transistors is challenging, as ESD effects may cause permanent damage to transistors and the addition of any ESD

protecting circuitry may lead to significant leakage (possibly larger than the actual transistor leakage). A strategy was chosen to duplicate all devices and apply ESD protections to the main ones, where special precautions are used when handling the duplicated ones where no ESD protections are added .

2) Library Evaluation

For validation and characterization of the DARE65T library itself, an analog-on-top mixed signal test chip was developed. It includes a major subset of all library cells. All analog cells must be accessible through direct connection, to allow for accurate measurements of all parameters. Noise coupling is minimized by separating all library cells in separate power domains and powering down all unused domains as much as possible.

A. Irradiation

The radiation hardening of the library cells will be evaluated according to the ESCC corresponding standards [1] and [2]. Library cells are evaluated for TID and SEE effects separately, where both irradiation types require other design aspects for measurements.

1) TID

The most significant effect of TID is the MOSFET transistor threshold voltage "Vth" drift. This can lead to changed operation of CMOS circuits. For analog/mixed signal circuits, the effects may be visible in a different way than for digital cells. Such parameter drift is evaluated at specified intermediate characterization points.

A second effect of TID is circuit latchup. Since such events can potentially be destructive, any latchup effects must be monitored closely and any detection must lead to immediate power down of the device.

To achieve a TID threshold of 100 kRAD, a total of 300 kRAD must be evaluated to have sufficient margin on the observed effects. The intermediate characterization points shall take less than 2 hours to ensure no annealing effects start appearing while the testing is ongoing.

2) SEE

Single Event Effects are caused by heavy ion particle strikes hitting the region around a P/N junction. As a result, a short pulse can be observed on internal nets of the device. This pulse may propagate across the die or be exposed to the external world when detected by an IO cell.

On-die pulse detection must be tailored to the cell under test, by a dedicated test structure for that cell. The various test structures are sampled periodically to minimize the probability of double hits during SEE testing, such that the effects of individual heavy ion particle strikes can be evaluated. Complying with [2], to reach 100 events during a total fluence of $1e^7$ particles/cm^2, a sensitive area of 1000 μm^2 is required for every cell type to be evaluated. For standard cell logic (flipflops, clock gating cells and combinatorial cells) a significant amount of variations could be evaluated (variations of 60 and 70nm gate length, LVT/SVT/HVT and different drive strengths).

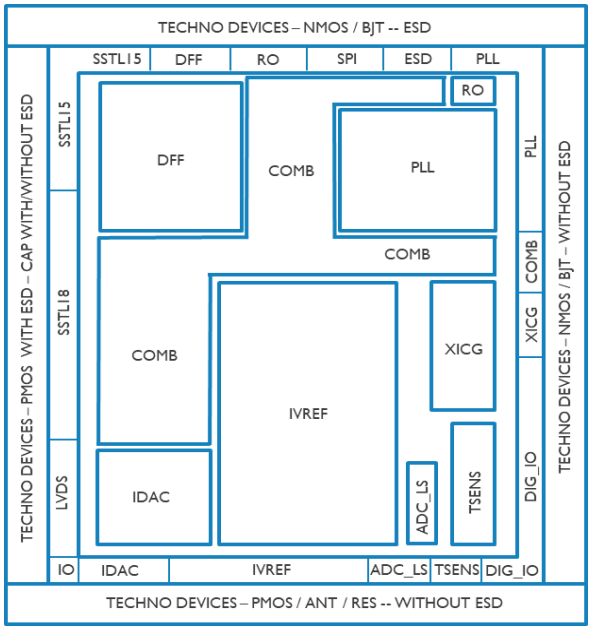

Figure II-1 Abstract floorplan of the test vehicle

The analog/mixed signal blocks has been designed to be SET free up to and 60 Mev.cm^2/mg. Therefore the sensitive area of such blocks is very small. and very low compared to their physical dimensions, so only one or two instances of every cell can be considered for testing. The idea is to catch 100 events during exposure or to reach the expected total fluence of 1e7 particles/ cm^2

III. Architecture

The overall layout of the test vehicle, including library cells and technology devices, is shown in Figure II-1.This section refers to the architecture for the DARE65T library cells, and explains how all are validated, characterized and irradiation tested with dedicated circuits.

A. Core cells

1) Ring oscillators

Using different DARE65T library flavors (LVT, SVT and HVT at 60nm and 70nm gate length), ring oscillators were constructed based on inverters, NAND and NOR cells. In addition, a set of ring oscillators operating at 2.5V were implemented to characterize standard cells based on IO transistors. The number of internal cells was selected to achieve an oscillation frequency of 1GHz, and the output of the oscillators is fed through a 7-stage flipflop based divider before connecting to an output pin.

2) Sequential logic

To obtain at least 1000 μm^2 sensitive area for D-flipflops, estimations show that more than 10k instances are required. The flipflops are implemented as a large shift register, which is split in four sections and rotated to cover four different angles of incidence for the SEE beam. 6 variants of LVT/SVT/HVT and 60/70nm cells were implemented this way. All variants were duplicated to allow for testing two D-FF state conditions at the same time, covering all test scenarios for input clock, flipflop internal state and values of (scan) data input.

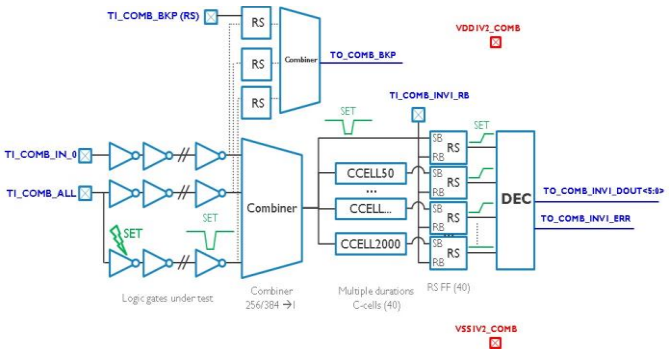

Figure III-1 SET test structure for combinatorial cells

A shift register without such sectioning was included for reference, to confirm the functionality during characterization and SEE testing.

3) Combinatorial logic

A variety of inverters, CCELLs, NAND, NOR with different drive strengths and library flavor (LVT, SVT, HVT and 60, 70nm gate length) was selected for SEE evaluation. To achieve sufficient sensitive area, for every cell type a large number of long chains of these cells were implemented (see Figure III-1).

The chain length is limited to a specific number of cell instances to allow for SET pulse propagation from the affected node towards the end of the chain, where a combiner merges all parallel branches and forwards the detected SET. Once the SET has propagated, it is fed through a network of pulse filters to identify the duration of the SET. Finally, the event is captured with latches and the pulse duration is encoded with a thermometric encoder that reduces the data rate for readout of one test structure. A backup network was added that detects pulses without qualifying the pulse duration, to avoid loss of detections in case the pulse filters would not perform as expected.

The network can be tested for production anomalies and functional correctness by manipulating the input status of the detector chains. Characterization of the pulse filters is done by generating several high frequency pulse trains with the PLL on TI_COMB_IN_0, such that the RS latches reflect the corresponding number of filter stages. With the known pulse duration (50% duty cycle of the input clock), the filter stages can be calibrated.

4) Clock gating cells

The DARE65T library includes radiation hardened clock gating cells (XICG). Three hardening levels are provided to comply with various mission profiles. For each hardening level, a test structure was included as shown in Figure III-2. With this test structure, individual strikes can be monitored real-time and the circuit is able to detect SET pulse propagation across up to 4 XICG instances. SEUs are detected through long pulse filtering. Any pulse beyond 2 ns is considered an SEU.

All chains are equipped with four alternating phases (a,b,c,d) which are grouped and monitored individually. Two monitor circuits are implemented for each phase to have minimal fault tolerance, e.g. SET/SEU on the detection circuitry can be isolated from the actual XICG chain by filtering out all detections where only one detector indicates an SET or SEU.

The chains are electrically tested by manipulating the input signal TI_CLK and repeatedly reading out the four phase results. This allows to identify any circuit failures before SEE campaign.

B. IO

Various IO cell types were developed for DARE65T. The cells are designed to be SET-free by construction, where a simple criterion is considered: if a receiver cell is not able to detect an SET pulse propagating from the remote transmitter, the pulse is not considered an SET pulse.

All IO cells are cold-spare capable, allowing for use as backup device.

1) Digital IO

The library includes a range of regular digital LVCMOS IO cells at 1.8V (underdrive), 2.5V and 3.3V (overdrive) supply levels. It features dedicated input and output cells, and bi-directional cells. In all cases, the drive strength is configurable. The input stage includes either a regular CMOS or a Schmitt trigger circuit, and variants are offered with pull up/pull down functionality. Output cells are offered with optional Slew Rate Control. Since the bi-directional cell

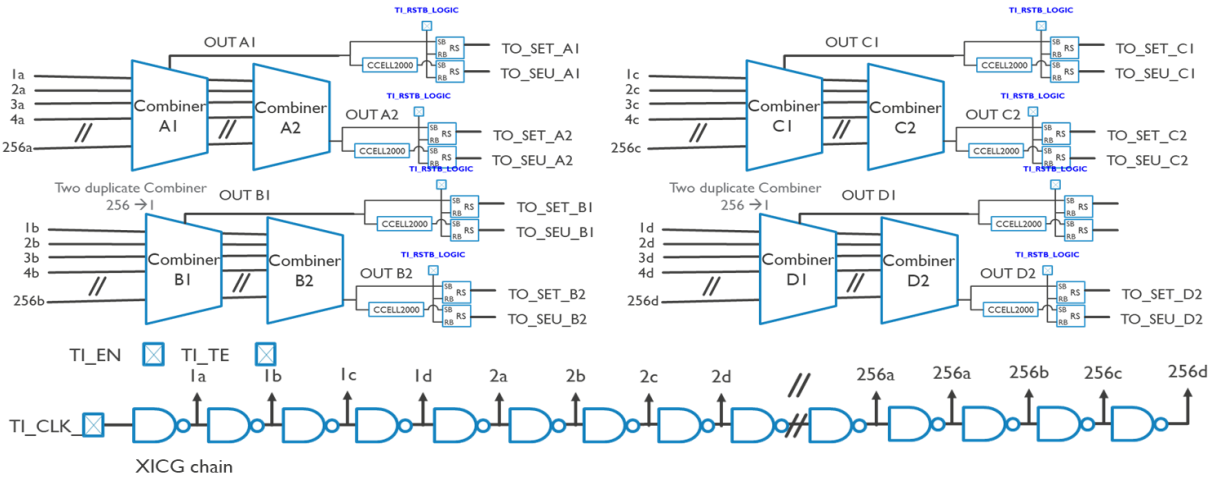

Figure III-2 SET/SEU test structure for clock gating cells

features all functions of dedicated inputs and dedicated outputs, only CMOS and Schmitt triggered variants of the bidirectional cell are included on the test vehicle.

SET detection on the IO input is done with a RS latch. The output is monitored through an external counter, as no core cells can be used to monitor the analog signal levels. In two steps, the cell is tested for input stage SET sensitivity (low and high logic states) and for the output stage SET sensitivity (low and high logic states).

2) LVDS

LVDS cells operate at 2.5V and were designed to reach up to 400 MHz frequency. To allow cold spare operation, no termination resistor is embedded in the receiver. Termination is performed externally on the test board. (see Figure III-4).

For SET testing, the LVDS Receiver (RX) core output is connected to an RS latch. The Transmitter (TX) output has been monitored using an oscilloscope. Here, termination is applied on the test board such that the receivers receive a correct input signal. The LVDS RX and TX are SEE tested in low and high logic state, for comparison of the sensitive area in both modes.

3) SSTL

Designed specifically for DDR memory interfaces, SSTL cells are offered for DDR2 (operating at 1.8V) and DDR3 (operating at 1.5V). For both standards, a receiver-only cell (RX) and a receiver/transmitter (RXTX) combined cell are offered with single ended and differential implementation variants. These cells have been designed to toggle up to 800 MHz, or 1600 Mbps, supporting all DDR2 and DDR3 standard rates (up to DDR2-1066 and DDR3-1600). Note that validation on this test vehicle is limited to 100 MHz operation due to wire bonding assembly (see Section IV).

The SET test structure for SSTL (differential) is identical to the LVDS test structure. Again, the RX was monitored with a latch and the RXTX was monitored externally with an oscilloscope. The test was performed with all combinations of RX logic low and high levels, and RXTX output logic low and high levels.

C. Analog blocks

1) IVREF

In the DAR65T platform, two current/voltage references are provided: IVREF1V2 and IVREF2V5. The IVREF1V2 operates at common 1.2V core voltage, where there IVREF2V5 operates at common 2.5V IO voltage level. Both can provide up to 5 current references (10uA), a voltage reference and a differential temperature indication. The IVREF block serves as a support block for various others: LVDS, ADC, and IDAC.

For SET testing, a dedicated high bandwidth buffer (>500 MHz, and a capacitive load up to 50pF) was developed that allows to monitor the current and voltage references with an external oscilloscope. Since this buffer is power consuming and oscilloscope channels are limited, all current and voltage outputs of the both IVREFs are multiplexed to the SET buffer.

The SET buffer was specifically developed for fast pulse response to an external oscilloscope. Before SET testing, the SET buffer is characterized by applying an analog step and monitoring the output step response with an oscilloscope. The achieved bandwidth is calculated from the measured rise time.

2) ADC and Temperature Sensor

The ADC is a 14-bit low-speed (1 kHz) ramp-type converter. It has a differential input range of +-1V and generates a 14-bit 2's-complement integer value on the core output (~10 ENOB). The ADC can be used as external ADC, or as an on-die Temperature sensor. To configure it as a temperature sensor, the ADC must be connected to a temperature depending voltage output of the IVREF.

During SET testing, the digital interface is checked for sudden bit flips, by connecting latches to these output pins. The ADC is configured in a continuous sampling mode and the input voltage is tied at fixed levels where the digital interface can be monitored (e.g. the "noise" bits toggling frequently should be avoided for SET monitoring).

3) IDAC

The 10 MHz current DAC with 12-bit input is based on a combined 8-bit thermometer DAC (MSB) and 4-bit binary DAC (LSB), driving up to ~10 mA per output.

For SET, the IDAC is driven in specific conditions (minimum, middle, and maximum output current) and any

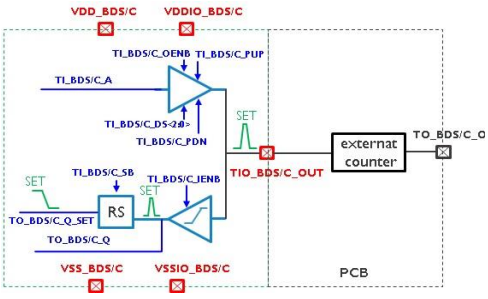

Figure III-3 Test structure for digital IOs

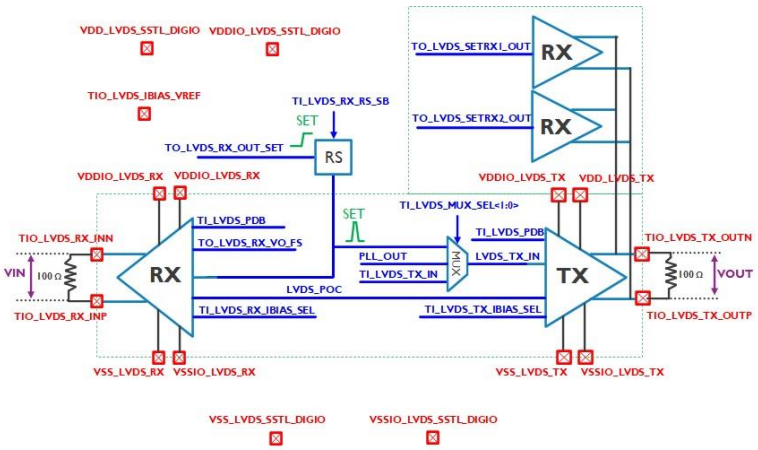

Figure III-4 SET test structure for LVDS

SETs on the IDAC are monitored with an oscilloscope on its differential output.

4) PLL

The last analog block in the test vehicle is a digital PLL with input clock range of 25-100 MHz, VCO operation frequency between 800 MHz and 1200 MHz and output clock generation between 6 MHz and 1200 MHz. Frequency synthesis is done through input, loop and output dividers with 2N multiplication and division factors. The PLL is hardened against SET/SEU through triplication of internal digital circuits (dividers) and hardening of the analog subblocks.

The main parameters to be tested under SET are the jitter and the extra clock edges. These are monitored by implementing two PLLs in parallel, with identical inputs. All analog output signals are routed with matched length and capacitance to a triplicated filter network that detects difference in clkout levels between the PLLs. The high and low mismatches are divided in 4 categories (>100ps, >150ps, >200ps and >250ps) and registered in a high frequency counter bank. The PLL's output divided is bypassed such that the VCO is exposed directly to the filter network. Whenever one of the PLL VCOs is affected by SET, the clock edge arrival at the filter network will differ and be forwarded by the XOR cell as a short pulse. All counters with corresponding minimum pulse duration filter will increment as long as the VCOs are not aligned. This way, the jitter itself as well as the number of cycles until recovery can be characterized.

Next to monitoring clkout with the pulse detectors, the lock detector is monitored with an oscilloscope. Whenever the jitter is too large, the PLL will lose lock and the oscilloscope should detect a pulse with similar duration as indicated by the filter network.

D. Digital Control

All library cells are controllable and monitorable through a memory mapped register bank. Using an 8-bit memory map, all control (input) pins of analog blocks as well as monitor (output) pins of the analog blocks are accessible. All pins are packed in register addresses as much as possible, to keep the memory map size minimal and maximize the read/write operation time.

Read and write operations are executed through an SPI link interface with custom command protocol including a set of single-cycle read/write operations and optimized burst operations to perform multiple read/write operations at consecutive addresses, saving up to 75% of bandwidth (see Table III-1). To facilitate the burst operation, the memory map is organized such that the set of register addresses to be acquired regularly during this campaign are compacted in a short block of consecutive memory addresses.

The SPI interface is used periodically to acquire internal state information during the SEE campaign. Therefore, it is implemented with maximum radiation hardening considerations (Triple Mode Redundancy as well as circuit level implementation with hardened standard cells). Since the SPI IO cells may be sensitive to SEE, every transaction is protected with a CRC byte on both the MOSI (master out, slave in) and MISO (master in, slave out) interface pins. When the device detects an incorrect CRC byte, it flags an interrupt line to the master, indicating it is not able to process any subsequent transactions. Similarly, along with the response stream towards the master, it appends a CRC byte to the end of the stream, enabling the master to identify any SEE events.

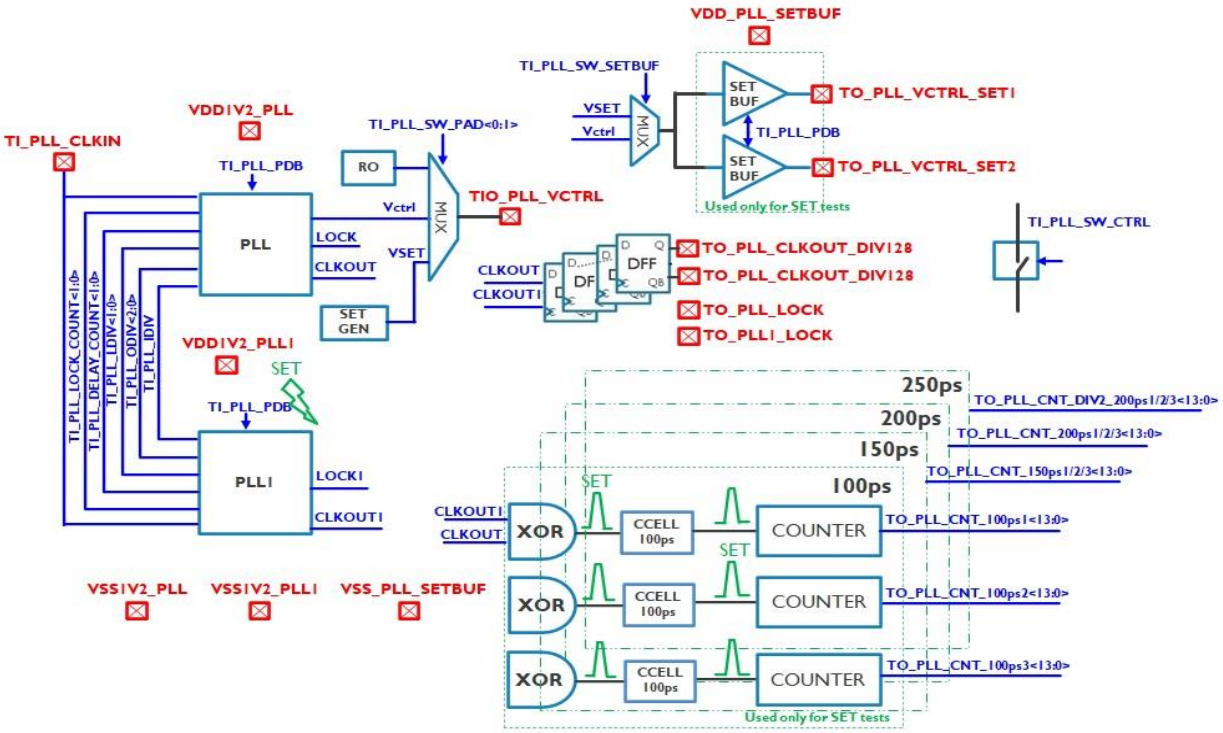

Figure III-5 SET test structure for PLL

Table III-1 SPI protocol

Op code	Description	Usage
S33	Read only (single byte)	MOSI 33<addr><00><CRC> MISO 00 00 <val> <CRC>
S69	Read+write (single byte)	MOSI 69<addr><val><CRC> MISO 00 00 <val> <CRC>
S0F	Read burst (<256 bytes)	MOSI 0F<addr><len><00>*<CRC> MISO 00 00 <val>* <CRC>
S66	Read+write burst (<256 bytes)	MOSI 66<addr><len><val>*<CRC> MISO 00 00 <val>* <CRC>

Although the SPI interface supports a 10 MHz operation speed, it is operated only at 500 kHz to ensure same time base for operations is used on characterization as well as during SEE, where long cables are required to connect from the tester to the test vehicle.

IV. Assembly and Test

Both assembly options (TV_DEV and TV_LIB) were bonded in the same CPGA-256 package, however in different numbers.

1) TV_DEV

For TV_DEV, 24 samples were bonded, and all samples were fully characterized. Although handling and early revisions of the test program did cause ESD damage, no less than 14 samples were fully characterized.

From this set, 11 samples (5 biased, 5 unbiased and 1 reference sample) were selected for TID testing up to 300 kRAD at high dose rate (450 rad/h). At 8 intermediate TID levels the samples were recharacterized, and after reaching 300 kRAD 24 hours of annealing at room temperature and 168 hours of annealing at 100°C with intermediate recharacterization were performed to record all parameters. TID testing was performed in April 2021 in the Alter Technology facilities (Spain). During the course of 5 weeks, test data was acquired and processed. However, as the test results are subjects to an NDA, no data or conclusions can be published.

2) TV_LIB

Assembly for TV_LIB included 44 samples, where for 10 samples no lid was mounted (reserved for SEE). Here, yield was much better as all IOs are ESD protected. Validation testing and preparation for characterization took significant more time, due to test hardware and software development, silicon debugging and finetuning the test setup.

TID testing was performed in September 2021 in two parallel campaigns. The IVREF relies on bipolar transistors and therefore a low dose rate campaign (36 rad/h) was performed, along with the high dose rate campaign (450 rad/h) for the rest of the library cells. All characterization points were executed with a reduced scope test program, as a full device characterization will take too much time to respect 2 hours of annealing time in between irradiation steps for all 10 irradiated devices.

During SEE testing, the SPI interface is used to initialize the device before the beam is activated, then readout every 10 ms several key registers to acquire a high time resolution snapshot of the SEE effects occurring over time. The amount of data exchanged during such interval depends on the test; especially for the combinatorial logic, a large amount of read and write operations are performed to get data and reset internal counters. Running at 500 kHz SPI clock frequency, above 9 ms out of 10 ms period is used to access the registers in several test cases. Once the total fluence reaches 1e7 particles/cm^2, the beam is stopped, and final state of the device is retrieved. This takes longer than 10 ms but is not critical.

Testing was performed with production tester, executing offline generated VCD waveforms and matching device response. Any failing cycle is registered and immediately after the SEE run, the failing cycles are processed with a software tool. Experiments showed that the full production tester memory (20M failing cycles or more) could be processed in less than 30 seconds, allowing for fast initial decision making. Based on the amount of failures and the nature (e.g. which register operation is failing, is it related to other registers and whether failures are likely) a decision is made whether the results are OK or the run must be repeated.

SEE testing was done in January 2022 in the RADEF facility in Finland. 3 devices were irradiated in 6 different configurations (1x SEL, 3x SEU and 2x SET) at 4 ion/angle levels with 0 and 45° tilt to get 6 LET levels. The processing tool showed to be very helpful as the amount of SEE events observed during the irradiation of the first device were very close to the expected SEE numbers. Altogether, over 20 GB of test data was captured and stored.

Full device characterization has not yet been completed. Therefore, processed characterization and irradiation results are not available yest.

V. Lessons Learnt (so far)

1) Implementation flow

The test vehicle was implemented in an analog on top design flow, with several blocks designed and implemented with digital flow. Verification of subblocks and circuits was done for all parts, however a full analog-on-top verification was skipped due to duration. At this point, some design flaws in the test circuitry were identified during silicon debugging.

2) Design mistakes

In the SET detection circuits several small issues were identified that complicated the testing. For example, the latches capturing SETs on the LVDS TX and SSTL RXTX via the on-die bypass RX cells were not included. As a result, these detections had to be performed with external oscilloscopes, leading to degraded SET detection capabilities.

3) Hardening of SPI interface

Although the internal register bus and the SPI communication protocol had been developed with ultimate hardening in mind (selection of standard cells with highest hardening level, triplication of all circuitry and access patterns during readout), two mistakes were identified during SEE campaign.

- An SET on an SPI input pin during transmission may cause a CRC error detection by the onboard SPI controller. However, the tester is unable to dynamically check the error indication and reset the device in a controlled state, leading to missing read/write operations in the device. As a result, the affected irradiation run must be repeated after final readout.
- The register bus is hardened at flipflop level (address+data storage, input/output flipflop to analog

IPs) but combinatorial logic is not triplicated (address decoding, register field unpacking). As a result, during higher level LET testing several occasions of wrong read/write operations were identified, resulting in unusable data from that point.

4) Test pattern definition - characterization

For characterization, many interactions between cells exist. Definition of the exact initiation sequence as well as measurement points occurred to be much more complicated than expected.

The SEE test program was less complex per IP because only steady state testing was performed. However, to get maximum results during minimum beamtime, all IPs must be tested individually in parallel. Combining all instructions in a single test pattern, respecting periodic readout interval, turned out to be more complicated than expected.

5) Large amount of IO test conditions during SEE

To test the IO cells and analog blocks with enough representative conditions during SEE, multiple instances of the cells are required in parallel or multiple runs must be scheduled consecutively. After a beamtime versus die area tradeoff we decided to fix the die area and increase the beamtime. Initially the number of test runs to cover all IO / analog conditions was 8, and after accepting some loss of coverage, was reduced to 2. A better tradeoff should be made earlier in the design process.

VI. Conclusion

In this article, we presented the architecture of the DARE65 Test Vehicle with all standard cells, IO cells and analog IPs available in the DARE65T platform. We presented the characterization and test approach, and our findings on the process.

VII. Further work

Once the data analysis for TV_DEV and TV_LIB has been done, all libraries will be updated. Next to the libraries mentioned in this article, a second test vehicle was manufactured with various hard-macro DPRAM memories and blocks generated with the DARE65T SPRAM Memory Compiler. We have recently started developing the test hardware and software and expect to perform irradiation testing later this year.

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- RADEF (Jyväskylä, Finland) for the SEE campaign execution, https://www.jyu.fi/science/en/physics/research/infrastructures/accelerator-laboratory/radiation-effects-facility

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