Rad-hard Microcontroller with Open Access ISA for Space Applications

H2020 Programme Space Theme

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Agenda

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- MORAL Project Introduction
- MORAL Microcontroller
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  - Digital Design
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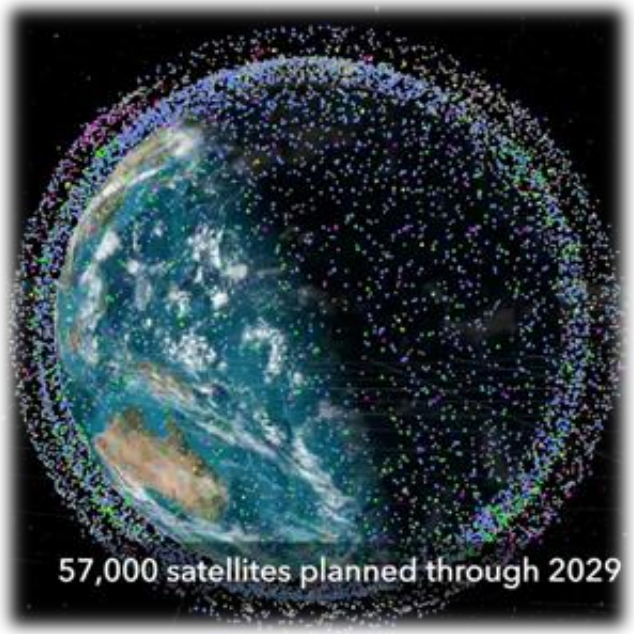
  - Memory and Analog IPs
  - Evaluation Board
- MORAL Software
  - PEAKTOP Toolchain
  - Compiler and RTSK
- Development Status

Background

Small satellites – 2030 and beyond

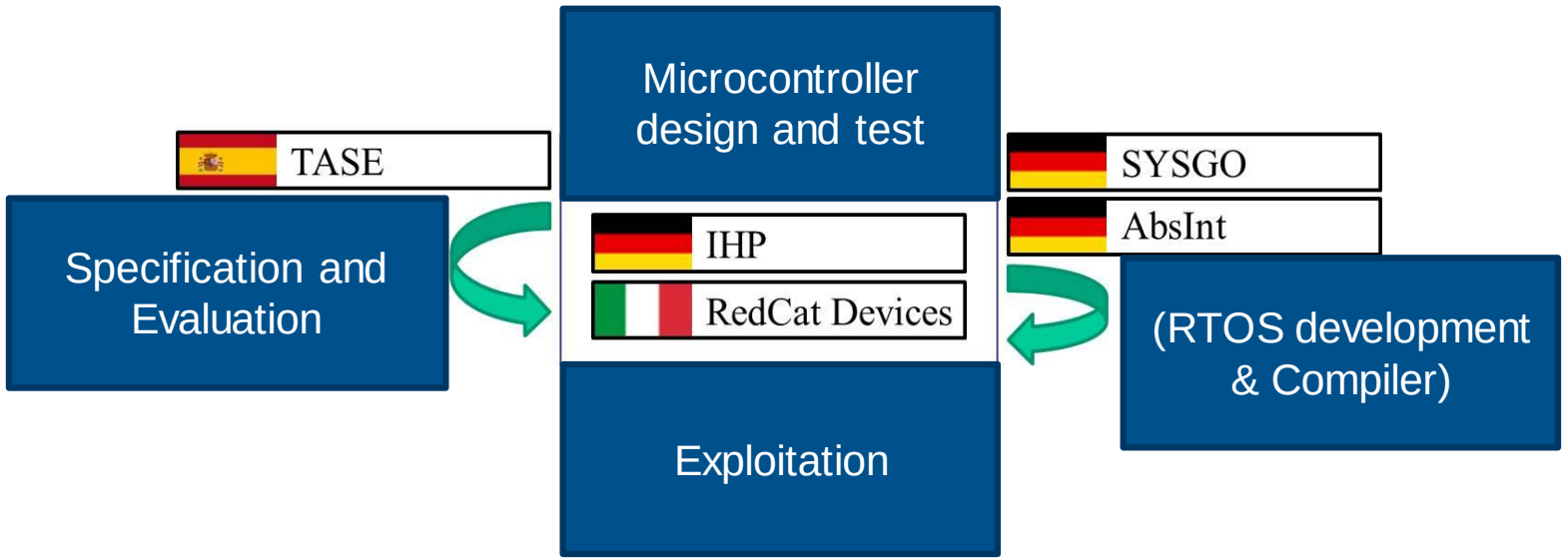
- Low-cost small satellites (from 10 kg to 500 kg)
  - Potential for scientific research and practical applications
- Small satellite modern applications
  - Satellite swarms or constellations replacing large satellites
  - Augmented satellite based navigation systems
  - Satellites in commercial aviation
  - Commercial satellite imagery based services
  - Robotic servicing technologies for space applications
- Mainly powered by traditional electronics
  - Increased capabilities, but reduced reliability



Introduction

MORAL Project – H2020 Space Theme Programme

- Duration from 01. January 2020 to 30. April 2023 (40 months)
  - Funded by the EC - GA No. 870365
- Two main objectives
  - Develop a completely European, ITAR-free microcontroller for space applications
  - Exploitation plan for entering the market
- 5 partners



Introduction

MORAL in a nutshell

- Microcontroller based on the novel PEAKTOP architecture, including a novel Instruction Set Architecture (ISA)
- Formally-verified C compiler, RTOS, and toolchain
- Demonstrator board
- Irradiation tests
- Aggressive exploitation plan for bringing the product into market

MORAL Microcontroller - PEAKTOP

Why a new processor core architecture?

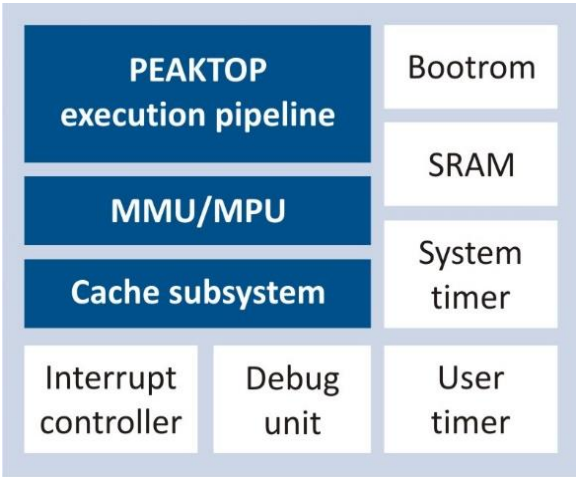
- IHP's PEAKTOP architecture
  - Freely available
  - Complete control over each aspect of the microcontroller
  - ITAR-free
  - Scalable (e.g., to 64-bit)
  - More than TMR and ECC features

- PEAKTOP provides mixed criticality support
  - Multiple functions with different criticalities and assurance levels to co-exist in the microcontroller architecture
  - General Purpose Register (GPR) banks can be dynamically grouped
    - Dual-, Triple- or Quadruple-Modular Redundant (DMR/TMR/QMR) module to increase the fault tolerance

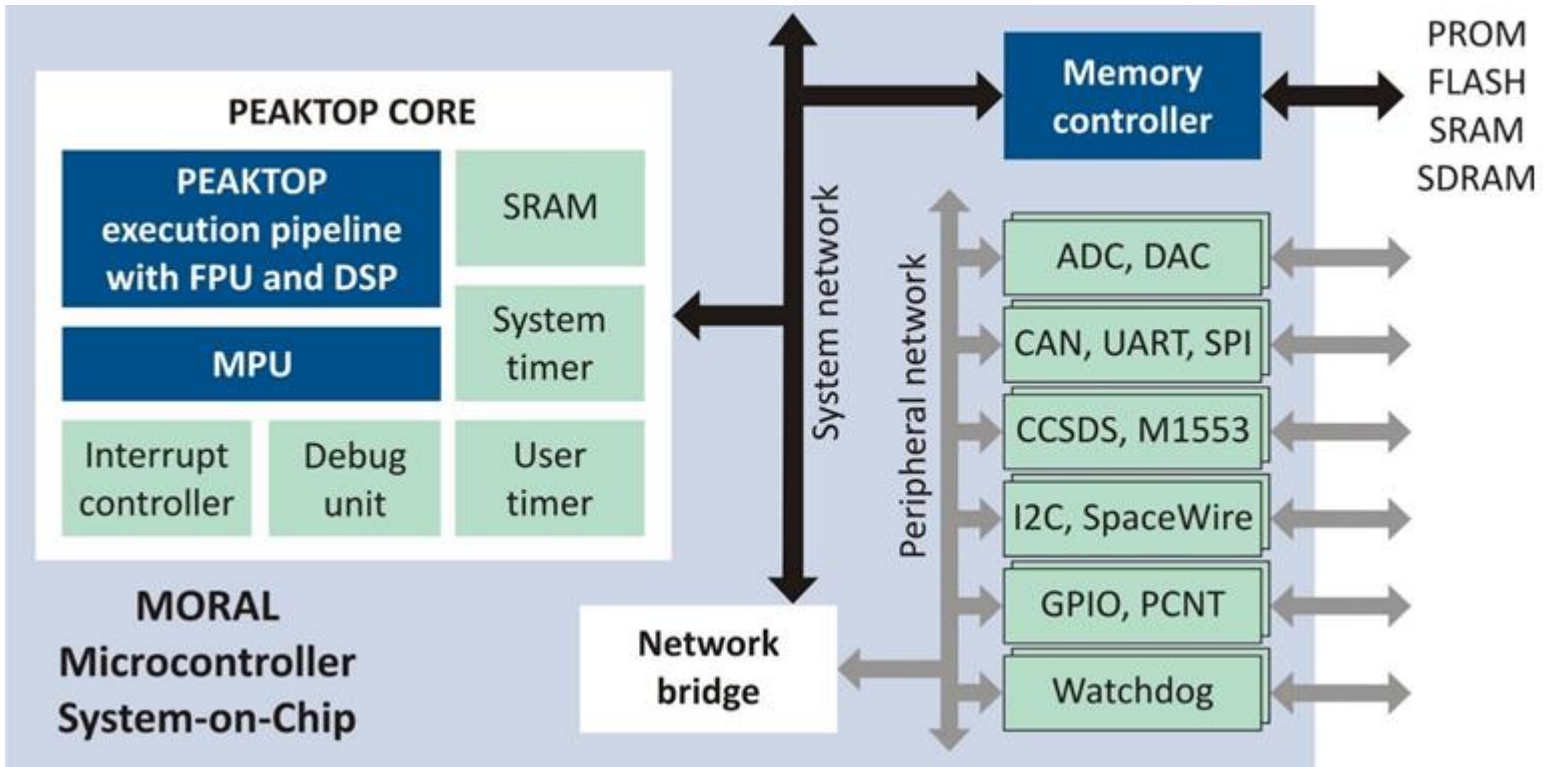
PEAKTOP Architecture

- IHP's own processor
  - Open ISA

- Core architecture characteristics
  - RISC architecture
  - Up to 64 GPR
  - IEEE 754 compliant Floating Point Unit (FPU)
  - Optional Digital Signal Processing (DSP) extension
  - New ISA is fully **orthogonal**, **regular**, and **circular**
  - Multiprocessing support (cache coherence, synchronization support, atomic transfers)
  - Configurable addressing space: up to 64-bit; virtual address space is up to 128-bits
  - 32-bit wide instructions up to 3 operands
  - 2-level Memory Protection Unit (MPU), or (optionally) 2-level Memory Management Unit (MMU)
  - Optional L1 (separate data/instruction) cache, and L2 cache

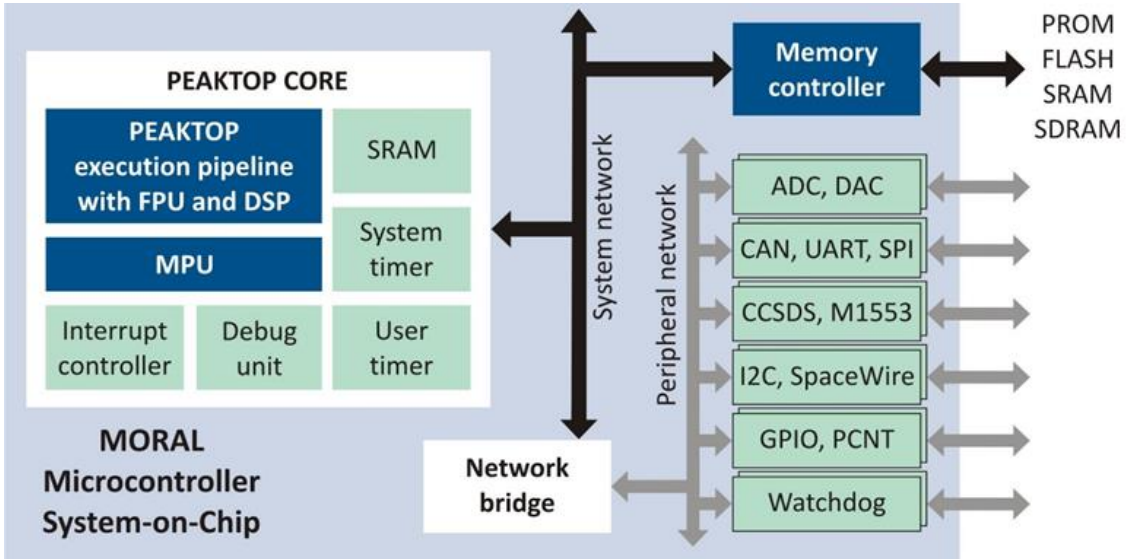


MORAL Microcontroller – Specification



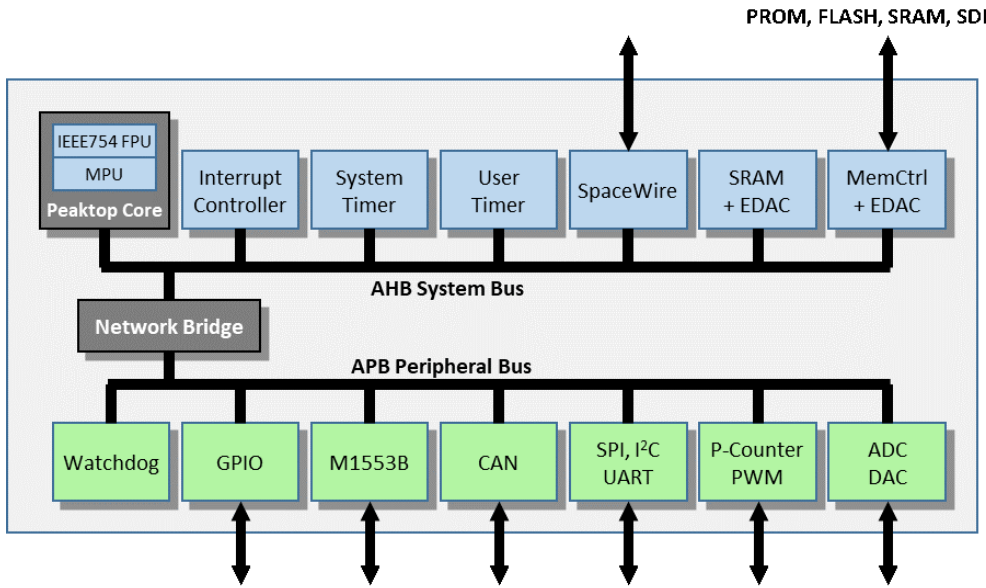
MORAL Microcontroller – Specification

- 256/512 Kbyte SRAM
  - Error Detection and Correction (EDAC) protection unit
- 1 x Interrupt Controller
  - 32 interrupt lines
- 6 x Timers
  - 2x system + 4x user timers
- 64 x GPIO ports
  - Shared with internal peripherals I/Os



MORAL Microcontroller – Specification

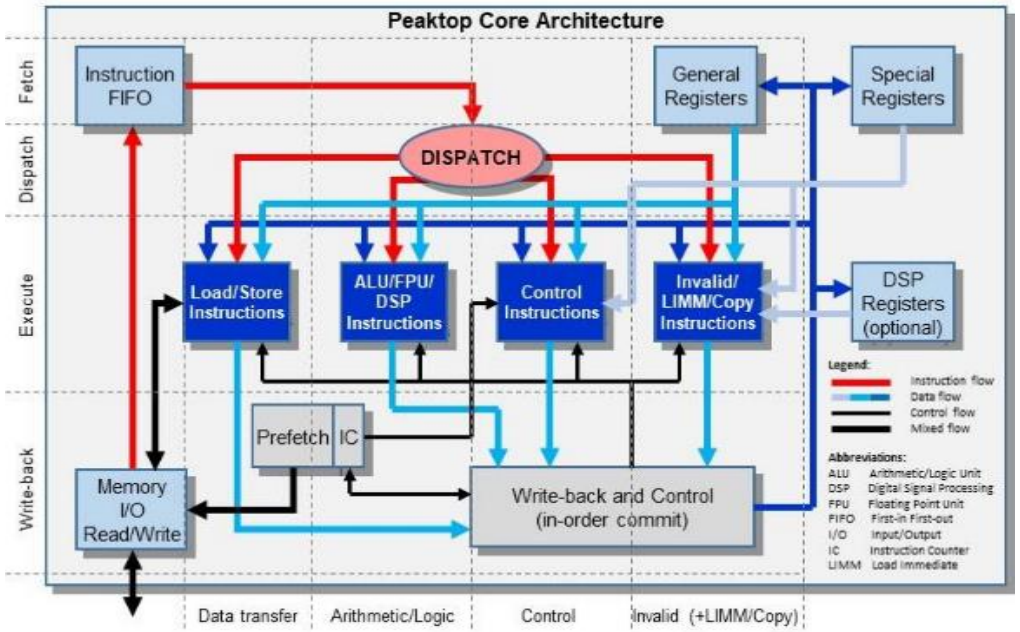
- Peripherals
  - 1 x 8-channel 12-bit ADC
  - 2 x 12-bit DAC
  - 2 x CAN 2.0 modules
  - 4 x UART interfaces
  - 2 x SPI interfaces
  - 2 x SpaceWire interfaces (incl. RMAP protocol)
  - 1 x MIL-STD 1553C bus interface (incl. redundant bus)
  - 2 x I2C interfaces
  - 1 x 8-channel PWM generator
  - 4 x Pulse counters
  - 1 x Watchdog timer

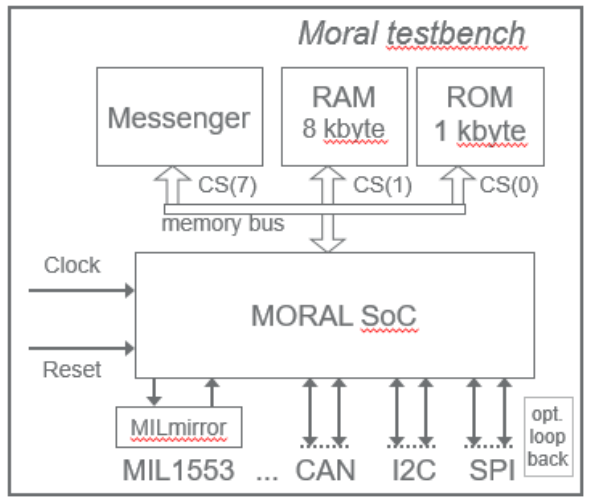


- Rad-Hard Specification
  - Total ionizing dose (TID) **100 krad** (Si)
  - Single event upset (SEU) for the processor's digital core **>30 MeVcm²/mg**
  - Single event latch-up (SEL) >60 **MeVcm²/mg**

MORAL Microcontroller – Digital Design

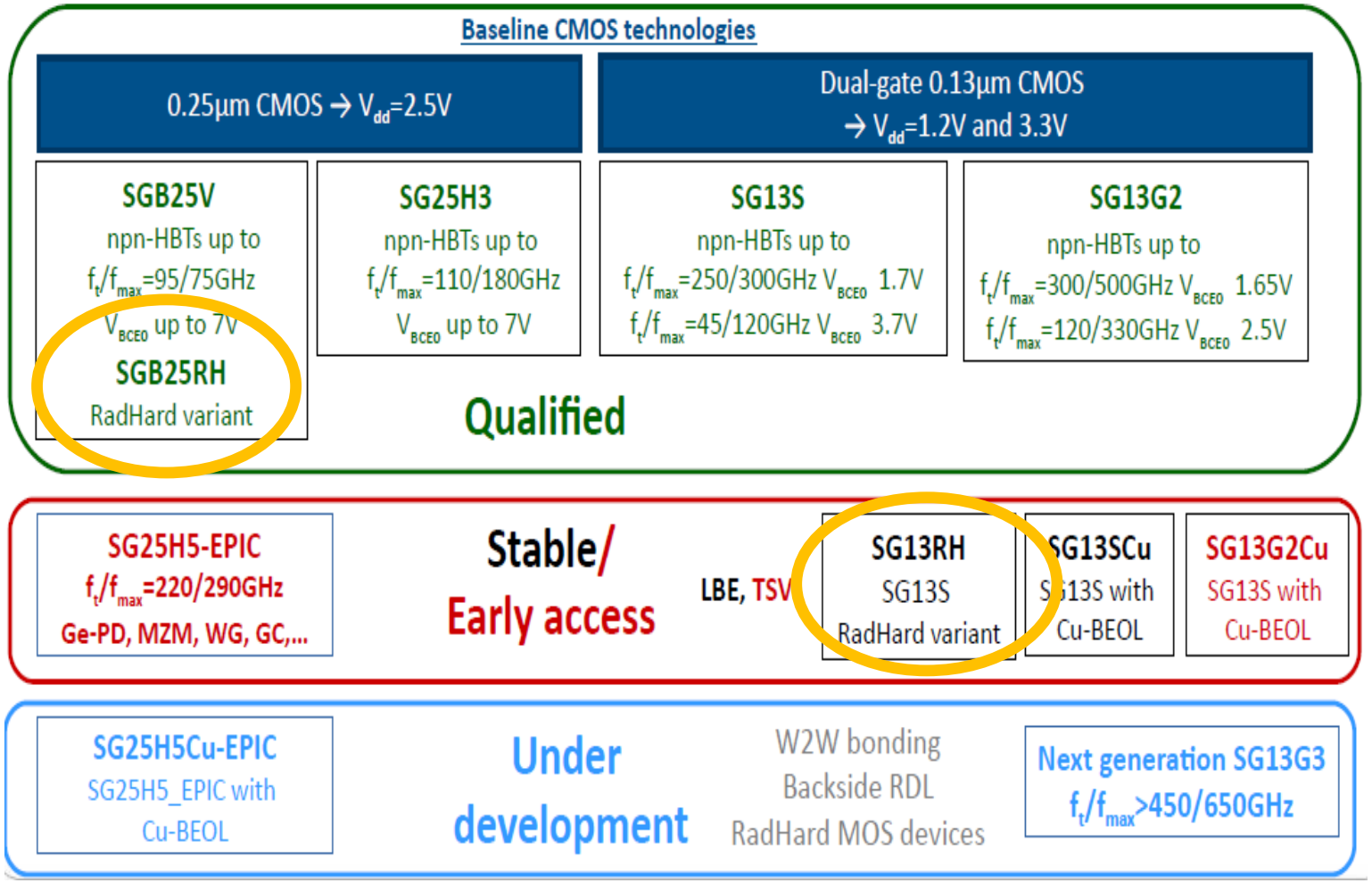
- Processor core design
  - PEAKTOP previously developed, implemented, and tested in IHP 130nm technology
  - FPU design and redesigned of MPU to support the RTSK needs
- Peripherals design an integration
  - MIL-STD 1553C designed at IHP
  - Peripheral in the specification integrated
- Verification
  - Carried every step of the design, from RTL simulations to post-synthesis, and in FPGA





MORAL Microcontroller – Technology and PDK

Commercially available IHP Technologies – Multi Project Wafer (MPW)



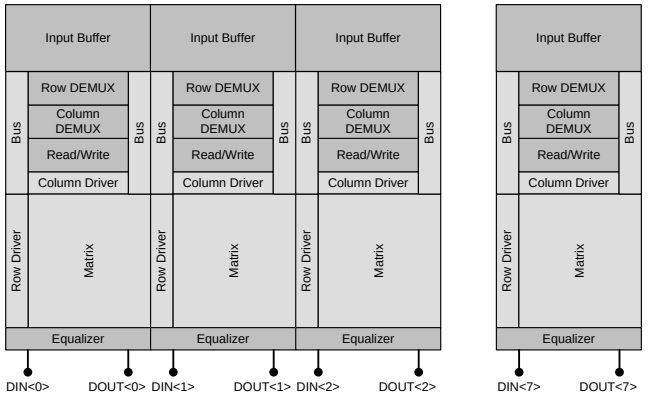
MORAL Microcontroller – Technology and PDK

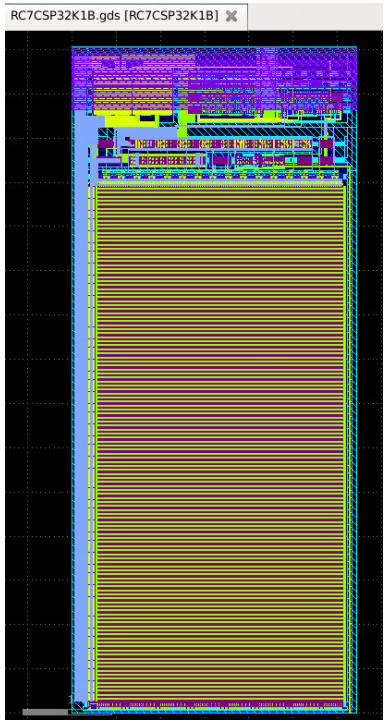
IHP SG13S/RH - PDK for Space Applications

	SG13S/RH
Process Description	**SiGe HBTs npn Peak f_T /f_{MAX} 220/340GHz 130nm Dual Gate –Oxide CMOS (V_{DD}=+1.2V, +3.3V ; T_{OX} = 2nm / 7nm)**
Commercial Qualification – Based on JEDEC Standard JP001.01 – EPPL/QML/QPL (ESCC QPL, ESCC QML, MIL QPL, JAXA QPL)	**completed 2014** Evaluation ongoing
PDK Availability ■ **Access Status**	**In development -Early Access NDA/EXPORT License**
CMOS Std Cell Core and IO Libraries	**IHP IXC013RH (~ 90 cells)**
Radiation Assessment (Digital) ■ **TID** ■ **CMOS Libraries**	**100krad(Si) – 300krad(Si) SEU/SEL completed SEL Threshold > 65MeV/cm²/mg (RHBD IHP cells) SEU Threshold > 30MeV/cm²/mg (IHP RTMR FF)**
Evaluation Testing ■ **in acc. ESCC No. 2269010**	**Activity started**
Operation Temperature (max rated T_J)	**-55°C to +125°C (TBC)**
Test Vehicles ■ in acc. ESCC No. 2269010	**TCV, DEC –I DEC-II(CMOS, Bipolar) RIC in progress**
Radiation Tests ■ TCV (Devices, analog) ■ DECs (Digital, Analog BiCMOS) ■ RIC (Mixed-Signal IC)	**completed** „ DEC-I (SEU/SEL), Early structures planned
Endurance Testing HT & RT ■ HBT npn-devices ■ HBT lifetime determination ■ CMOS devices ■ CMOS Core & IO Std Cell Library	**Activity started (qualification of technology for general purpose applications done)**

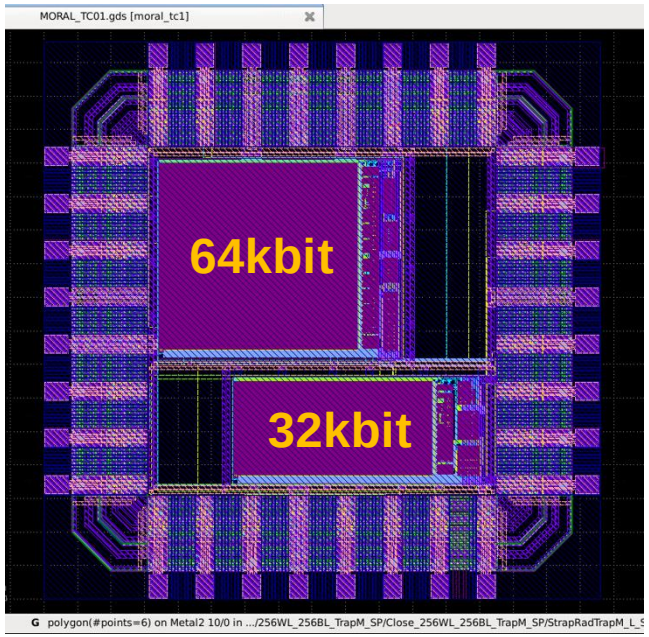
MORAL Microcontroller – Memory and Analog IPs

- Rad-hard SRAMs
  - Independent decoding schemes
  - 6T SRAM cell
    - Island Guard Ring (IGR) instead of Enhanced Guard Ring (EGR)
    - Tradeoff between inter-device leakage degradation and area





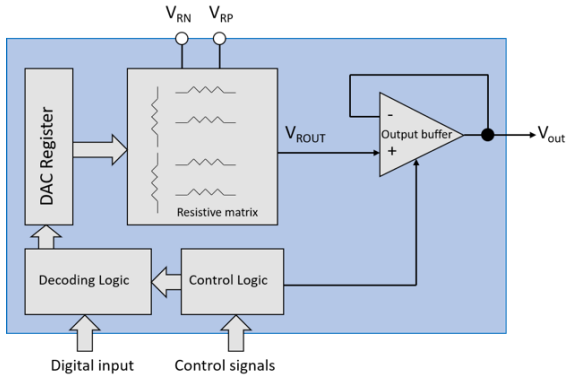
Single bit macro

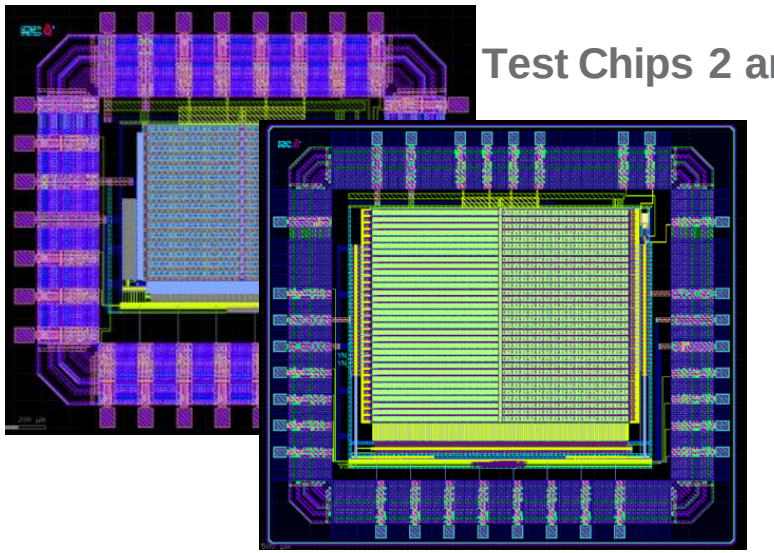


Test Chip 1

MORAL Microcontroller – Memory and Analog IPs

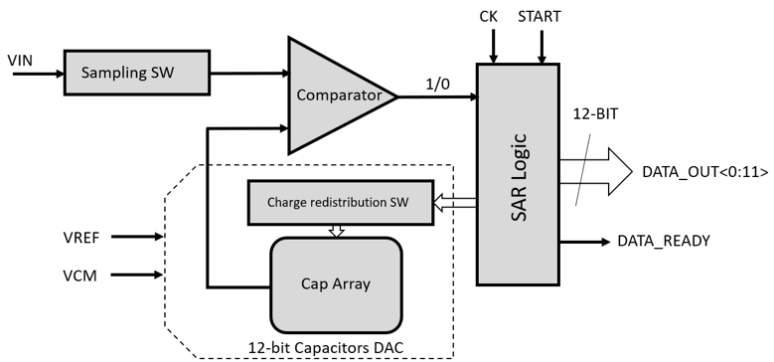
- Rad-hard 12-bit DAC
  - Architecture based on resistor divider (Kelvin divider)

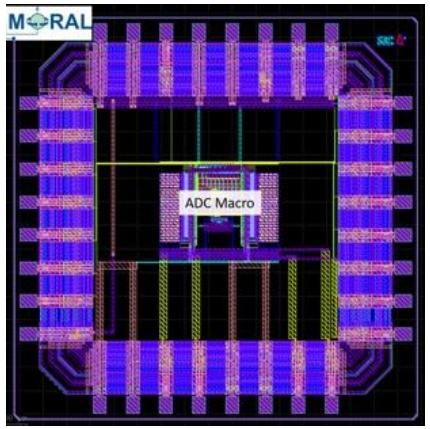




Test Chips 2 and 4

- Rad-hard 12-bit ADC
  - Architecture - SAR (Successive Approximation Register)
  - Single-ended and differential



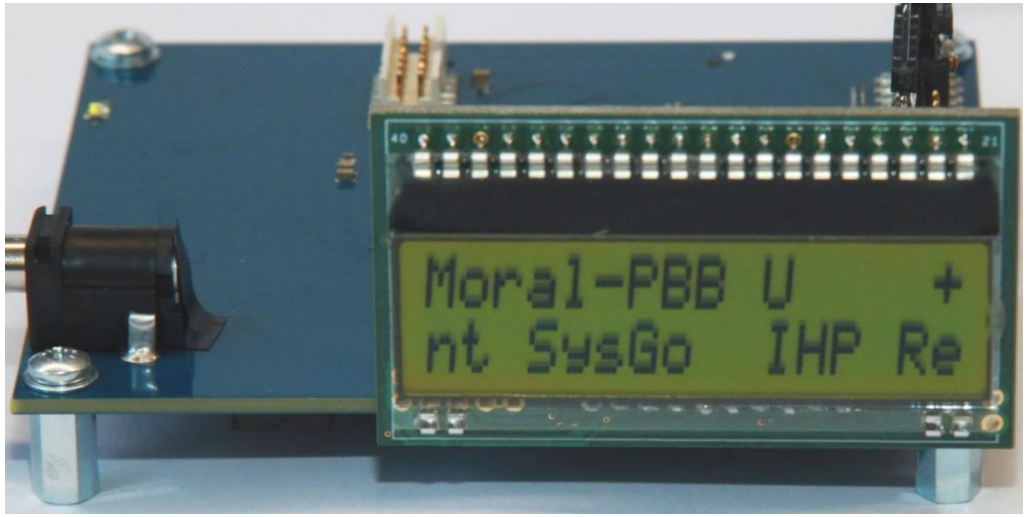


Test Chips 3

MORAL Microcontroller – FPGA Board

- Implementation on programmable hardware platform
  - Early hardware debug
  - Early tests of complex software
    - Ex.: Operating system, compiler and assembler tool-chain, and simple applications

- Project dissemination
  - Opportunity for the academia to know and experiment with the new architecture

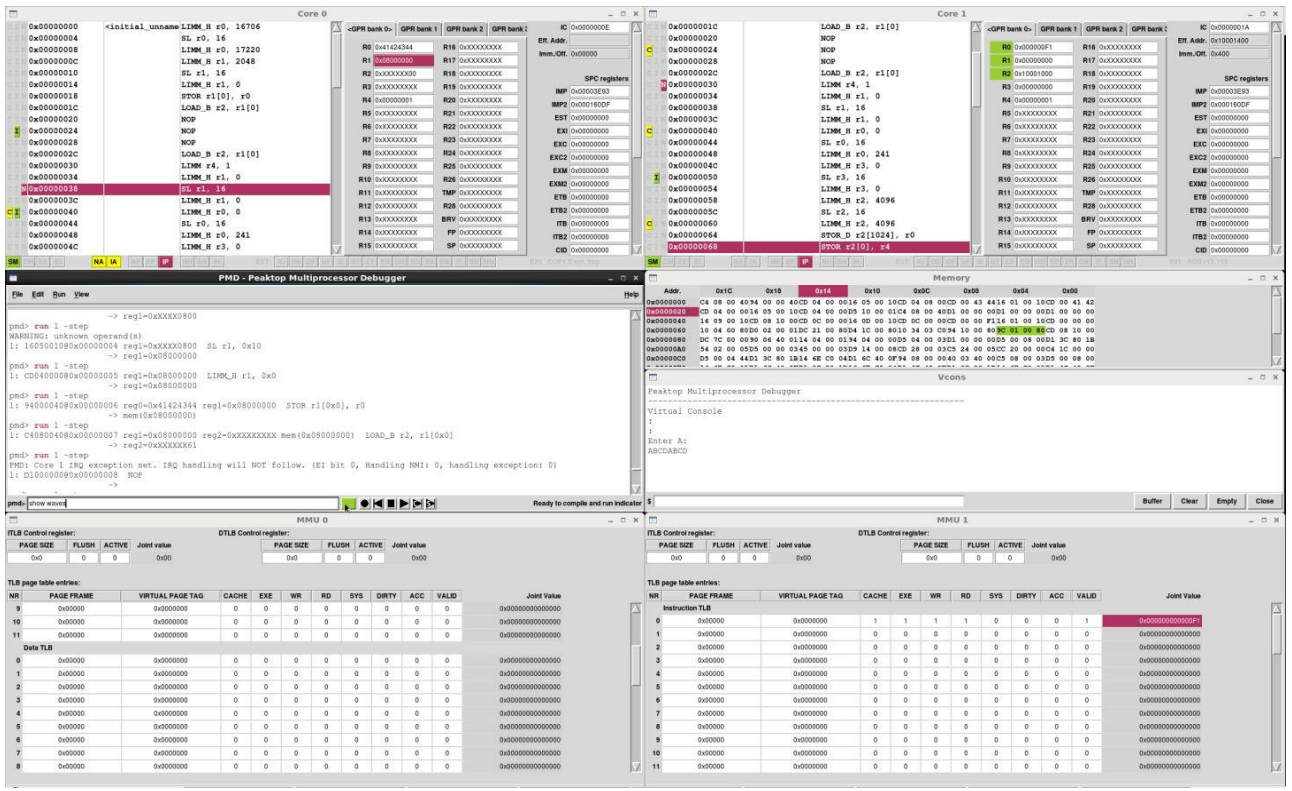


FPGA board

For availability of an evaluation board use the contact form in MORAL's website.
www.moral-project.com

MORAL Software – PEAKTOP Toolchain

- Open source toolchain
  - Multiprocessor Debugger
  - Instruction Set Simulator
  - Complete ISA and tools documentation



https://www.moral-project.eu/acad_open_source.html

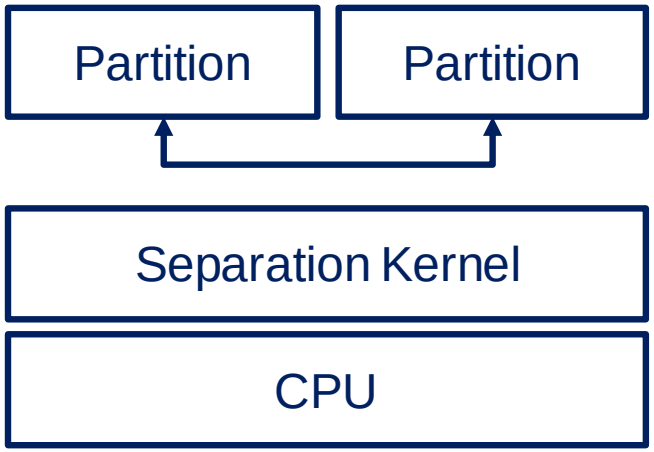
MORAL Software – Compiler and RTSK

CompCert – 2021 ACM Software System Award

- Compiler for C programming language
- The only **formally verified** compiler in the market
  - Free for evaluation, research, and education
  - Commercial licenses distributed by AbsInt
- Porting of CompCert for the PEAKTOP architecture
  - Implementation of binary utilities
  - Optimization and formal verification
  - Semi-automatic testing with FPGA board

MORAL Software – Compiler and RTSK

- Real Time Separation Kernel - RTSK
  - Provides isolated partitions
  - Communication between partitions
  - Partition is an execution environment that
    - Serves as a virtual CPU
    - Contains a guest operating system



- RTSK tailored for the PEAKTOP microcontroller
  - Microcontroller for space platforms provide limited RAM for any COTS
  - Must have a very low footprint

- Separation kernel prototype
  - First release for project partners
  - Running on the FPGA board

Development Status

MORAL Project	Status	Period	Comments
Prototype specification	done	Q2 2020	Completed
Prototype design	done	Q1 2021	FPU, DSP support, and M1553
Prototype functional tests	done	Q1 2021	Integration and functional simulations
Prototype emulation	done	Q2 2021	Running on the FPGA board
Memory and analog IPs design	done	Q4 2021	SRAM, DAC, and ADC
Test chips fabrication	done	Q4 2021	Four test chips
RTSK	done	Q4 2021	Running on the FPGA board
Compiler - CompCert	done	Q1 2022	Porting and verification completed
SRAM, DAC, and ADC test chips evaluation	done	Q2 2022	12-bit DAC and 12-bit ADC
Drivers, library, and software tools		Q1 2023	Specification on-going
Prototype fabrication and testing		Q2 2022	Layout on-going
Prototype stress tests		Q1 2023	Radiation test PCB on-going
Prototype demonstrator		Q1 2023	Demonstrator PCD on-going

MORAL Website

- Access for more information and news about MORAL
- Links for the project Social Media
- PEAKTOP toolchain download

www.moral-project.eu

Thank you for your attention!

Felipe Kuentzer

MORAL

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