Rad-hard Microcontroller with Open Access ISA for Space Applications

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***Abstract*— The MORAL project consist in the development a completely European, ITAR (International Traffic in Arms Regulations) free microcontroller for space applications, focused on small satellites, flight control and payload computers for the purposes of mission control, earth observation, navigation and many other applications. The processor core of the microcontroller is based on a novel IHP PEAKTOP architecture, including novel instruction set architectures (ISA). The microcontroller would provide mechanisms for increased reliability and adaptability according to the needs of the space applications. Besides the microcontroller, the required ITAR-free middleware, RTOS (Real Time Operating System) and toolchain would be also available. The end goal is the exploitation of final project results targeting a trans-continental market. In this work an overview of the MORAL project is presented, including the microcontroller specification summary, radiation-hardening methodology, and the project developments.**

I. Introduction

The application field of small satellites develops rapidly over the last years. It is expected that the number of satellites until 2029 will exceed 57000. This opens new perspectives and application possibilities, including replacement of old satellites and more complex processing needs for tasks such as satellite constellation and swarm formation.

For various applications within the satellites the microcontrollers are needed. This includes control domain, with propulsion systems, various robotics applications, motor & mechanisms, DC/DC conversion, or thermal regulation. Another application domain is represented also by scientific instrumentation for control of various sensing devices. Microcontrollers market is already having a number of very good and mature solutions, including products from Cobham Geisler, Atmel, and several US suppliers (Vorago, Texas Instruments).

One trend in general hardware development is the open hardware approach which rapidly started to develop in the last years. One of the major concepts is the use of open access Iinstruction Set Aarchitecture (ISA), where the main example is the rapid growth of RISC-V approaches. This trend requires also changes in the space domain.

This development is part of the EU project MORAL, targeting development of microcontroller IC with a 130nm standard CMOS technology, and corresponding development software. MORAL approach exactly addresses this need with the target to develop a completely European, ITAR-free microcontroller for space applications. MORAL approach is based on the novel PEAKTOP architecture (incl. novel open access ISA [1]), and includes formally-verified C-compiler, Real-Time Operating System (RTOS) and toolchain, and corresponding demonstrator board.

II. MORAL Project

A. MORAL Microcontroller

The microcontroller contains, in addition to the regular execution pipeline, also floating-point unit, memory protection unit, as well as Digital Signal Processing (DSP) support. The integrated SRAM, based on rad-hard Enclosed Layout Transistors (ELT) and extended with Error Correction Code (ECC) for Single-Event Upset (SEU) correction, should support initially 256 KB, with the perspective of further memory space increase. The microcontroller includes a number of interfaces relevant for space applications, including CAN, UART, SPI, SpaceWire, I2C, MIL-STD-1553, etc. The summary of the microcontroller characteristics and the complete list of peripherals is presented in Table 1. It is important to emphasize also the integration of rad-hard analog to digital and digital to analog converters with 12-bit resolution. The former is a successive approximation registers (SAR) based Analog to Digital Converter (ADC), while the latter is a resistor-string Digital to Analog Converter (DAC). The block diagram of MORAL's microcontroller design is show in Fig. 1.

TABLE I. Microcontroller specification summary

	Description
PEAKTOP Core	– 32-bit CPU with floating point unit (FPU) compliant to IEEE 754-2008 standard – DSP support – 2-level Memory Protection Unit (MPU)
Memory	– 256 KB 32-bit on-chip SRAM extended with error detection and correction (EDAC).
Communication interfaces	– 2x SpaceWire: include RMAP (remote memory access protocol) function – 4x UART interfaces – 2x SPI interfaces

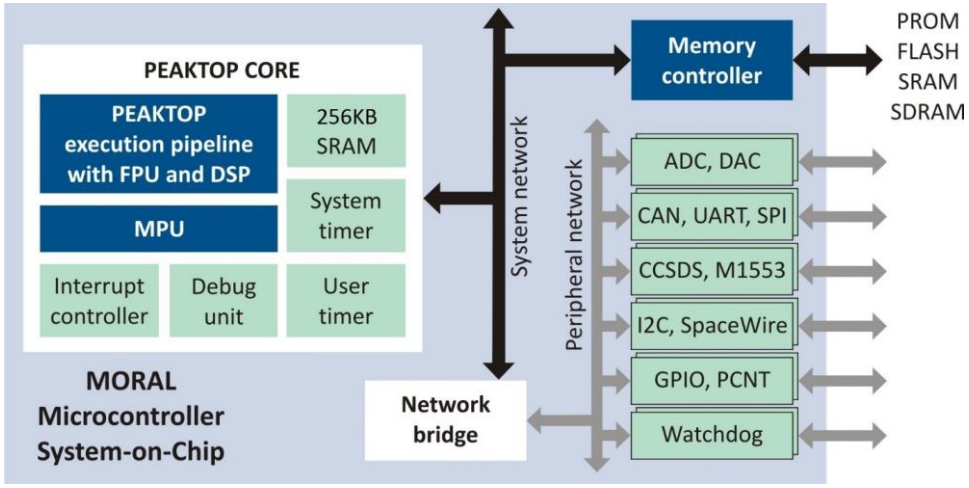

Fig. 1. MORAL Microcontroller block diagram

	Description
	– 2x I2C interfaces: 8-bit oriented up to 1Mbit/s bidirectional and up to 5Mbit/s unidirectional – 2x CAN 2.0B interfaces: up to 1 Mbit/s – 1 x MIL-STD 1553C bus interface: raw data rate of 1 Mbit/s
Analog components	– 2x 12-bit DAC converters – 1x 12-bit ADC converter: 8 single-ended or 4 differential channels
Other components	– 32-bit timers connected to AHB system bus: 2 system timers and 4 user timers – 1x interrupt controller (32 interrupt lines) – 4x pulse counters – 1x watchdog timer – 1x PWM generator: independent 8-channel or complementary in up to four 2-channel pairs – 64x GPIO ports (shared with internal peripherals I/Os)
Technology	IHP SG13RH (S) process
Packaging	208 pin ceramic
Rad-Hard	– TID 100 krad (Si) – SEU for the processor's digital core >30 MeV cm2/mg (Si) – SEL >60 MeV cm2/mg (Si)

B. Radiation Hardening Methodology

The key aspect of MORAL development is the radiation hardening methodology which is consequently implemented at different abstraction layers. Concerning the analog IPs, the hardening has been achieved acting on architecture, circuit and layout sides. For the Digital to Analog Converter (DAC), the choice of a topology based on poly-resistors (insensitive to radiation) is coupled with proper MOS sizing. Extendeduse of ELT shapes and guard-rings are common to both. For the Analog to Digital Converter (ADC), metal-insulator-metal (MIM) capacitances (insensitive to radiation) and over-design have been adopted. Moreover, digital control section serving analog functions is implemented with proven rad-hard digital library.

At the level of complex digital sequential cells, the Triple Modular Redundancy (TMR) methodology has been applied for filtering SEUs while timing filters address Single Event Transients (SETs). SETs in control logic are addressed by specific combinational cells, pre-tested for SET sensitivity. SET mitigation is achieved either at circuit level by reducing the number of p-channel and n-channel transistors not directly connected to power supply and ground, and layout level by making leverage on enhanced guard rings also used for Single Event Latch-up (SEL) mitigation. Extensive use of ELT geometry guarantees Total Ionizing Dose (TID) resiliency well over 100 Krad (Si) making the final SoC suitable for the major part of Low Earth Orbit (LEO) and Geostationary Earth Orbit (GEO) missions. At system level, the error accumulation is addressed by use of error correcting codes and scrubbing in memory.

C. Project Development

The project started in 2020, and until now significant developments have been performed. The complete Register Transfer Level (RTL) processor core has been developed and verified in extensive simulations. The complete RTL platform is also mapped to an Field-Programmable Gate Array (FPGA), which is used for co-verification. As for the analog Intellectual Property (IP), the DAC have been successfully characterized in lab operation environment. The final integration and back-end design is ongoing. The target process is SG13RH technology from IHP, that is currently under European Space Agency (ESA) evaluation. The technology has been commercially qualified and used in many products, and radiation hardness features have been verified within successfully finished DLR project. Based on such background the aim is for for 100 Krad (Si) TID hardness, as well as to be SEL-free up to at least 60 MeV·cm2/mg (Si) and with SEU sensitivity > 30 MeV·cm2/mg (Si).

At the software side, CompCert, a formally verified C compiler, was successfully ported to the PEAKTOP architecture. Through its formal verification, CompCert is free of miscompilation and allows the use of code optimizations, even for safety- and mission-critical applications. This ensures the effective use of limited hardware resources. Furthermore,

formal verification of software is a major advantage over typical proven-in-use arguments, which are not applicable if the target audience is not a mass-market.

Serving as an operating system, a new separation kernel has been developed to run on the PEAKTOP CPU. The challenging frame conditions, and strong security and safety standards, are combined with an extremely small footprint, to match the embedded memory limitations.

After successful production the produced integrated circuit (IC) will be functionally verified, but also initial reliability tests will be performed. In parallel the work on the demonstration board, which will include also application demonstration, is under development.

III. CONCLUSION

The PEAKTOP microcontroller platform introduces novel ISA concept and aims to result in competitive mixed-signal solution for space applications. The advanced development stage of digital & analog IPs, as well as system software, provide us with great confidence for successful exploitation of final project results. Acknowledgment

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