First Silicon Enabling Rad-Hard Non-Volatile Memory in 22nm Technology for Space Applications

P. Zuber, A. Bucci, L. Berti, G. Pollissard, E. Timokhin, G. Franciscatto, S. Dupont,
G. Glorieux, K. Bertrand, A. Dhiman, E. da Costa Losqui, K. Vanhoutte, G. Thys, M. Kakoulin
Imec.IC-link, Leuven, Belgium

C. Marquet, C. Sellier, P. Wang
3D PLUS, Buc, France

zuberp@imec.be, thys@imec.be, kakoul74@imec.be

Abstract

In this article, we report the design hardened against radiation effects (DARE22G) of new analog and digital IP in 22nm FDSOI. The main purpose of the design is to enable a magnetic non-volatile random-access memory (MRAM) for space use. A test vehicle has been taped out, and first functional tests pass.

I. Objectives

Space electronic applications require ever increasing non-volatile storage densities while being immune to radiation and temperature changes for at least 15 years of mission time.

Due to the beneficial intrinsic single event effect immunity of fully depleted SOI, its mainstream availability in a modern-day, commercial–and therefore low-cost compared to custom–22nm process, and zero bit-failures of previous MRAM generations under radiation, these technologies were a natural choice for the project [2,3].

The objectives are to verify if modern commercial STT-MRAM cell SEU- and commercial FDSOI process SEL-immunity levels are sufficient to serve space applications for low, medium, and geostationary orbits for civil and scientific applications. Furthermore, we systematically analyze the process' basic TID tolerance. A deeper analysis of TID in the same technology, including mitigation by back-biasing is conducted in [1].

Table 1: *MNEMOSYNE test vehicle targets*

Process	*22nm Planar Fully Depleted SOI*
Metal stack	*9 metal layers*
Supply voltage	*0.8V core / 1.8V & 3.3V IO*
SET / SEU immunity	*60*MeV.cm^2/mg
SEL threshold	*70*MeV.cm^2/mg
TID mitigation level	*< 100krad*
Mission life	*15 years*
HTOL	*2000 hours*
Temperature profile	*-40°C .. 125°C (default)*
Assembly	*wire bond*

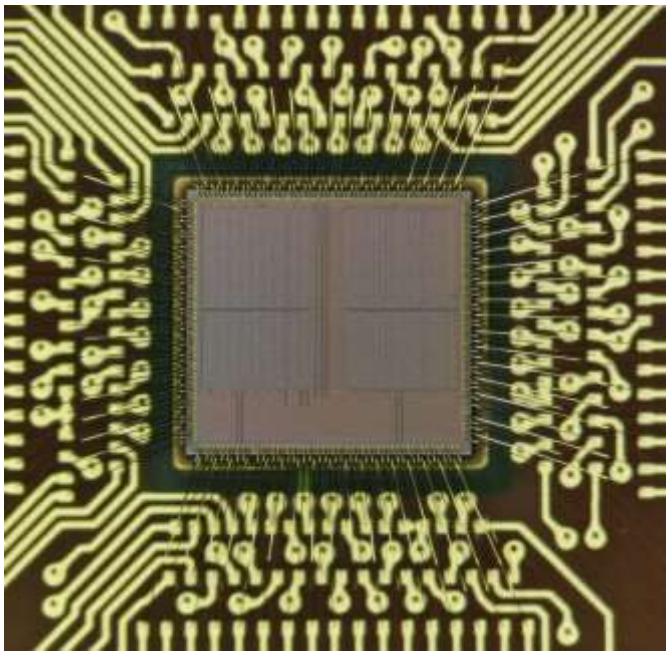

Figure 1: *Test Vehicle bonded to substrate.*

To support the evaluation of new, radiation hardened by design (DARE) analog, mixed signal and digital IP blocks, a digital-on-top test vehicle is required. Since the IP is new, testing, characterization, and radiation-stressing of the chips is a fourth objective. Table 1 shows general IP and test vehicle requirements.

Another aim is to establish a complete radiation hardened platform with all IP required to support any future space application. For the test vehicle, we still resort to some standard cells by the foundry. In a future version of the chip, we will move to 100% DARE foundation IP.

The remainder of this article is structured as follows. In section II we describe the power management unit which integrates all IP required to sequence the start-up, power the MRAM and the core, provide a system clock, and monitor the supply conditions. In Section III we describe the foundation IP, which also includes a new rad-hard 3.3V IO library. The next Sections elaborate on the test vehicle itself, and its test considerations. The last Section provides a status summary and an outlook.

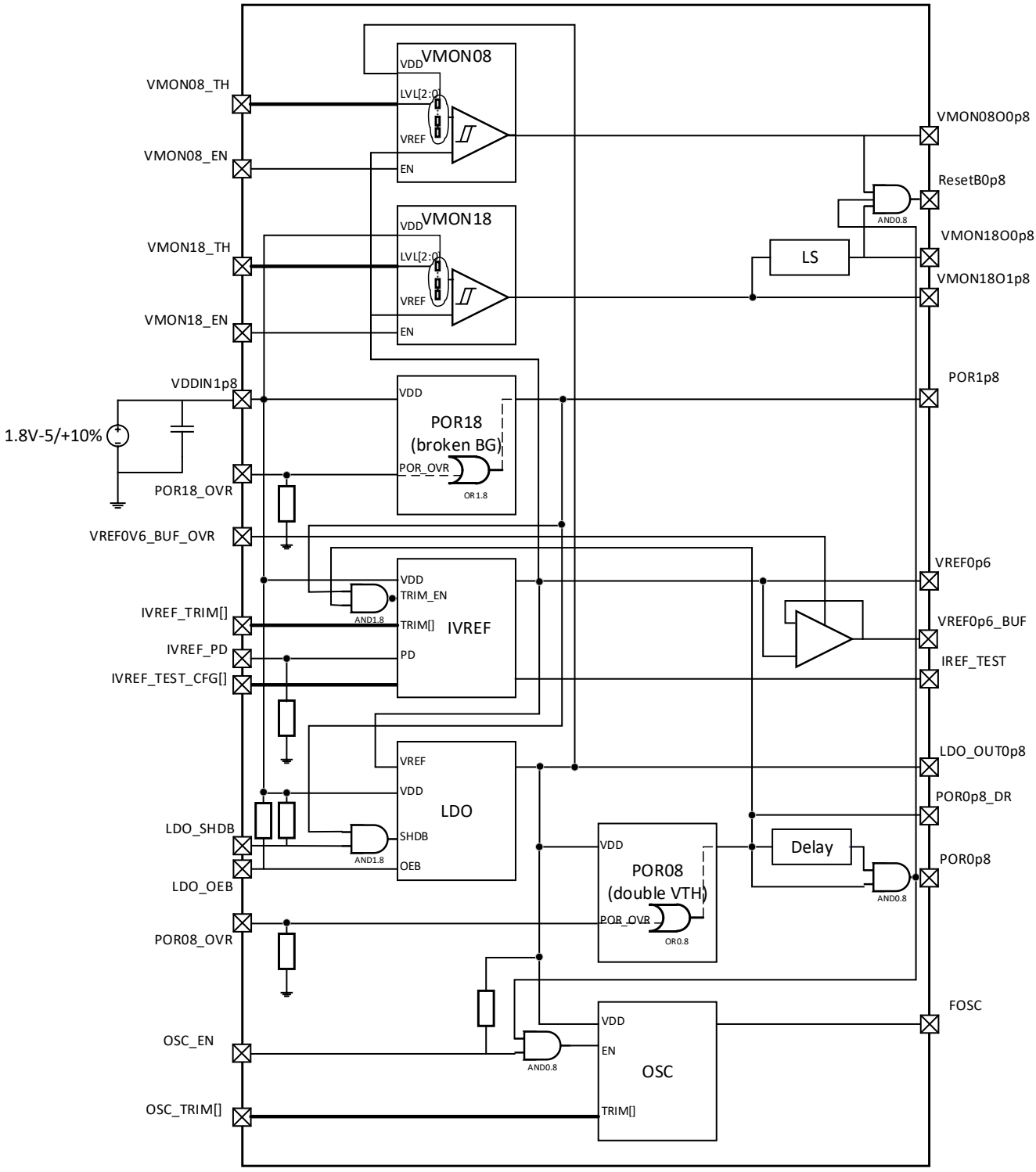

Figure 2: *High level view of PMU*

II. PMU

The power management unit (PMU), cf. Figure 2, is a monolithic integration of most analog IP required to serve the following purposes:

- Provide regulated system core voltage of 0.8V
- Provide 0.6V buffered reference voltage required by the MRAM macro
- Provide system clock of 100MHz
- Provide safe start-up sequence, including core reset release
- Provide precision voltage monitors at runtime

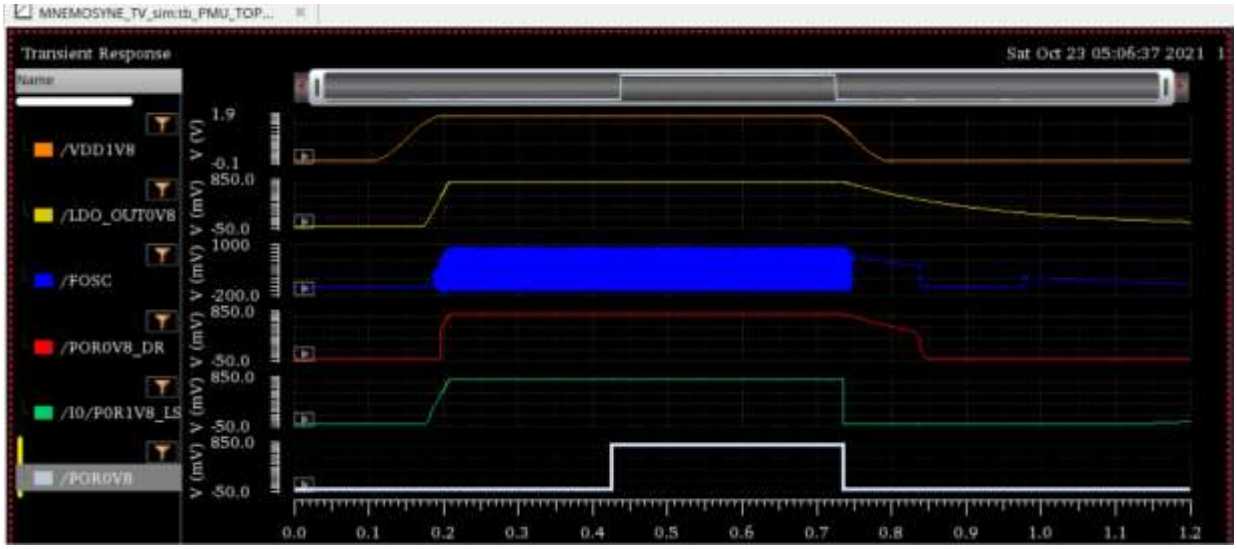

Figure 3: *Essential PMU power-up and power-down. The digital delay using the oscillator ensures that the reset is released only after a safety interval of few 100usec.*

- Provide power cut-off functionality to the non-volatile arrays if in stand-by.

Central to the PMU is a current/voltage reference generator (IVref). It is required not only for the low dropout (LDO) voltage regulation from 1.8V to 0.8V chip supply, but also for the system clock oscillator of 100MHz, the buffered voltage reference of 0.6V required by the MRAM and programmable voltage monitors for the 0.8V and 1.8V supplies. Next to these blocks, there are also two reset controllers, a reset delay, test and debug support circuits and some required glue logic.

The IVref is trimmable to better than <4% accuracy over corners. Safe start-up with default trim from 1.8V is ensured by a modified bandgap-based power on reset (POR) controller that also turns on the LDO for creating the core supply of 0.8V. This voltage triggers the second POR for 0.8V, enabling the trimmable RC oscillator – also using safe standard trim values – and the delay line clocked by the oscillator, ultimately releasing the reset from the digital core after a confidence period of at least 160µs.

Note that in this phase of system start-up, the LDO and OSC are in relaxed tolerance mode with lower accuracy and maximum current, sufficient to safely read out from the fuse box and apply the trim values.

After trim of IVref and oscillator, the two voltage monitors can be enabled and tuned with 4 bit granularity each. They are intended to be used by the control part of the core, typically through firmware, to record any supply out of tolerated range.

The system is now ready. This test vehicle is primarily designed for accessing the on-chip IP through digital commands received via one of the 1.8V and 3.3V SPI interfaces, at a maximum clock rate of 133 MHz. Several modes exist for direct IP access at the pins and access through an on-chip controller.

The voltage regulator stability has been verified by simulation against specific custom package parasitics and third-party supplied current profiles of the MRAM blocks. This also applies to the reference voltage buffer.

To avoid unintentional write or erase of the non-volatile or one-time programmable memories, a power switch for the array voltages has been designed. It respects the maximum possible current encountered during read/write/erase and automatically disconnects the array voltage when the core supply is not present. This IP is very useful as it saves off-chip components. For layout purposes, it is designed as separate macro, not integrated into the PMU.

All IP is verified across consumer PVT corners crossed with total ionizing dose corners (0.8V/1.8V/3.3V +-10%, -40°C to 125°C, 0 to 100krad) and withstands, except for the LDO, more than 15 years of continued operation at more than 115°C from an electromigration point of view. The LDO is safe for 15 years at 105°C equivalent T at its continuous max rating (100mA), which exceeds by far the targeted mission profile of 65°C equivalent T or mission time of 15 years by far.

Total ionizing dose tolerance is verified and characterized by an in-house transistor model wrapper, filled with measurement data gained from a previous test chip in this technology. Transistor-type specific parameter sets, for 0 and 100krad, were applied. Furthermore, all analog and digital IP blocks are systematically scanned for SET and SEU sensitive nodes using our custom fault-injection tool and re-designed if needed.

For improving the SEE behavior, we designed SET filters, use DICE flops, triple majority voters, specially designed antenna diodes and applied other methods. Specific properties of the FDSOI technology were also exploited, for example the switches for power-down modes are using isolated gates of series devices.

III. Foundation IP

Within the scope of this project, we also developed a new radiation hardened 3.3V general purpose IO library, and used the radiation hardened 1.8V general purpose IO library from the EFESOS project [1], a sister project where a range of other IP, such as a 10-track library, are developed. As core library for this chip, we resorted to the approach of a previous project, where a radiation hardened 8-track standard cell li-

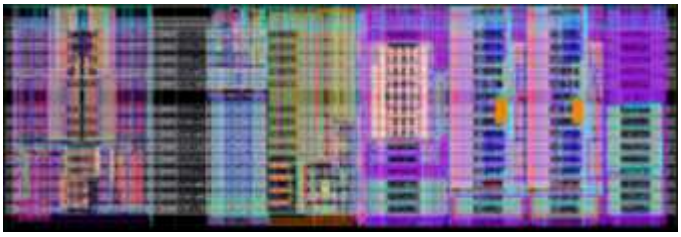

Figure 4: *IO33 layout test segment with bias generator (left) and GPIO (middle) and range of supply and other auxiliary cells. In the filler and breaker cells at the borders, one can see well the grey horizontal ring signals.*

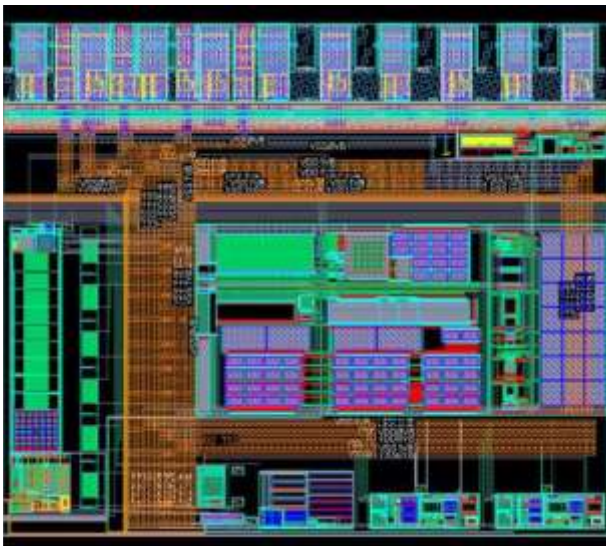

Figure 5: *PMU layout with clearly visible LDO bond pads along the north edge, oscillator to the west, IVref in the east PORs, VMONs and glue logic in the south.*

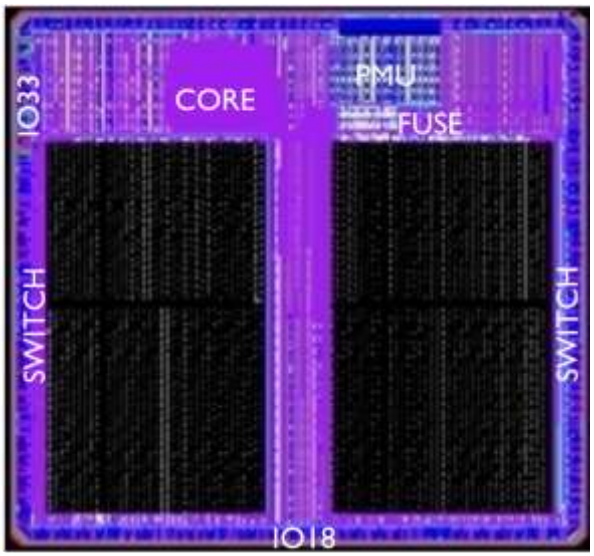

Figure 6: *Test vehicle layout*

brary extension to the existing foundry library was developed. This will be changed to the before-mentioned 10-track library in the future.

The new radiation hardened 3.3V IO library in a 0.8V/1.8V process was not a straightforward design task. Transistor stacking and back-biasing were required to achieve the tight constraints on speed (133MHz) while staying in safe operating regions with 1.8V transistors. Important features like slew control and Schmitt trigger are implemented as well.

Auxiliary cells were also designed. These include power supplies for IO (3.3V) and core (0.8V), IO adapter cells between 1.8V and 3.3V domains, filler cells, breakers and a power detection cell that sends a shutoff signal to the GPIO in case either power is not present. The latter also provides the required three bias voltages for the level shifters, which run along the IO-ring together with other ring signals, cf. Figure 4.

The 8-track standard cell library provides the essential radiation hardening elements required. These include DICE flops, latches and clock gates, filters, triple majority voters, SET filters and hardened clock buffers. For normal random logic, compatible commercial cells were used in this project. This solution is a placeholder and will be replaced soon by an all-new 10-track library with much richer cell set also comprising hardened cells for random logic, and which will be available in twelve gate-length / Vt flavor combinations. At the time of writing (May 2022), the library cells are under manufacturing in another test chip [1].

Layout of all IP is also radiation aware. Previous test chips showed a typical impact diameter of heavy ions. Sensitive node pairs were placed apart by at least this value to avoid hard-to-analyze muti-node spikes.

IV. Test vehicle implementation

The digital-on-top RTL2GDS2 flow included standard stage reviews after each phase (requirements, architecture design, schematic, layout). Some work was required to be done in parallel to the IP, and industry standard abstracts (lef, lib, simulation models) were developed for this purpose.

A state-of-the art industrial digital implementation system was used. As such tools are optimized for the mainstream targets power, performance, and area, radiation hardening was added by scripting. Typically, this includes the introduction and protection from being optimized away of redundancy, and the use of restricted cell sets for SEU critical parts. Clock and reset trees were allowed to map to only very restricted cells with highest SET immunity. Full-custom glitch filters were inserted at important nodes as well.

For sign-off we adopted foundry-provided early/late derates for normal device aging and added extra margins for TID derived from cell characterization runs using a modified compact model. N-well and P-well back gates of the logic core devices are accessible and can be freely biased for experimentation purposes.

V. Test Aspects

All IP is optimized for test, debug, and characterization. Essential functions can be bypassed so that dependent errors are avoided. IVref for example is supplying the voltage buffer, oscillator, LDO and voltage monitors. A potential loss of reference is backed up by a reference bypass pin. Similar bypasses exist for SPI, array power switch, power-on reset, system clock and others.

The top-level supports DfT scan, and dedicated test modes for characterization of the 3.3V IO library and all IP macros

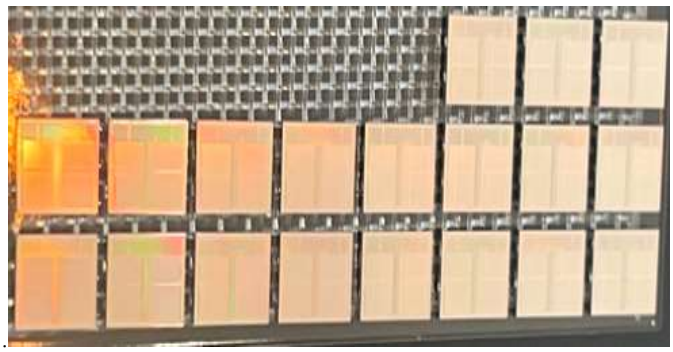

Figure 7: *First set of test vehicle dies before assembly*

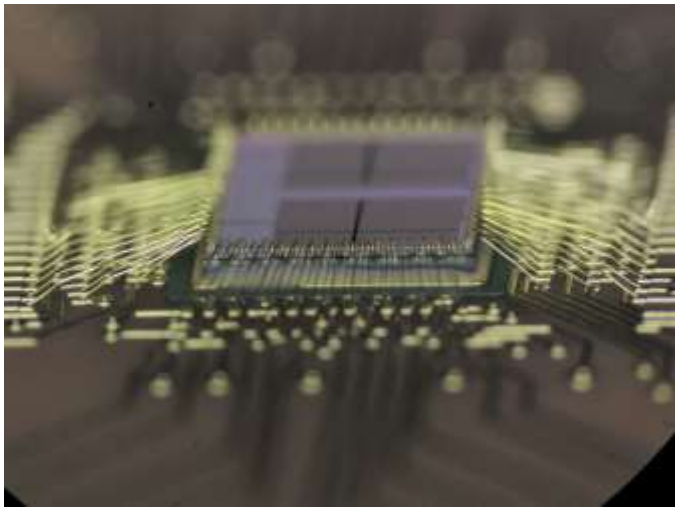

Figure 8: *Bonding of test vehicle.*

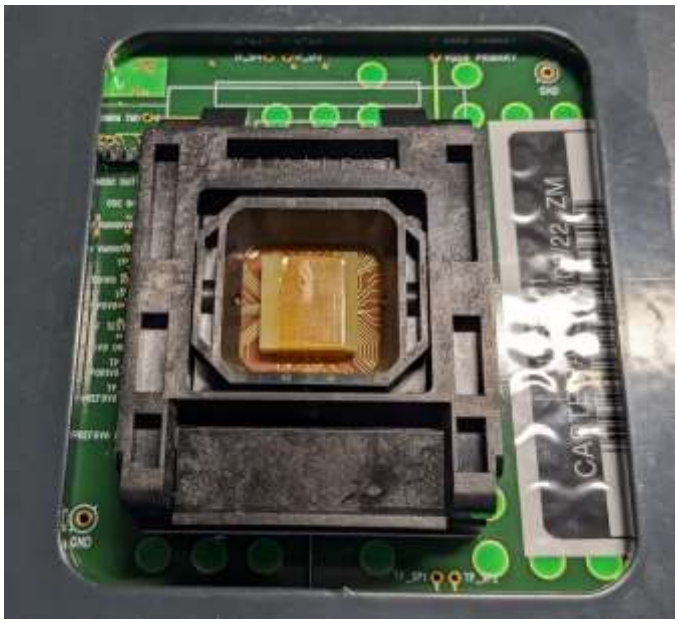

Figure 9: *Test board with socket*

used. Due to the many test ports, the chip is slightly IO limited.

An IP test plan has been worked out with several hundred tests for the four domains of production screening, bring-up and characterization, SEE tests and characterization after TID.

VI. Status and Future Work

The test vehicle dies have been manufactured, assembled, and have undergone first functional tests, which are positive (Figure 7 to Figure 9). Trimming and screening is carried out in parallel to radiation test preparations for SEE, using laser and heavy ions, and TID testing. The test vehicle will also undergo an HTOL test.

Once the campaign is finished, and the new DARE IP is characterized, a scaled-up version of the test vehicle, optionally with improved hardening of the components, will be developed.

The DARE22G platform is also constantly expanded. Apart from the OSC, IVref, LDO, POR, VMON, SWITCH, PMU and 3.3V library developed in this project, a sister project [1][6] is contributing with a new 10-track library, 1.8V IO library, LVDS, SSTL, back-bias generator and TID sensor. There will also be new ADC, DAC, SERDES and PLL macro blocks [7].

VII. Acknowledgements

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The consortium is consisting of Beyond Gravity (former RUAG), NanoExplore, University of Padova, TRAD, 3D PLUS and imec.

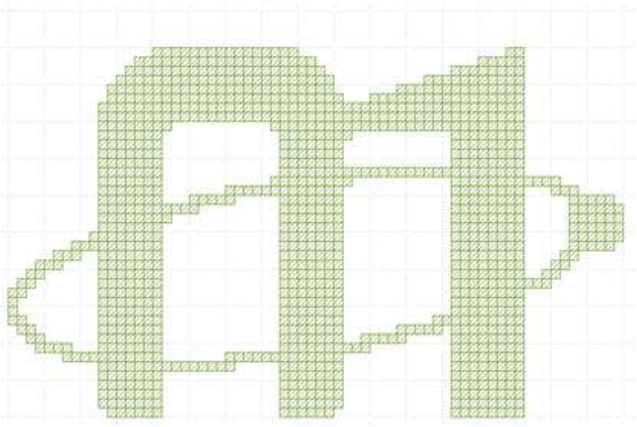

Figure 10: *Project logo, rasterized for use as assembly marker in top level metal layer.*

VIII. References

[1] E.H. Boufouss et al., AMICSA 22 [2] M.C. Casey et al., MAPLD 18 [3] R.R. Katti et al., REDW 18 [4] https://cordis.europa.eu/project/id/870415 [5] https://mnemosyne.dei.unipd.it [6] https://cordis.europa.eu/project/id/821883 [7] E. Pun-García et al., AMICSA 22