Detailed SET Ionized Charge and Pulse Duration Measurement of a 65 nm CMOS Technology

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This paper presents the measurement results of Single-Event Transients (SET) in a commercial 65nm CMOS technology. The heavy-ion test campaign measured both total SET ionized charge and SET pulse duration. In this test chip, single transistors of different types and dimensions were implemented as victim devices. SET variation due to different supply voltages also was investigated. The detailed measurement principle and circuits are described in [1].

The test chips were irradiated with heavy ions at the Heavy Ion Facility (HIF) in UCLouvain, Belgium. Nickel and Xenon are used in this test with different incidence angles (0° and 45°) to obtain a different effective LET. Two chips were tested at room temperature and exhibited consistent results. During the test, over 20000 SET events were observed on each chip.

SET ionized charge measurement

The SET charge collection of 65 nm technology follows the prediction. For example, the PMOS devices exhibit a smaller collected charge than the NMOS devices. DNW devices collect more than 30% less charge than non-DNW devices. The longer channel length of the devices results in a more charge collection and a higher sensitive area. However, some of the results are not as expected. Conventionally, the drain area is considered the SET-sensitive region of the transistor. From the measurement results, the unit device cross-section is larger than the expected unit device drain area. Specifically, the gate and even source area need to be taken into account.

SET pulse duration measurement

When the LET is high enough to produce a pulse to trigger the measurement circuit, the measurement results form a bell shape on the pulse duration vs. occurrences plot. A higher effective LET heavy ion can cause a higher most-frequent duration (mean value), a wider duration distribution range (variation), and the total number of occurrences. Besides, a longer channel can cause a more extended duration since the total transistor area is increased. When comparing the sensitive area of the non-DNW devices with the DNW devices, unexpected results are founded. DNW devices show a larger unit device cross section compared to non-DNW devices. It indicates that the DNW makes the victim devices more sensitive at high effective LET situations in pulse duration measurements. This phenomenon can be caused by the potential rise in the p-well followed by the injection of electrons into the p-well from the source.

More detailed information can be founded in [2].

References:

[1] Li, Z., Berti, L., Vignon, B., & Leroux, P. (2021, May). Single-Event Transient Ionized Charge and Pulse Duration Characterization in a Commercial 65nm CMOS Technology. *8th International Workshop on Analogue and Mixed-Signal Integrated Circuits for Space Applications (AMICSA)*

[2]Li, Z., Berti, L., Wouters, J., Wang, J., & Leroux, P. (2022). Characterization of the Total Charge and Time Duration for Single-Event Transients Voltage Pulses in a 65 nm CMOS Technology. *IEEE Transactions On Nuclear Science*, 2022.