Detailed SET Ionized Charge and Pulse Duration Measurement of a 65 nm CMOS Technology

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I. ABSTRACT

This paper presents the measurement results of Single-Event Transients (SET) in a commercial 65nm CMOS technology. The heavy-ion test campaign measured both total SET ionized charge and SET pulse duration. In this test chip, single transistors of different types and dimensions were implemented as victim devices. The detailed measurement principle and circuits are described in [1]. The test chips were irradiated with heavy ions at the Heavy Ion Facility (HIF) in UCLouvain, Belgium. Nickel and Xenon are used in this test with different incidence angles (0° and 45°) to obtain a different effective LET. Two chips were tested at room temperature and exhibited consistent results. During the test, over 20000 SET events were observed on each chip.

II. INTRODUCTION

The transistor parasitic capacitances become smaller and smaller because of the shrinking size in advanced CMOS technology. Therefore, the application will consume less power and achieve a higher operating frequency. However, the reduced parasitic capacitance makes the transistors more sensitive to SETs. To evaluate the SET performance of the design, one of the design procedures is performing the SET response simulation with a SET electrical current model [2]. This SET current model requires a sufficient charge and pulse duration expression to have a result that is close to reality. This paper presents SET heavy-ion test results of a 65 nm technology. It contains the on-chip SET total ionization charge measurement and the SET pulse duration measurement. These test results are also used to assist the DARE65 platform design from imec. IC-Link. It should be noted that all the results present in this paper had been published in [3].

III. SELECTED VICTIM DEVICES

The eight most often used MOSFETs are chosen as victim devices and are implemented into the chip. The size information is shown in Table I. Because different sizes and types of victim devices are chosen, a comparison of several SET results can be made according to Table I:

- SET results between NMOS and PMOS
- SET results between DNW devices and non-DNW devices
- SET results between L=60 nm and L=500 nm
- SET results between Core devices and IO devices*
- SET results between different power supplies*

Table 1 Victim devices size information

index	Victim Device	W	Finger	Length
VD1	CORE NMOS	10µm	10	60nm
VD2	CORE NMOS			500nm
VD3	CORE DNW NMOS			500nm
VD4	CORE PMOS			60nm
VD5	CORE PMOS			500nm
VD6	IO NMOS*			500nm
VD7	IO PMOS*			500nm
VD8	IO DNW NMOS*			500nm

*The SET measurement results of the IO devices and all devices in different suplies can be found in [3].

IV. SET IONIZED CHARGE MEASUREMENT RESULTS

The measurement results of minimum length (60 nm) core NMOS and PMOS are shown in Fig. 1. For ionized charge measurement, one occurrence responds to one readout which indicates the ionization charge is higher than Q_{th}. Q_{th} is set by the measurement and can be adjusted from 180 fC to 1.41 pC with a step of 40.5 fC/step for VD1 [1]. At a maximum effective LET of 88.39 MeV·cm2/mg, NMOS and PMOS victims show 277 and 279 occurrences at the minimum Q_{th}, respectively. The higher Q_{th} is set, the lower number of occurrences will get. The number of occurrences at the minimum Q_{th} is used to calculate the unit device cross-section (Occurrences $@Q_{th,min}$/*Fluence*/No.Devices). Then, the unit device cross-section of each NMOS and PMOS transistor is $4.85\times 10^{-7}cm^2$ and $4.88\times10^{-7}cm^2$. However, when the Q_{th} is higher, the occurrences of PMOS drop much faster than it does for NMOS. Finally, the maximum collected charge can be read when the occurrences are close to zero. In this case, the maximum charge of PMOS and NMOS transistors are 1.274 pC and 0.898 pC, respectively. In the lower effective LET case, not only the maximum collected charge but also the unit device cross-section of the PMOS devices are lower than for the NMOS devices. At the lowest effective LET, the ionized charge of PMOS always smaller than the minimum Q_{th}.

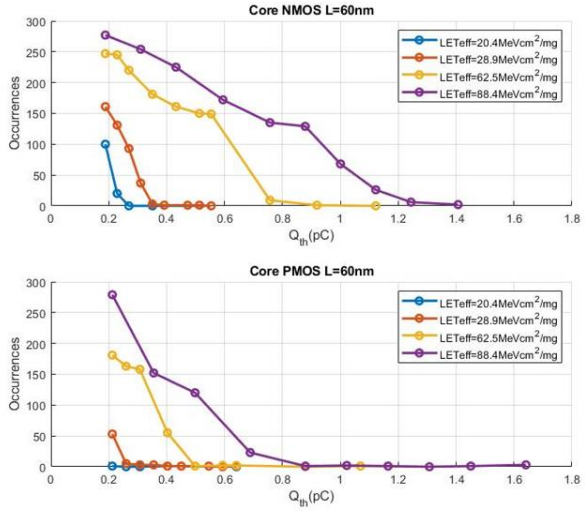

Figure 1 Measurement results of core NMOS and PMOS with a length of 60nm and 1.2V supply voltage.

Similar analyses are applied to all the core victim devices. The unit device maximum collected charge and cross-section of all victim devices at different effective LET are shown in Fig. 2 and Fig.3, respectively.

Fig.2 indicates that the maximum collected charge increases with effective LET, but does not show a convergent tendency. The PMOS devices exhibit a smaller collected charge compared to the NMOS devices, which is consistent with the off-chip charge measurement in [4]. Additionally, the longer channel length devices feature a larger amount of collected charge.

When effective LET is increasing, all unit device cross-sections of core devices increase and show a trend of convergence at high effective LET in Fig.3. In general, the unit device cross-section is larger than the expected unit device drain area. Specifically, the gate and even source area need to be taken into account. This is supported by the results of the devices with different gate lengths, but identical drain areas, where the longer length devices show a larger unit device cross-section in Fig. 3. Besides, when the heavy ions do not directly hit the transistors but other places like the substrate, the charge diffusion in the silicon substrate or the local p/n well also contribute to the charge collection. The amount of diffusion charge depends on the ionization radius of the heavy ions in silicon and the distance between the hit location and the drain node shown in fig. 4 [5]. It is further observed that the PMOS devices show a smaller or equal unit device cross-section than the NMOS devices at all effective LET. For DNW NMOS devices, the unit device cross-section is reduced when compared with the non-DNW NMOS devices. The reason is that the part of the charge generated in the pwell region is collected by the DNW before it can be collected by the NMOS drain. Further, the charge below the pwell/DNW junction cannot be collected by the NMOS drain because of the triple-well collection to the n-well tap.

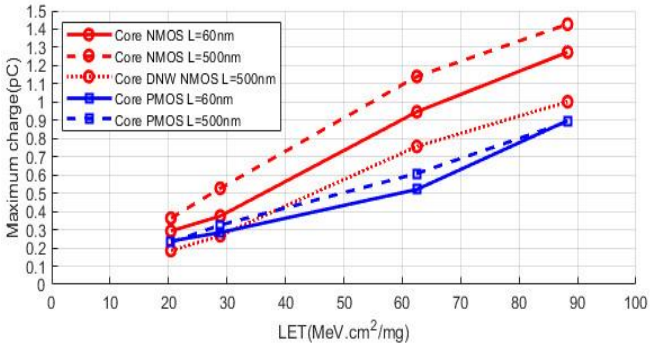

Figure 2 Maximum collected charge of core NMOS and PMOS with length of 60nm and 1.2V supply voltage.

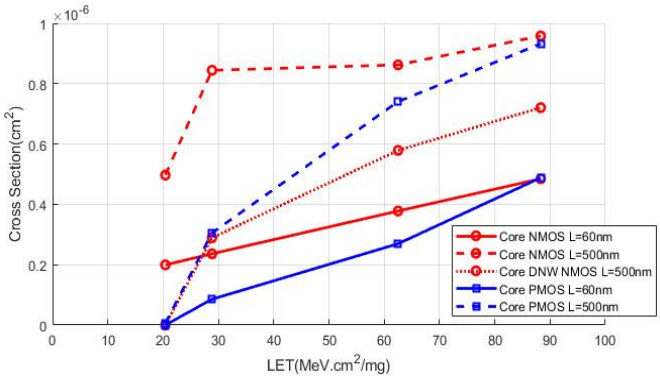

Figure 3 Cross section of core NMOS and PMOS with length of 60nm and 1.2V supply voltage.

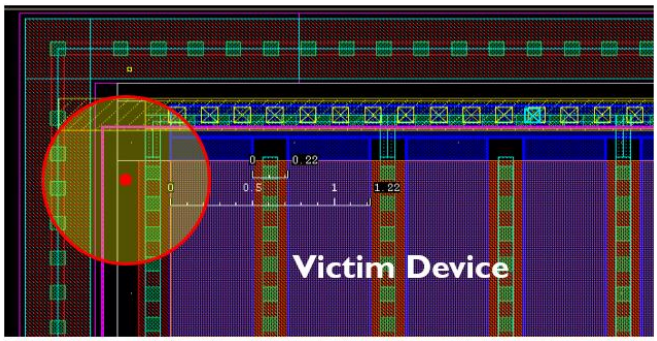

Figure 4 Ionization radius of the heavy ions needs to be considered when calculating the sensitve area

V. SET PULSE DURATION MEASUREMENT RESULTS

Due to the limitation of the duration measurement methodology, it is hard to make a fair duration comparison between the N-type and P-type victim devices [1]. Therefore, the duration measurement results are compared only within the same type of victim device.

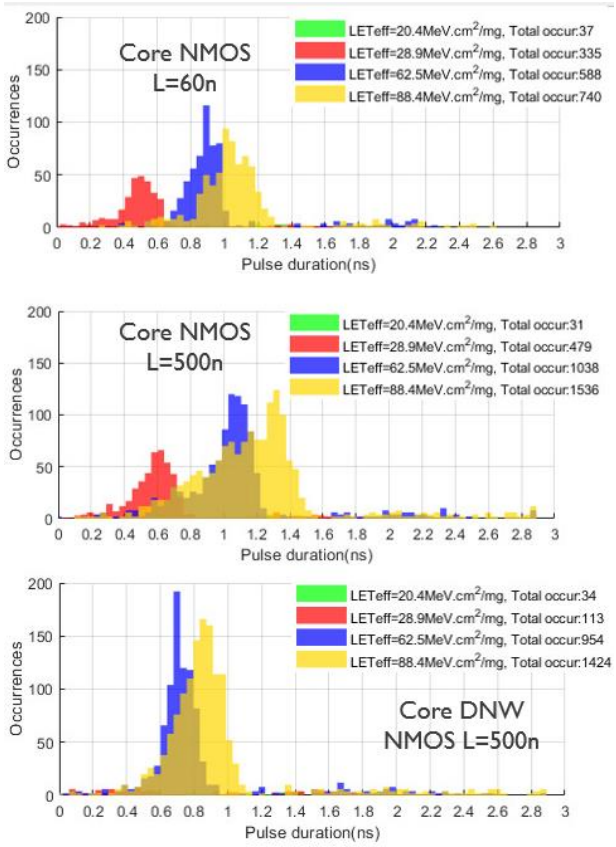

Figure 5 Pulse duration measurement results of Core NMOS.

The SET pulse duration measurement results of core NMOS with a channel length of 60 nm, 500 nm and core DNW NMOS with a channel length of 500 nm are shown in Fig. 5. One SET pulse measurement reading is considered as one occurrence. The y-axis indicates the number of occurrences at each pulse duration (x-axis). The total number of occurrences is also marked in the legend of each sub-figure in Fig. 5. Several common patterns can be found in all three sub-figures: First of all, when the effective LET = 20.4 MeV·cm^2/mg, the maximum voltage drop is not sufficient to trigger the measurement circuit and there is no clear distribution plot. Secondly, a higher effective LET heavy ion can cause both a higher most-frequent duration, a wider duration distribution range, and the total number of occurrences. This is expected since a higher effective LET heavy ion can introduce more ionized charge into the circuit and causes a longer time to recover to the original voltage. Though most duration readout forms a bell-shaped distribution when effective LET ≥ 28.9 MeV·cm^2/mg, sporadic high duration events happened outside the bell shape. The reason for these high duration events is that double hits happened in one measurement period. The effect of the channel length on SET duration demonstrates that a longer channel can cause a longer duration since the total transistor area is increased. When the heavy ion hits the gate area or even the source area, there will be some charge collected by the drain by diffusion. This result is consistent with the results from the charge measurement. When the DNW is applied to the N-type transistor, the total number of occurrences is reduced for each effective LET. Besides, the most frequent duration and the distribution range are reduced. This can be explained by two points mentioned earlier in the section on the charge measurement results: the DNW collected part of the ionization charge through the local p-well/DNW junction and isolates the charge below the DNW keeping it from being collected.

The duration measurement results of the core PMOS victim devices are shown in Fig. 12. The unit device cross-section is derived (Occurrences / *Fluence* / No.Devices. If the measurement results exhibit a bell-shaped distribution, the most frequent pulse duration (square in the figure) and upper/lower boundary (horizontal bar in the figure) are plotted. Similar duration trends can be found when the effective LET and channel length vary. It is noteworthy that, compared with the unit device cross-section results from ionization charge measurement in Fig.3, duration measurement cross-section results show the same magnitude but slightly lower values. This is explained by the fact that in the duration measurement circuit, the victim devices are widely distributed in *M* (*M* > 100) blocks and the boundary space of the victim devices in each block contributes a more sensitive area.

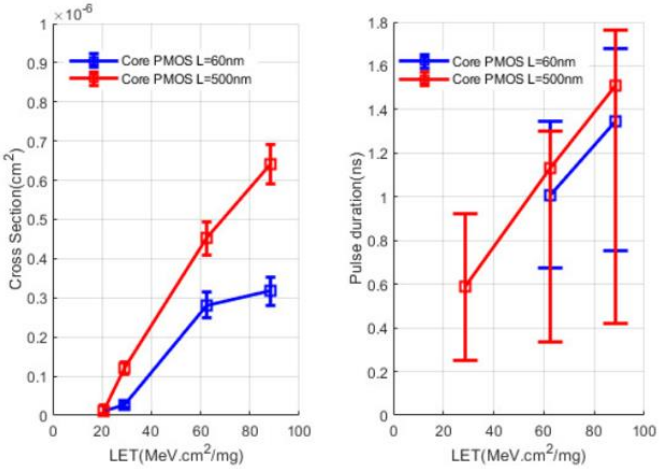

Figure 5 Pulse duration measurement results of Core PMOS.

VI. CONCLUSION

A 65 nm test chip had been successfully tested in the test campaign in the UCL facility. The eight most widely used transistors are implemented as victim devices to measure their SET charge and pulse responses. The measurement results revealed not only the quantity of the SET charge amount and pulse duration but also proved the SET response mechanism behind the different types of transistors.

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