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Title

Flexible Test System for Single Event Effect (SEE) Characterization of Digital and Mixed-Signal Integrated Circuits

Summary

This paper presents a flexible Single Event Effect (SEE) test system designed to detect and record Single Event Upsets (SEU), Single Event Transients (SET), Single Event Functional Interrupts (SEFI) and Single Event Latch-ups (SEL) that may arise in digital and mixed-signal ICs from irradiation by heavy ions. The test system is based on a digital core synthesized on an FPGA, a Cortex-M3 Armv7-M microcontroller and miscellaneous circuitry devoted to providing the required supply voltages, process SEL phenomena, generate and process input/output test signals and monitor key voltage levels.

Content

SEE characterization is one of the fundamental tests that integrated circuits for aerospace applications undergo [1] [2]. This characterization is required for both, Radiation Hardened by Design (RHBD) and Commercial Off-The Shelf (COTS) Integrated Circuits. The reduction of costs and development time in this type of characterization is one of the notable demands of the market, for this reason, from the point of view of maximizing efficiency, it is very important to design test systems using design strategies that make these systems reusable, flexible and scalable.

To devise the system architecture presented in this paper, the common requirements in the characterization of high resolution and high speed (16bit, 100MHz) ADCs and DACs, microcontrollers, and the most common IPs, such as Flash RAMs, SRAMs, Configuration Register Files (CRFs), PWMs, GPIOs and serial buses (I2C, SPI, CAN, UART) have been taken as design reference [3] [4] [5].

The system is based on a programmable central control unit together with test IPs synthesized in reconfigurable logic (FPGA), an Armv7-M Cortex-M3 microcontroller and additional mixed-signal circuitry including mainly test signal generators, signal analyzers, programmable window comparators, insertable voltage regulators together with a 16-bit sigma-delta ADC-based voltmeter.

In addition, the system has been provided with expandability in 3 main directions:(1) expandable processing capability: Application-Specific Instruction-Set Processor (ASIP)-type Extensible Instruction-Set Architecture (ISA) [6] for the main control unit synthesized on the FPGA, which allows additional instructions and test units to be easily added, along with multiple I/O buses available to increase the processing capability of the system, to which supplementary processors can be added in addition to the Armv7-M, (2) expansion of miscellaneous circuitry: free connectors for expansion daughter boards, and free site on the main PCB to add additional circuitry directly soldered to the PCB, and (3) customizable control GUI: the system includes a GUI devoted to controlling and monitoring the characterization of the circuits during radiation and has a common skeleton from which it is customized for each particular IC to be characterized.

The test system has been used to characterize a RHBD 15-bit resolution SAR DAC, a Pipeline ADC and an automotive-grade COTS microcontroller including on chip IPs such as the Flash RAM, SRAM, External Memory Interface (EMIF) module, ADCs, PWMs, GPIO port and serial buses (SPI, UART, CAN).

The paper will focus on the architecture of the SEE characterization system.

Primary Authors

Carranza-González, Luis

Co-Authors

Ricca-Soaje, Álvaro; De las Cuevas Gómez, Gonzalo

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