Sum-Integration Analog to Digital

Implementation and Evaluation of Sum-Int ADC IP-core on NanoXplore FPGA

9th International Workshop on Analogue and Mixed-Signal Integrated Circuits for Space Applications – AMICSA 2022

Company: PiKRON, s.r.o. (Czech Republic)

Project page: https://gitlab.com/pikron/projects/sumintadc

ESA De-Risk 4000134870/21/NL/GLC/rk

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ADC Conversion Work before SumInt

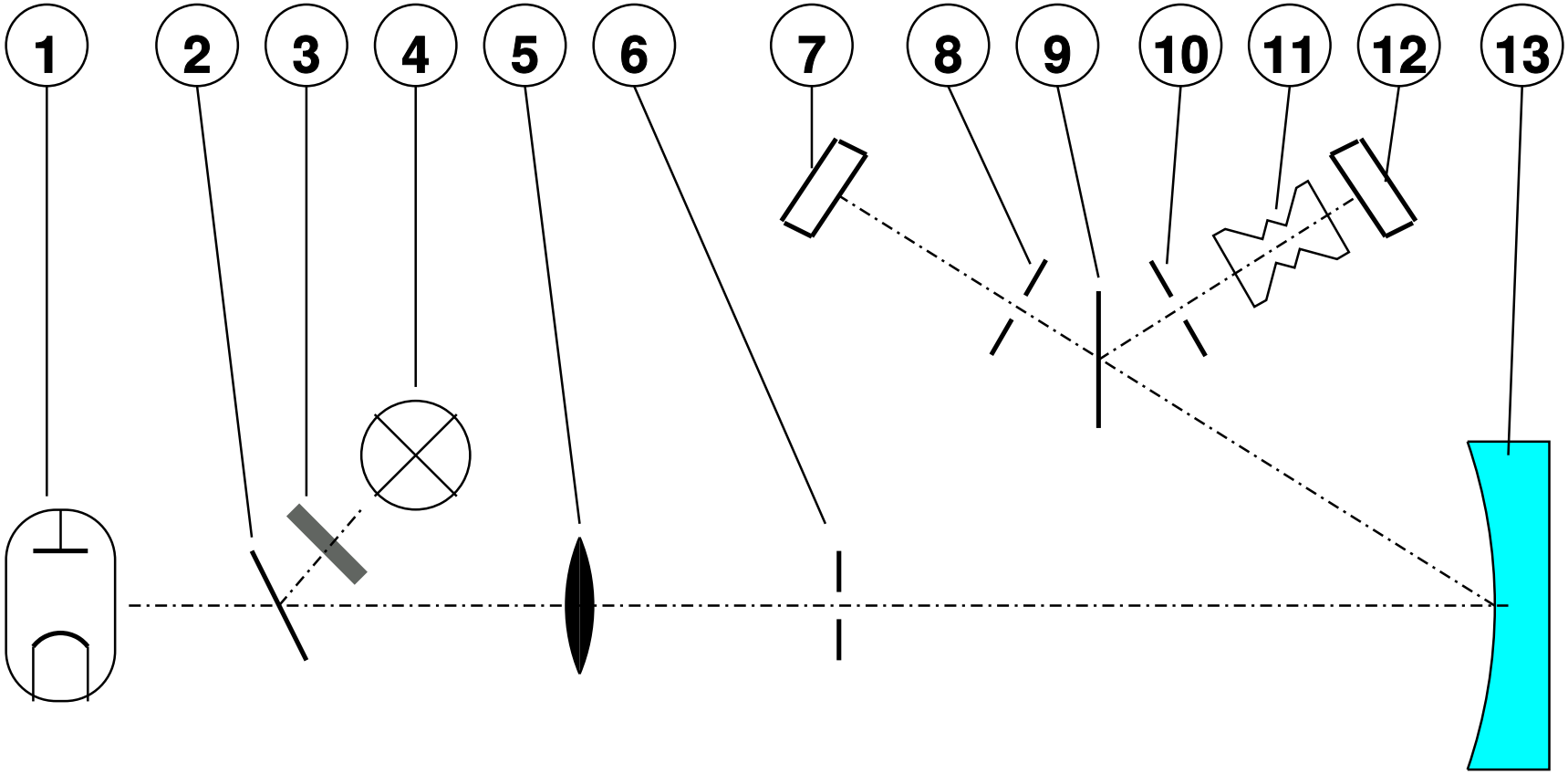
- Design of the new generation of HPLC spectro-photometric UV VIS detector (LCD 4000) at **Laboratory Instruments Praha** company led by Ing. Ladislav Píša was in need of digital signal processing
- Team dissolved due other opportunities offering after 1989 changes and the first year CTU students Pavel Píša and Petr Porazil stepped in to take the design
- Classical double integration principle has been used, the first based on five 74193 chips then on combination of 74193 chip combined with 16-bit counter in Intel 8253
- Design has been successful and first insrument was delivered into Institute of **Organic Chemistry and Biochemistry** of the **Czech Academy of Sciences**

LCD 4000 UV VIS HPLC Detector

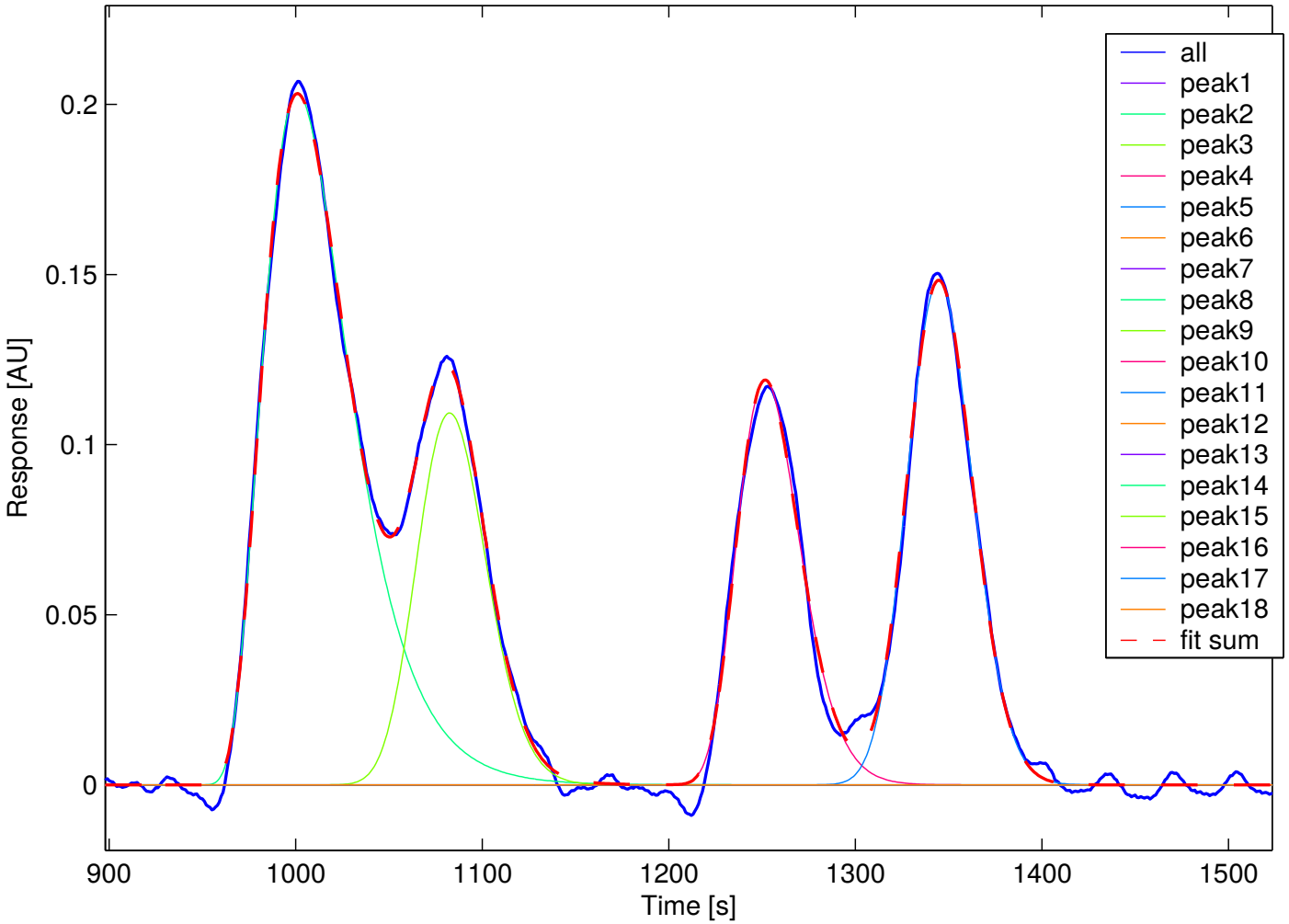
- Many LC 4000 systems has been delivered and served for more than 20 years in daily routine on polypeptide, cancer cure and other research
- Typical system setup
  - LCD 4000 HPLC UV VIS detector
  - LCP 4000 high performance (40 MPa) HPLC pump
  - CHROMuLAN – open source chromatograhy station system

Source: http://pikron.com/pages/company/history.html

HPLC Detector Optical Setup



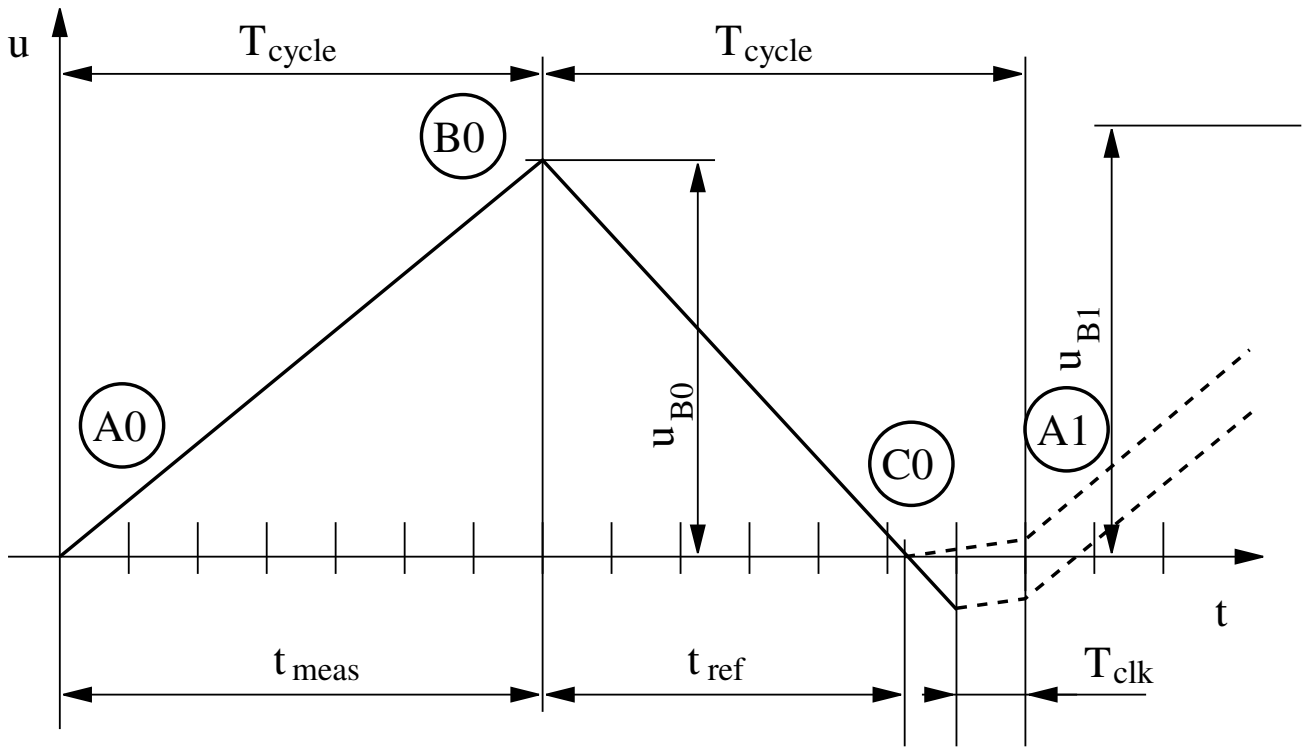
HPLC Signal and Areas under Peaks



The assay output is integral/area under each peak which is proportional to the chemical compound concentration in the original sample

Double Integration ADC Challenges

- The input is integrated only part of time between A_i and B_i
- Start of new cycle at A_{i+1}



- The second problem can be solved by active zeroing but each semiconductor electronic switch injects some charge during changing between conductive and insulator states. Problem is not easy to resolve.

New Detector Design and ADC Wishes

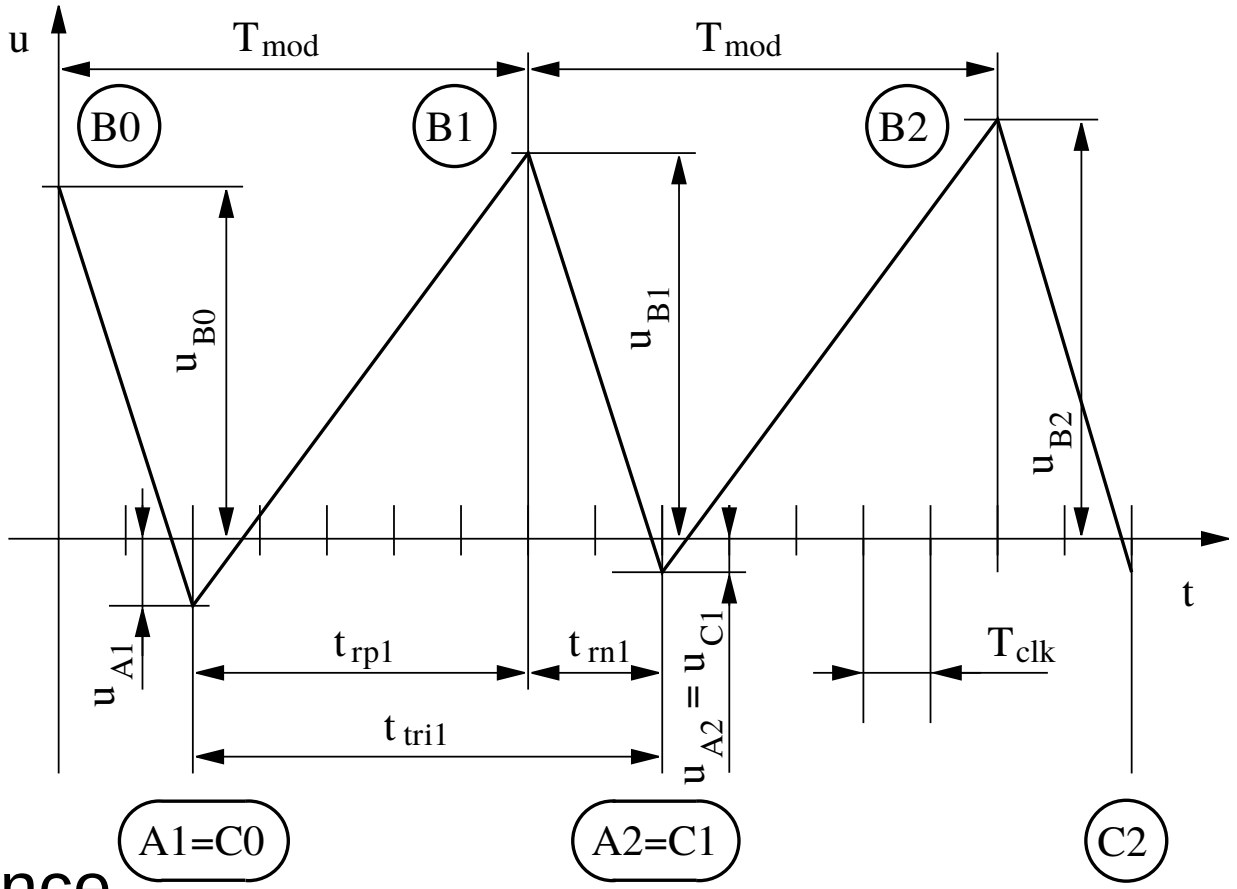
- LCD 5000 – same team but in own formed company
- Required resolution better than $1 \cdot 10^{-5}$ AU.
- Primary digital signals has to allow filtering which suppress noise ideally by better factor than $1/\sqrt{n}$
- Input signal has to be integrated for whole time without a gap (required for a HPLC substances response/peaks area calculations) continuously together with chemical noise
- The conversion has to be monotonic with strict demand on linearity
- The conversion has suppress light source (deuterium lamp) instability, ideally by continuous conversion of ratio between measurement and reference signal (short term stability up to 1 ms is not a problem, high frequency instability is considered as white noise)

ADC Requirements – Continuation

- Long term stability when temperature changes (laboratory conditions 18 to 35°C are presumed)
- Raw samples has to provide minimal mutual correlation (required for fast HPLC applications) at least till 25 Hz sample-rate
- When uncorrelated samples at 1 Hz are considered, electrical resolution of 22 bits is required
- Analog and digital part of the converter has to be separated as much as possible. The whole input range of electrometric inputs from photodiodes is in range of nA and required resolution ideally equivalent to 10 fA
- The converter has to be realized from available componets

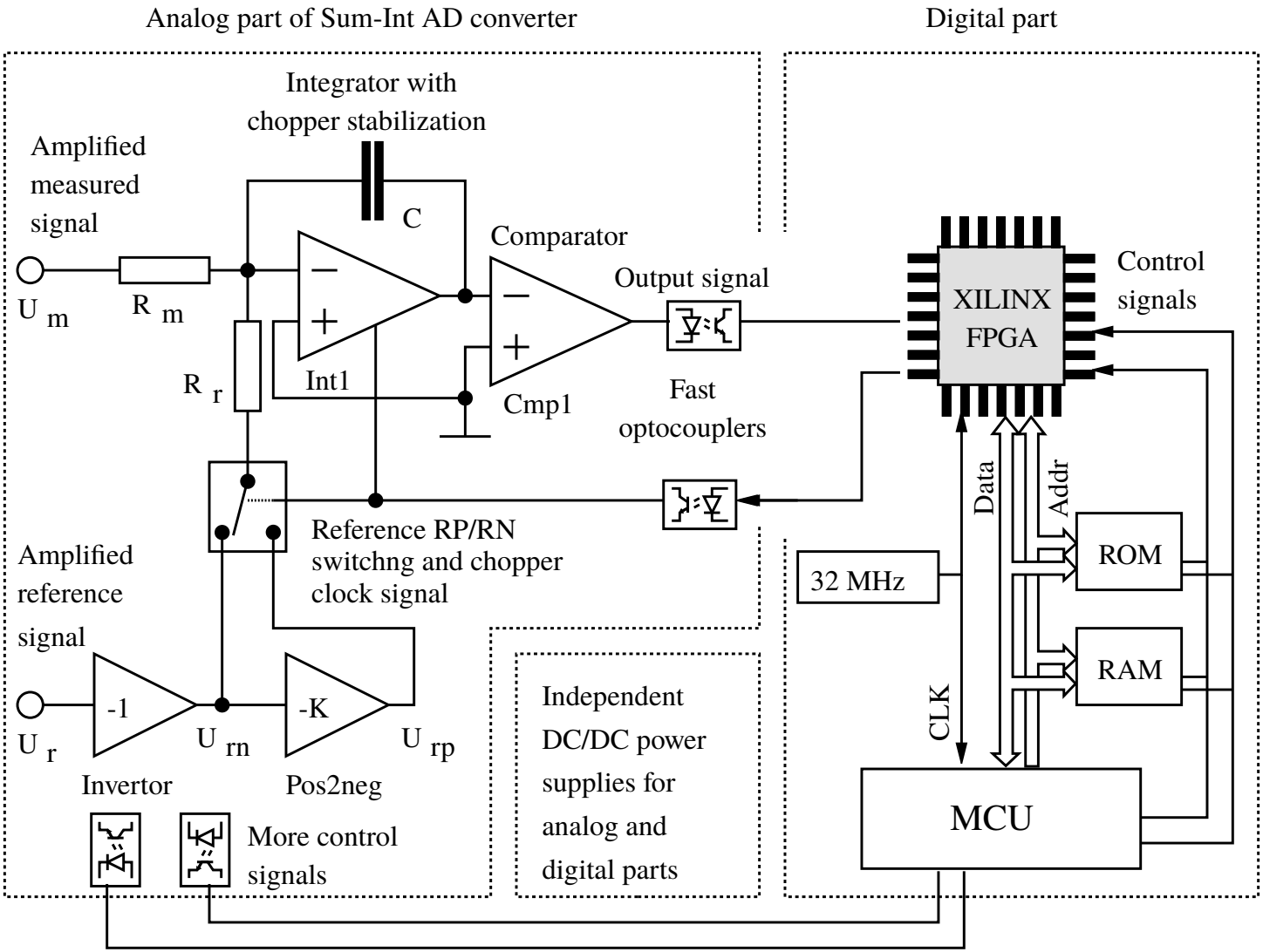
Suma-Integration ADC Principle

- Never reset the integrator
- Continuous integration of input signal
- Switching only application of positive and negative reference

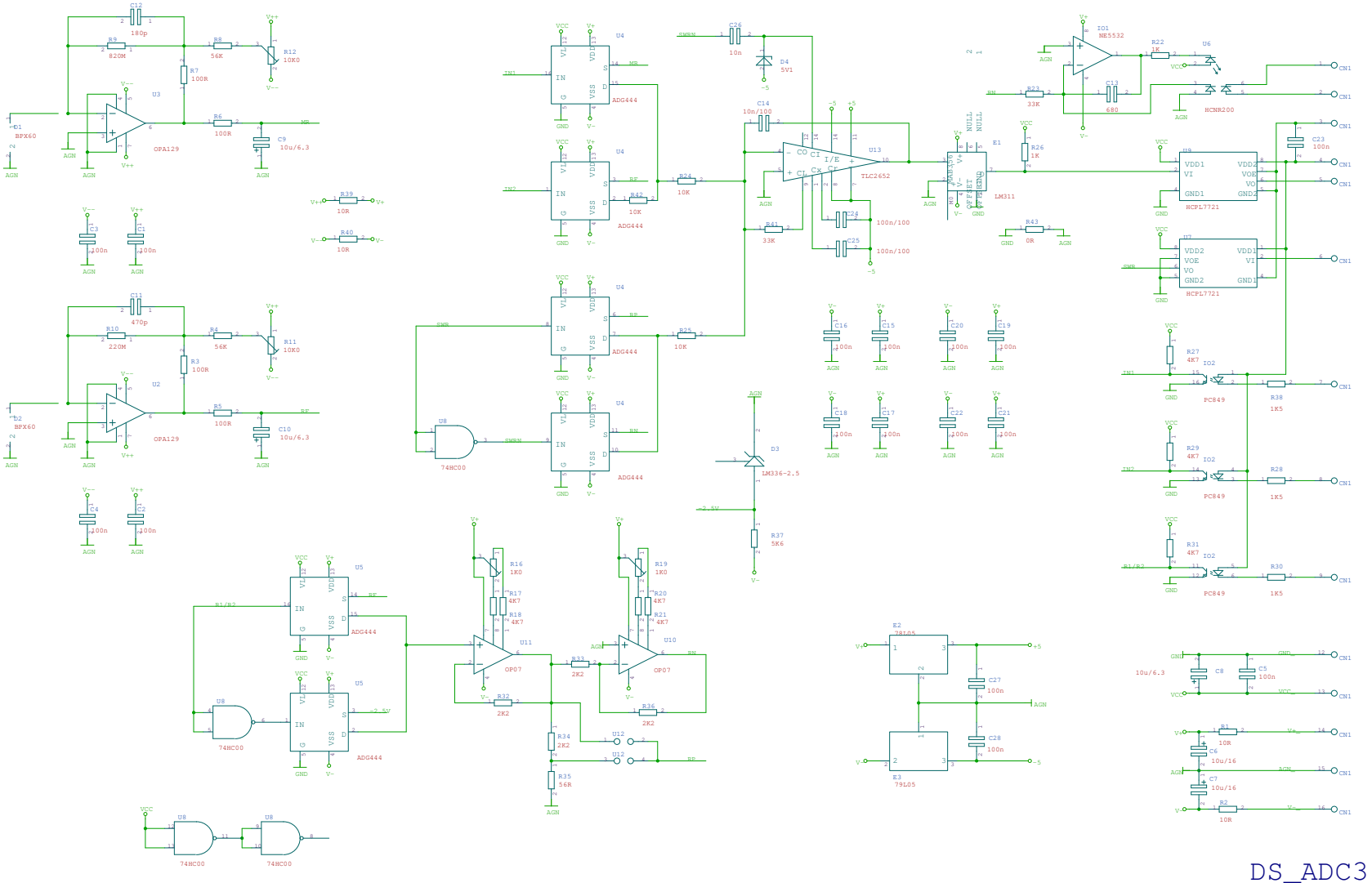


- Error/unconverted charge/voltage reminder preserved into next cycle – zero integral error in theory

SumIntADC Realization In 1999 Year



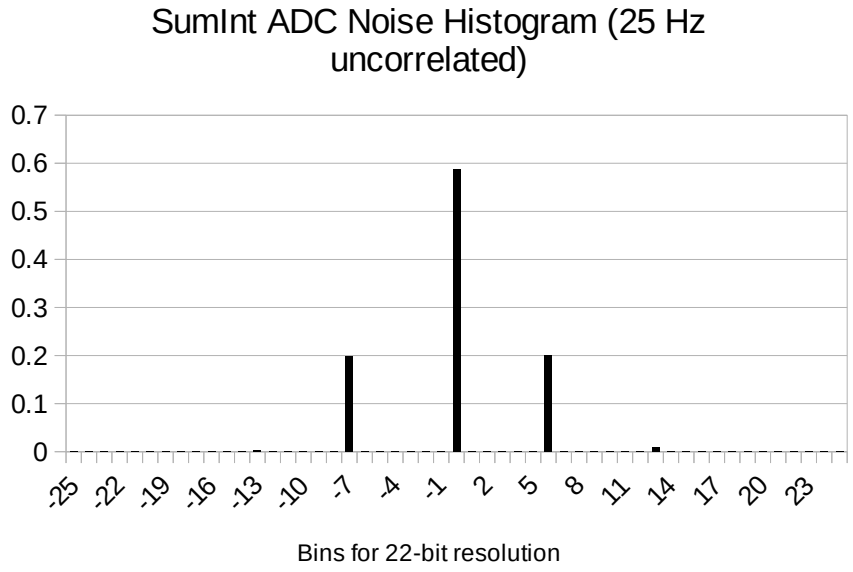
SumIntADC Original Analog Front-end

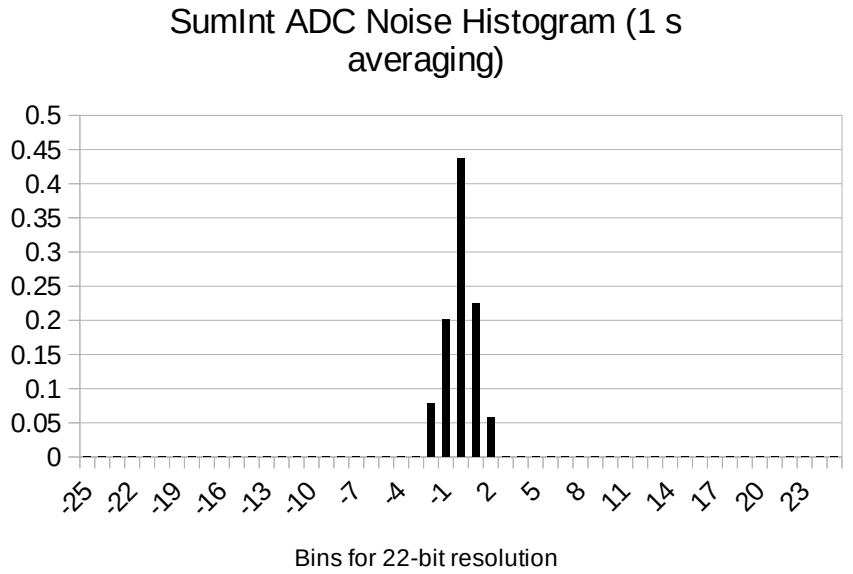


SumInt ADC Critical Components

- OPA129 – electrometric inputs
- OP07 – reference signal conditioning
- ADG444 – switching between positime and negative reference as well as reference and inputs switching
- TLC2652 – main integrator, chopper stabilized, automatic offset voltage zeroing synchronized with conversion cycle
- LM311 – analog comparator on integrator output
- HCPL7721 – optocoupler to drive reference switch and deliver comparator output
- Digital side, 32 MHz driven XC3064-PQ160 and SAB-C509-LM

SumInt ADC Achieved HPLC Results





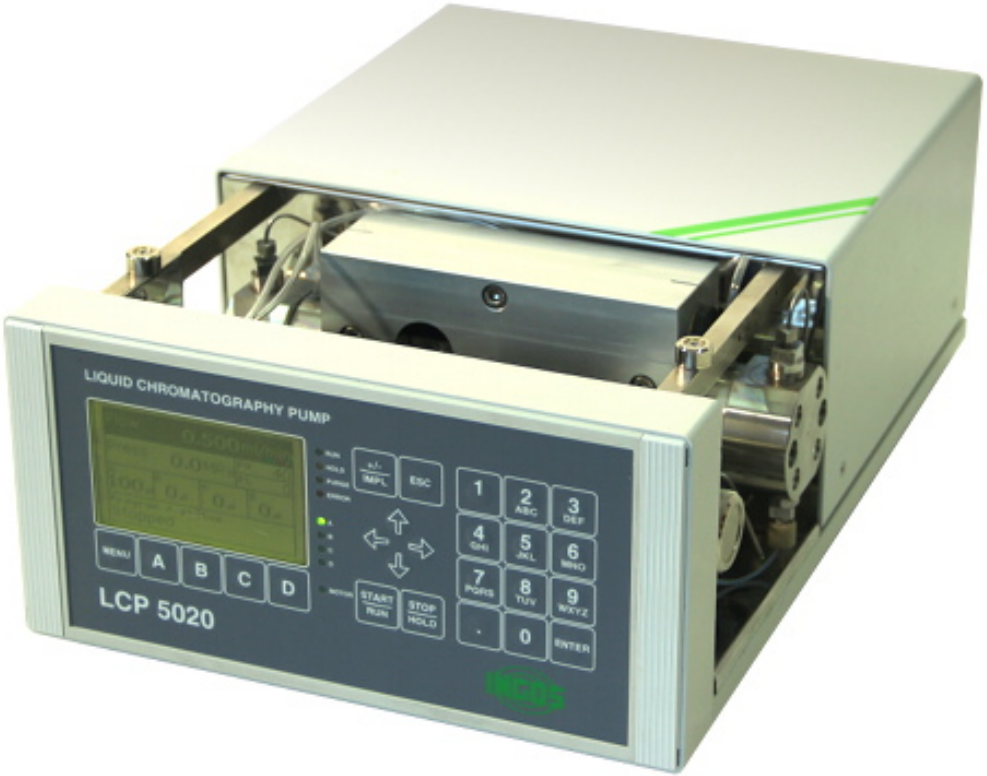
- The bins on graphs correspond to 22-bit resolution
- The signal has been acquired for 300 second
- Raw unfiltered samples acquired at 25 Hz falls into bins equivalent 19 bits resolution. Simple moving average enhances resolution to almost 22 bits. Better than $1/\sqrt{n}$

Digital Design Updated in 2013 Year

- LX_CPU processor board
  - LPC4088 (Cortex-M4F)
  - Xilinx XC6SLX9 – optional
- For HPLC UV VIS detector application FPGA not required
- Whole SumIntADC principle impeded with a half of 74LVC112, 74LVC1G86 and LPC4088 internal counter/timer capture and compare units
- Fast ADC clock (modulator time quanta) frequency increased to 72 MHz

source: http://pikron.com/pages/products/cpu_boards/lx_cpu.html

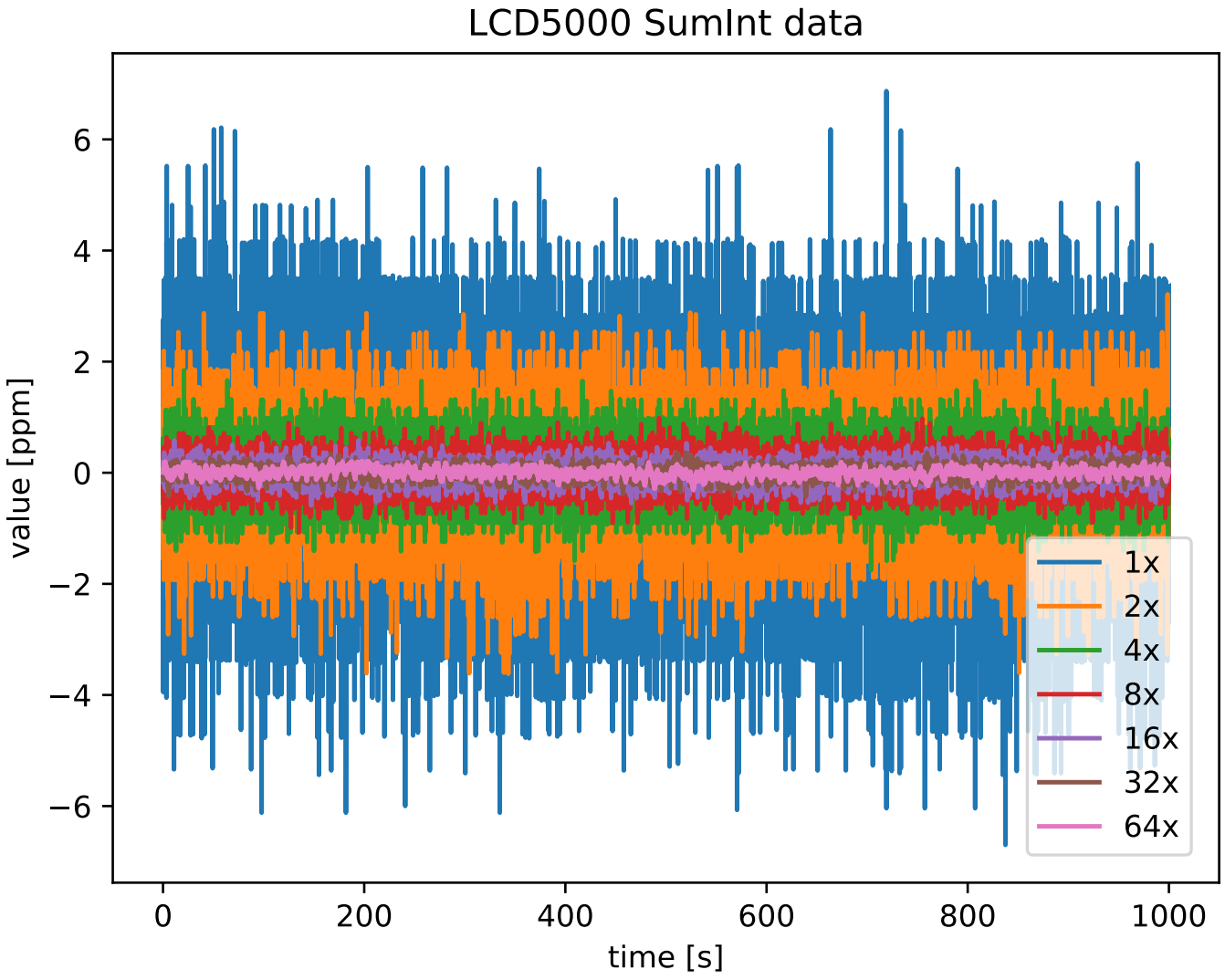
Actual HPLC detector



source: http://www.pikron.com/pages/products/hplc/lcd_5000.html

Complete PiKRON's HPLC Setup

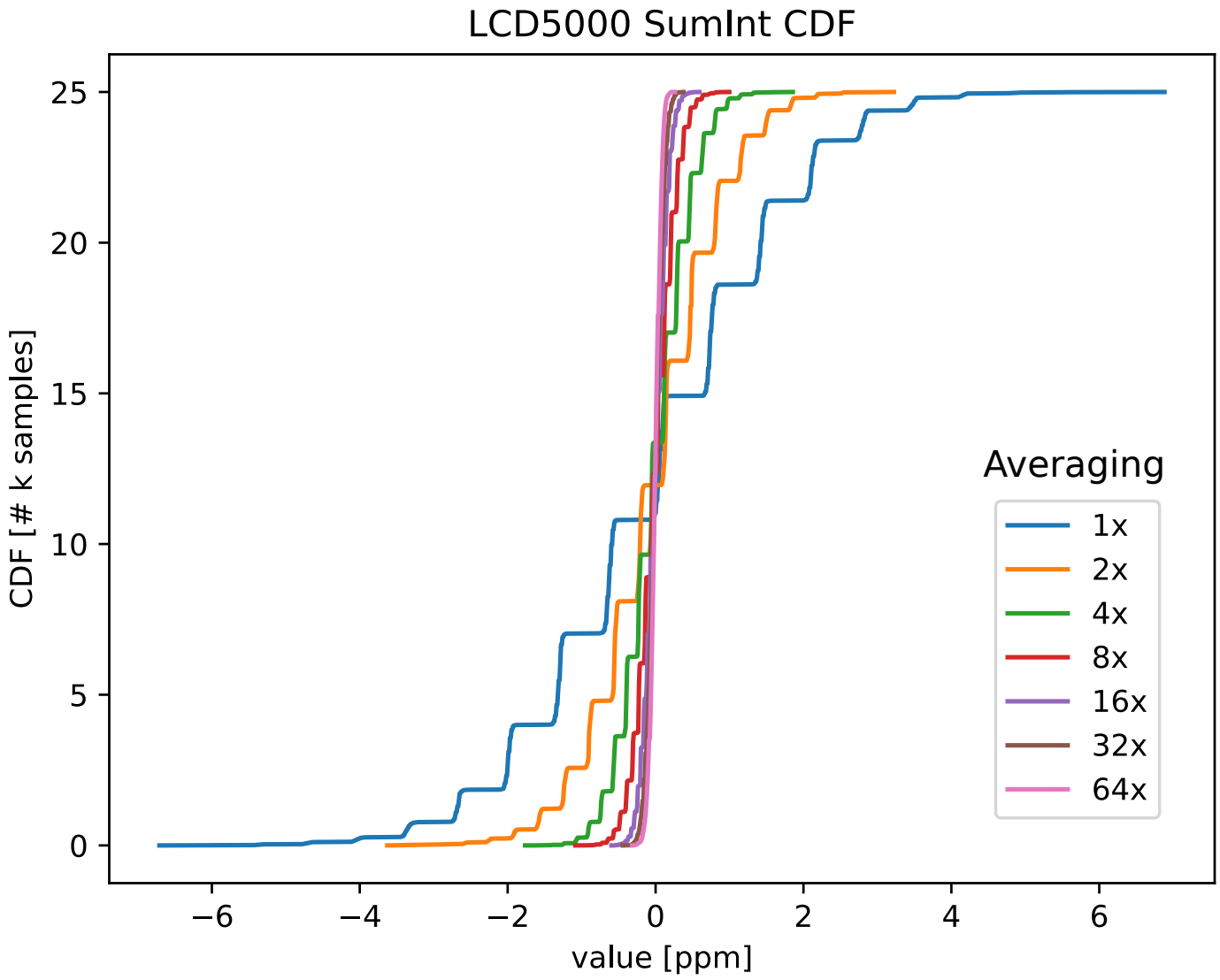
Updated System Zero/Null Signal



LCD 5000/
LCD 61 HW

f_{adcclk} = 72 MHz
f_{adcmod} = 5 kHz
$f_{averaging}$ = 25 Hz
output moving averaging
0.04 s
to
2.56 s

Updated System Zero/Null Signal CDF



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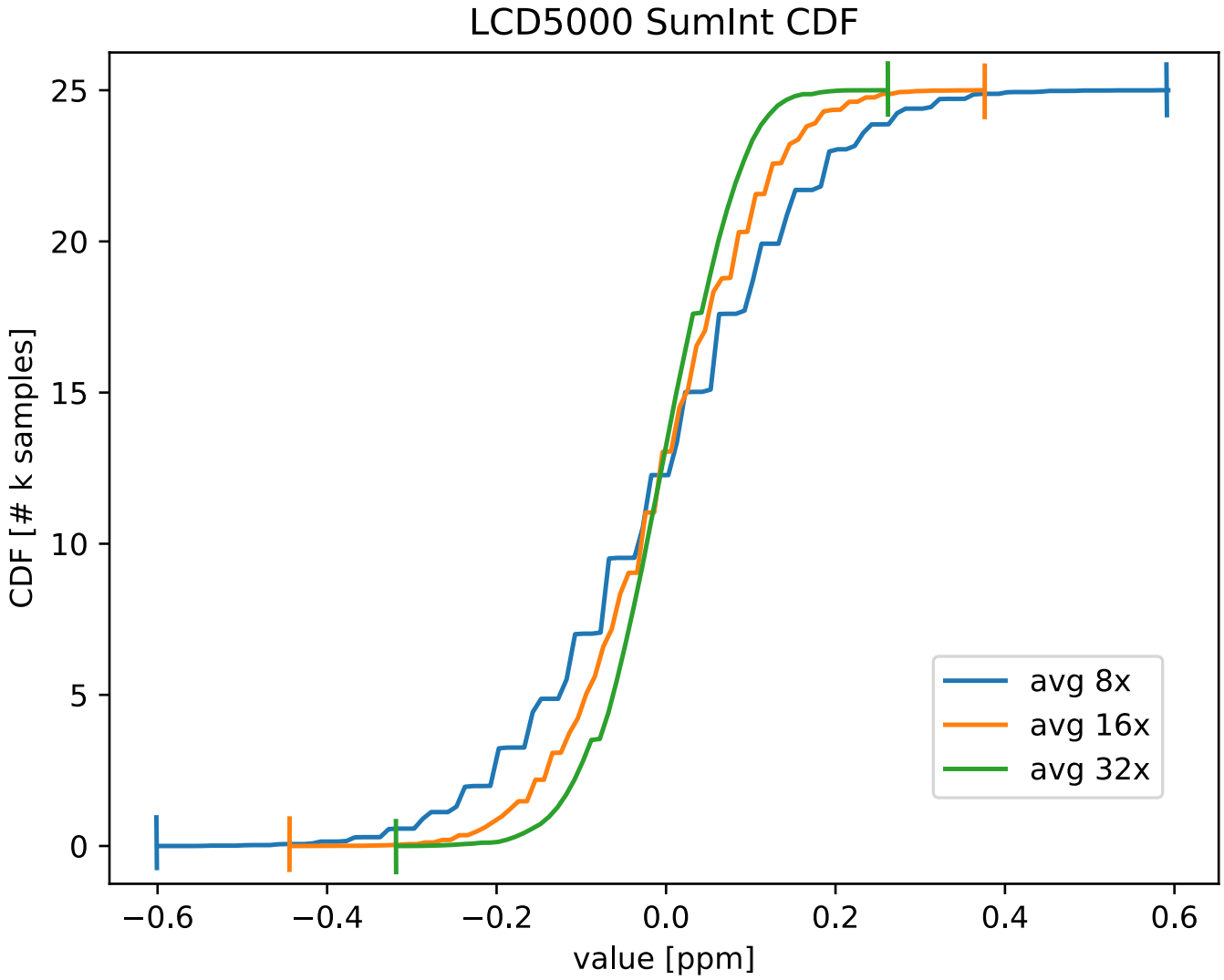
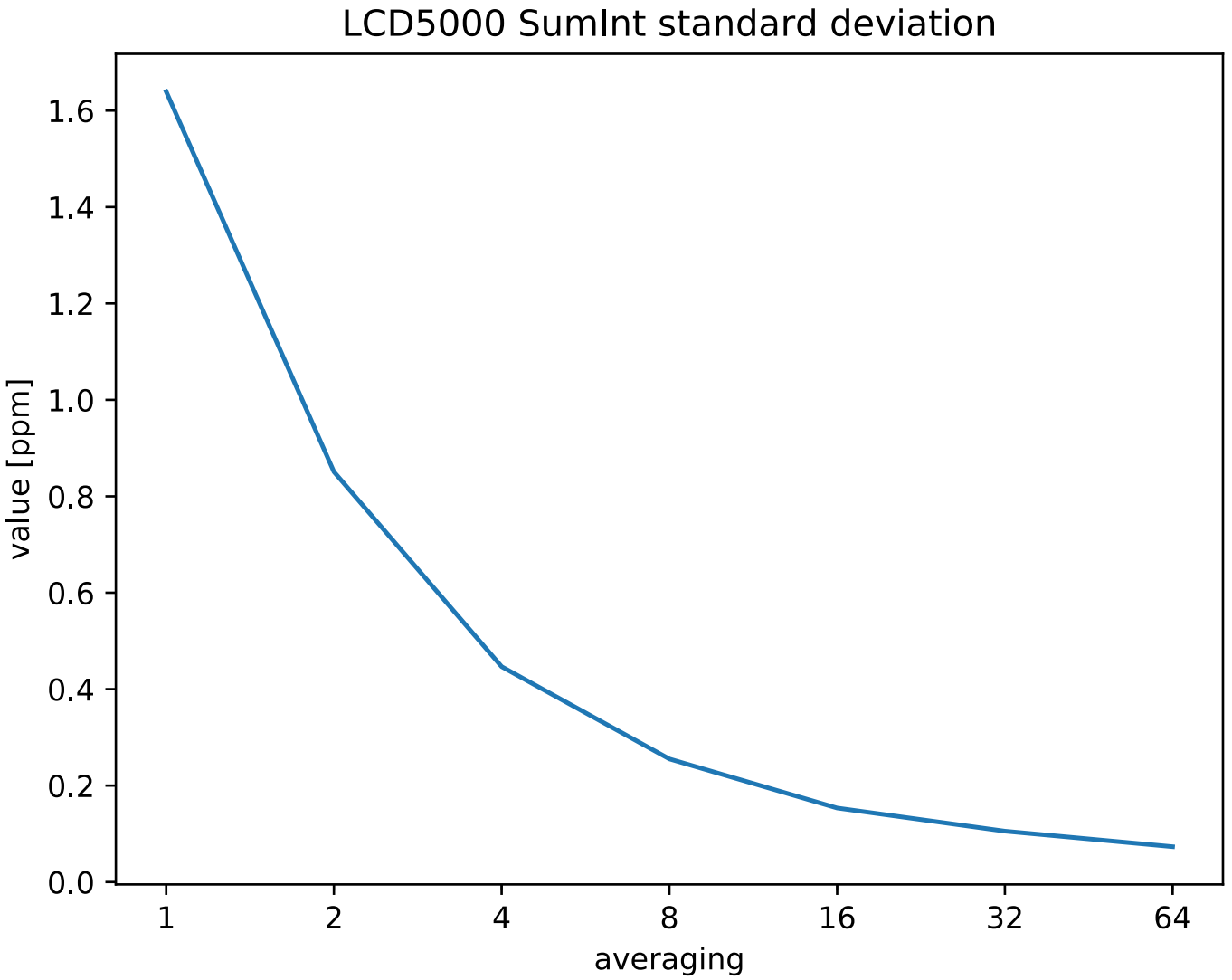


LCD 5000/
LCD 61 HW

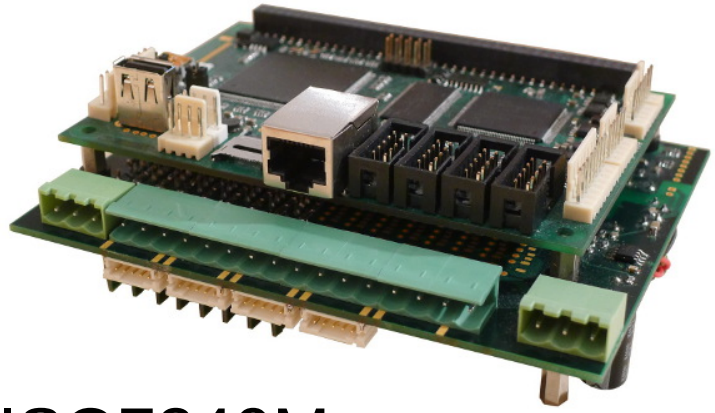
f_{adcclk} = 72 MHz
f_{adcmod} = 5 kHz
$f_{averaging}$ = 25 Hz
output moving averaging
0.64 s
to
2.56 s

Zero/Null Signal Standard Deviation



LX_RoCoN Motion Controller

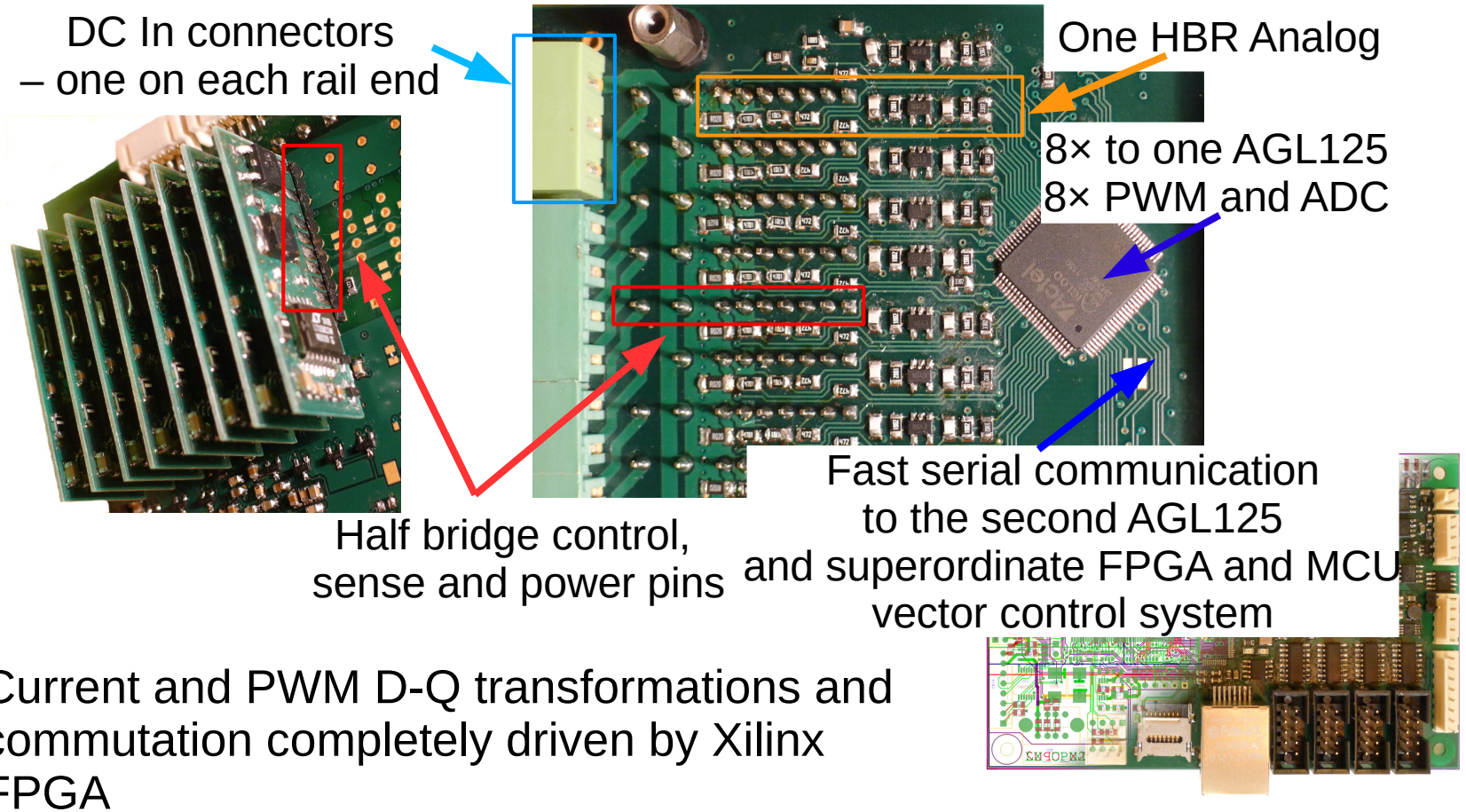
- LX_CPU processor board
  - LPC4088 (Cortex-M4F)
  - Xilinx XC6SLX9



- 16× 5 A, up to 28 VDC
- 16× Microsemi IGLOO and 2× ISO7240M
- SPI like communication between XC6SLX9 and IGLOO
- Return clock signal to match data on 50 MHz
- SumInt ADC realization on MCP6021T-E/OT
- In production from 2016

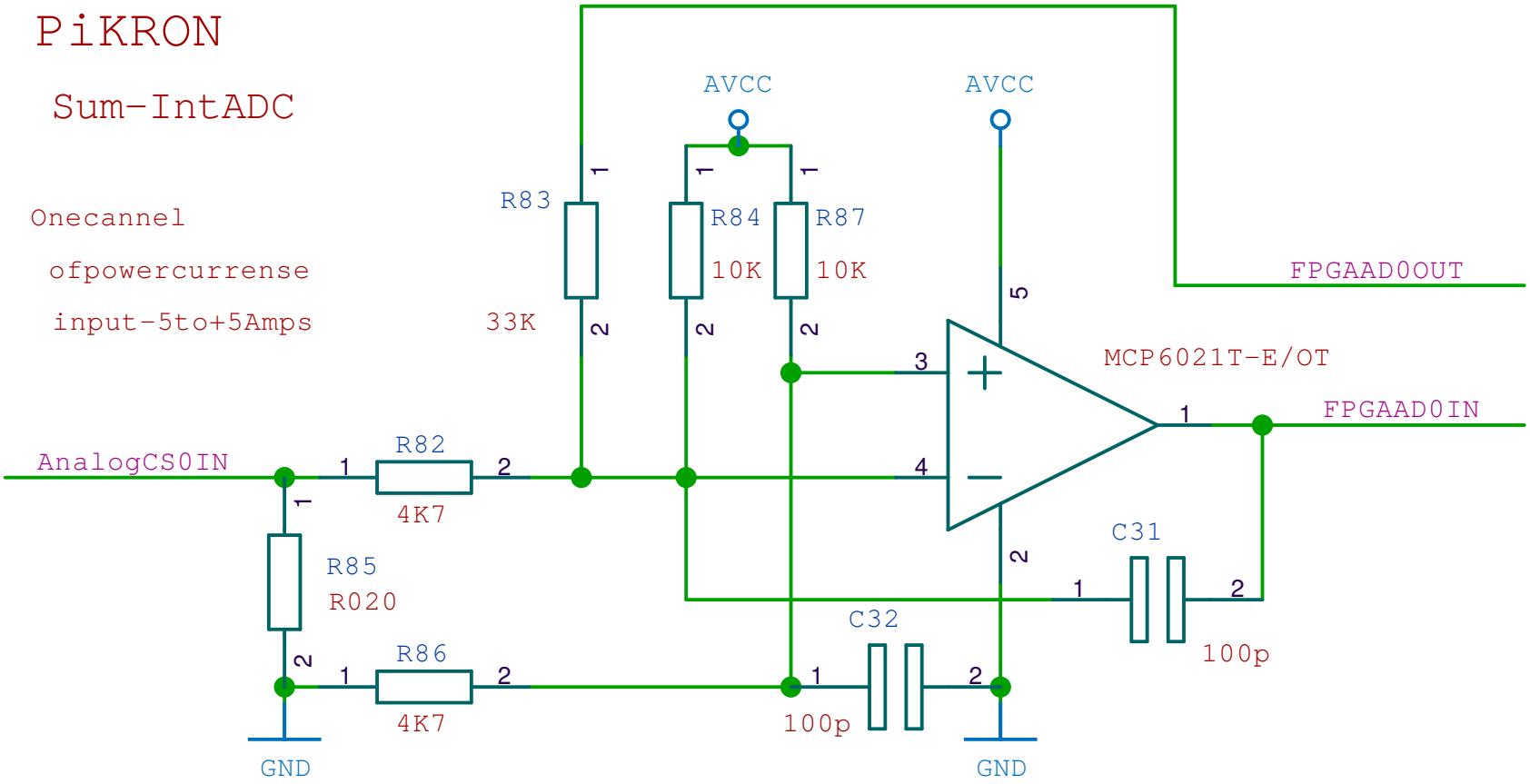
LX_RoCoN SumInt ADC Solution

- Example: up to 4 BDLC/PMSM and IRC equipped or sensor-less stepper motor control (16× 5 A, up to 28 VDC, fully protected phase half-bridges)

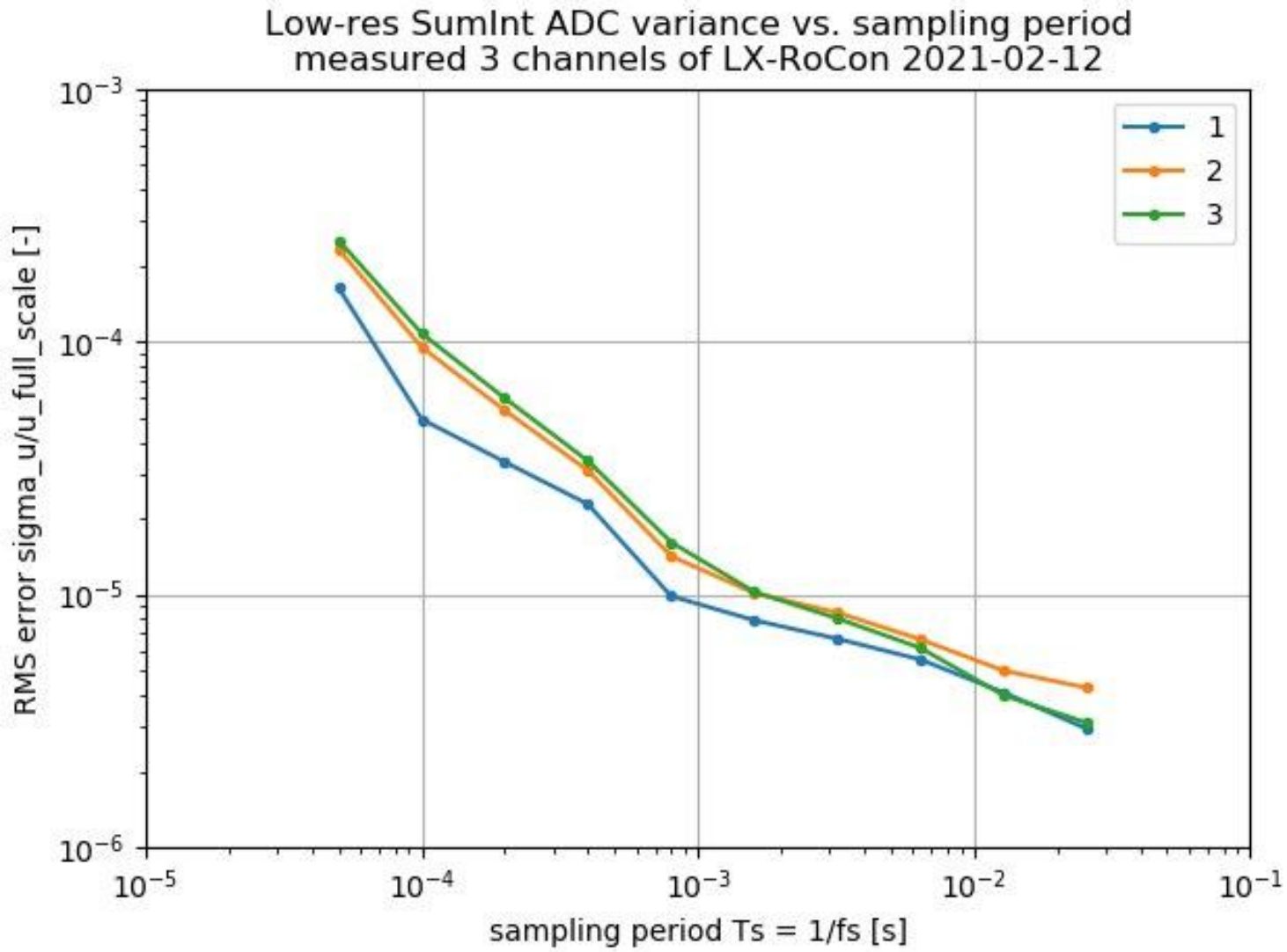


- Current and PWM D-Q transformations and commutation completely driven by Xilinx FPGA

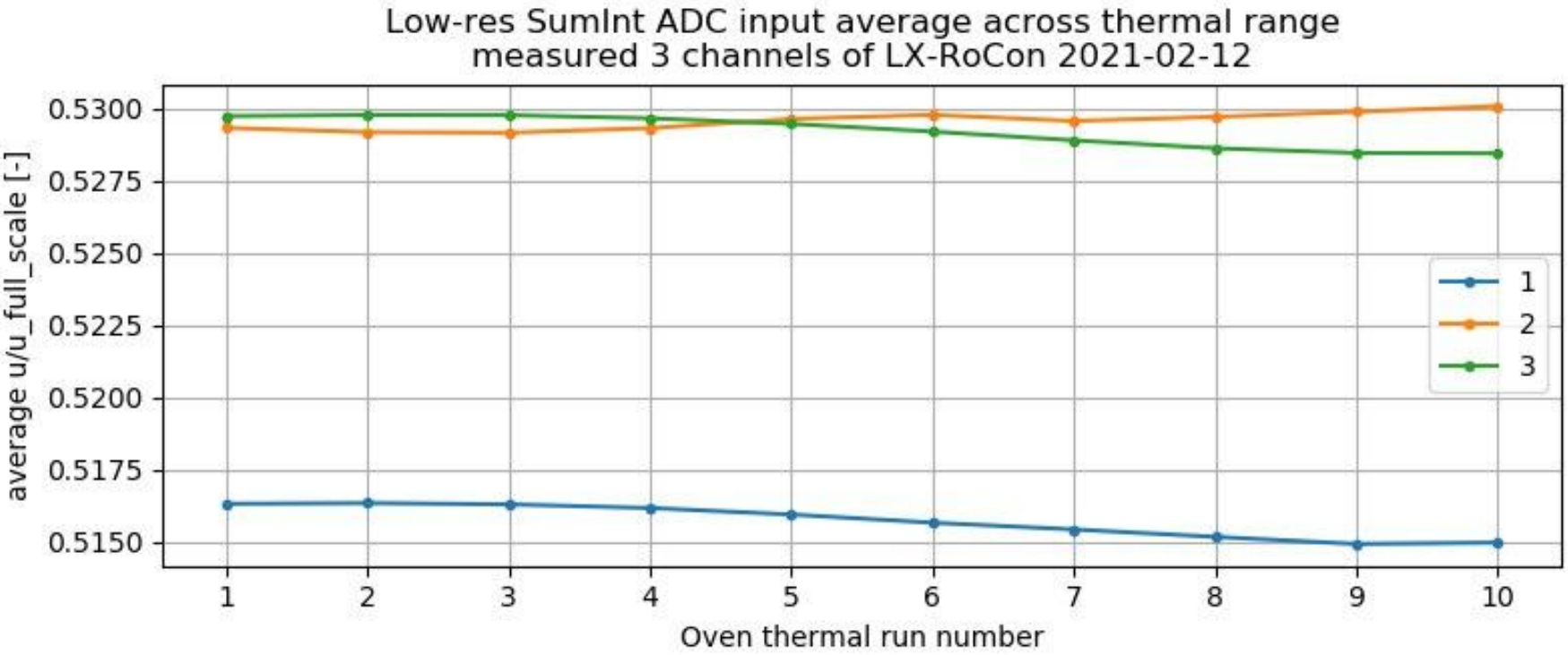
LX_RoCoN SumInt ADC Channel



LX_RoCoN – Noise for Zero/Null Input



LX_RoCoN – Test fom 24°C to 74°C



Available Space Grade Components

- List of ESA Qualified Parts
  - ESCC QPL (Qualified Parts List)

    https://escies.org/webdocument/showArticle?id=119
  - ESCIES ESA Radiation Reports

    https://escies.org/labreport/radiationList
- Rad-hard Lists by Chip Companies
  - Texas Instruments – option directly in the regular search
  - STM Space Products

    https://www.st.com/en/space-products.html
  - Analog Devices Space Products
  - https://www.analog.com/media/en/news-marketing-collateral/product-selection-guide/Space_Products_Selection_Guide.pdf
- Other Space Related Components Lists
  - https://www.doeeet.com/home

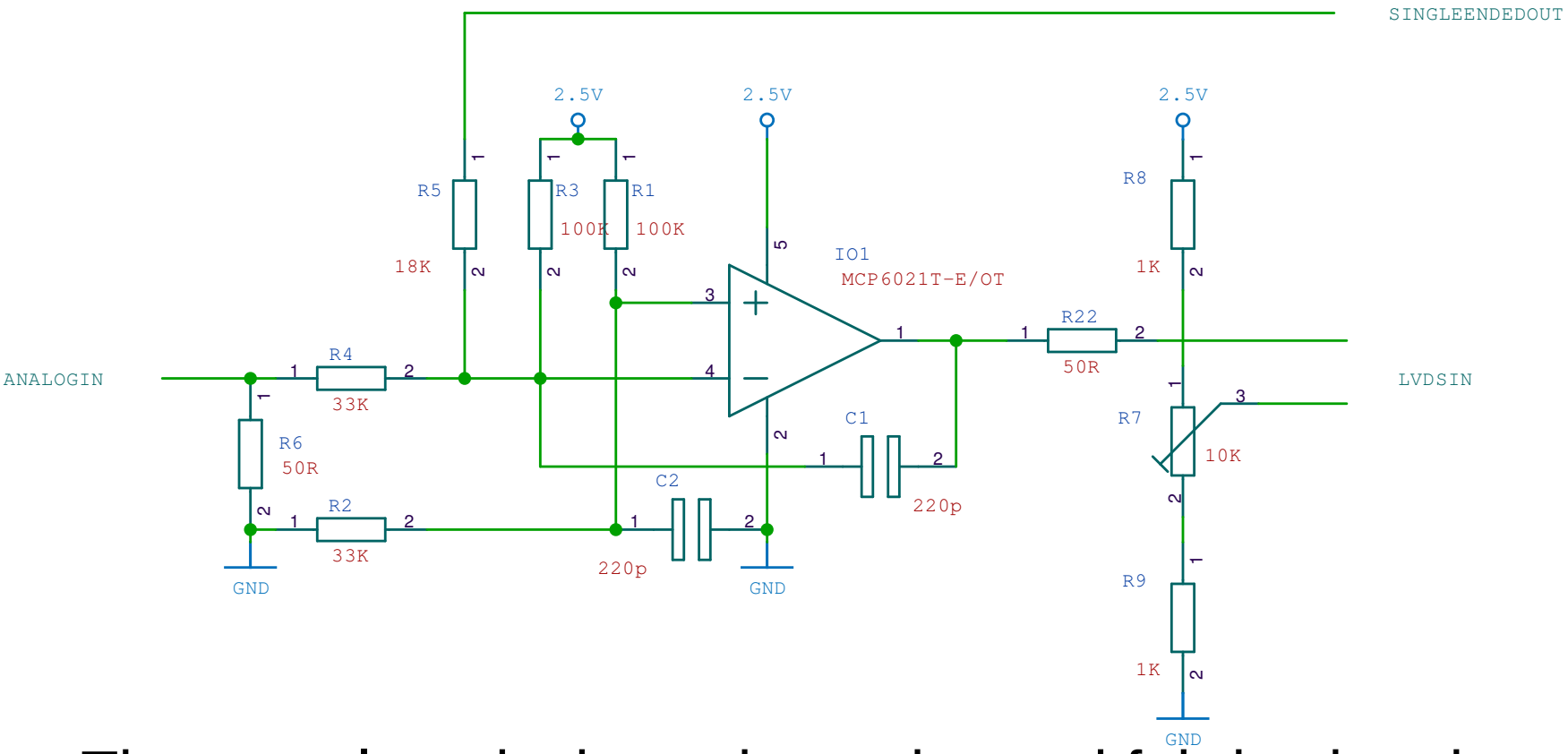
Space Grade Operational Amplifiers

- ADA4084-2S VCC 3V to 36V, Offset Voltage typ 20µV, max 100µV, but up to 400 nA input bias at +125°C, declared as rail to rail, fast recovery and comparator, but it clamps inputs over diodes together, declares CMRR @3VDC single supply from 0 to 3 VDC, but according to graph deterior/misbehaves till 1.2 VDC (MCP6021 input bias curret 640pA @+125°C, max 5,000 pA
- ISL70444SEH VCC 2.7 V to 40 V, Offset Voltage typ 20 µV, max 500 µV
- RH1499M VCC 4.5 V to 36 V, Offset Voltage typ 200 µV, max 1100 µV
- LMP2012QML-SP Dual, VCC 2.7V to 5V, Offset Voltage typ 0.8V, max 60uV, CFP 10
- *OPA4H014-SEP offset 120 µV max, drift 1 µV/°C, input bias current 10 pA (–55°C to +125°C ±3 nA), equivalents OPA140AIDBVT and OPA140AIDBVR (found late)*

Other Space Grade Components

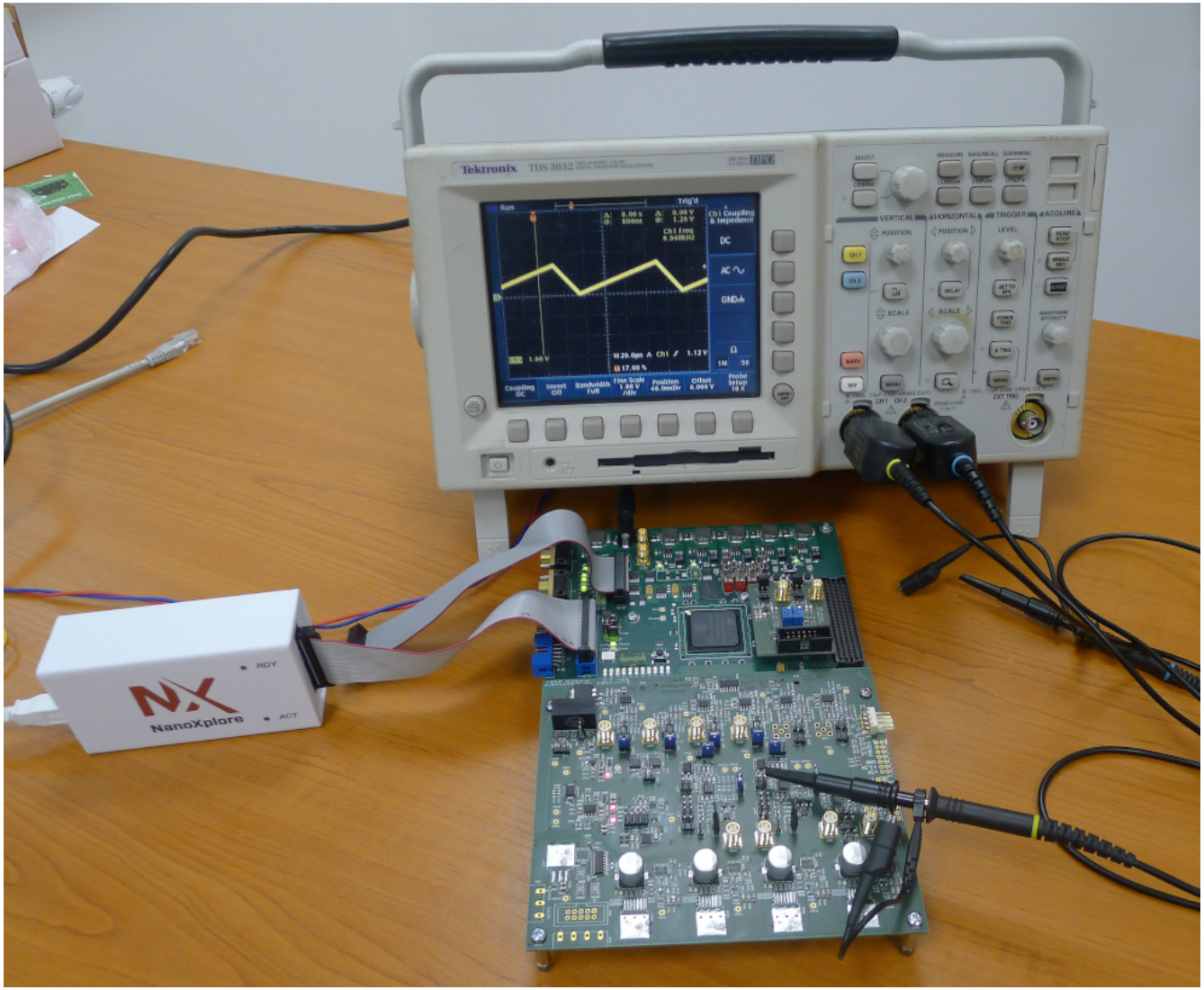
- Digital Galvanic Isolators
  - ISOS141-SEP Radiation Tolerant High-Speed Quad-Channel 3/1 Digital Isolator (NASA's ASTM E595 Outgassing Spec), 2.25 to 5.5 VDC
  - ISO774x-Q1 Automotive, High-Speed, Reinforced Quad-Channel Digital Isolators 3/1
- Linear Voltage Regulator
  - TPS7H1101A-SP - LDO Adjustable 3A V_{in} 1.5-7V
  - LM2940QML-SP - 5V 1A Vin 6-26V
- Voltage Reference
  - LT RH1021-5 - 5V
  - Intersil ISL71090SEH25 - 2.5 V
  - AD REF43S/REF43 - 2.5 V
  - AD AD584S - 2.5/5/10 V
- MOSFET Transistors
  - IRHLF87Y20 - N-channel, $R_{dson} < 32$ mΩ @ V_{gs} 4.5 V
  - IRHLNS87Y50 - N-channel, $R_{dson} < 2.5$ mΩ @ V_{gs} 4.5 V

The Idea Based on LX_RoCoN

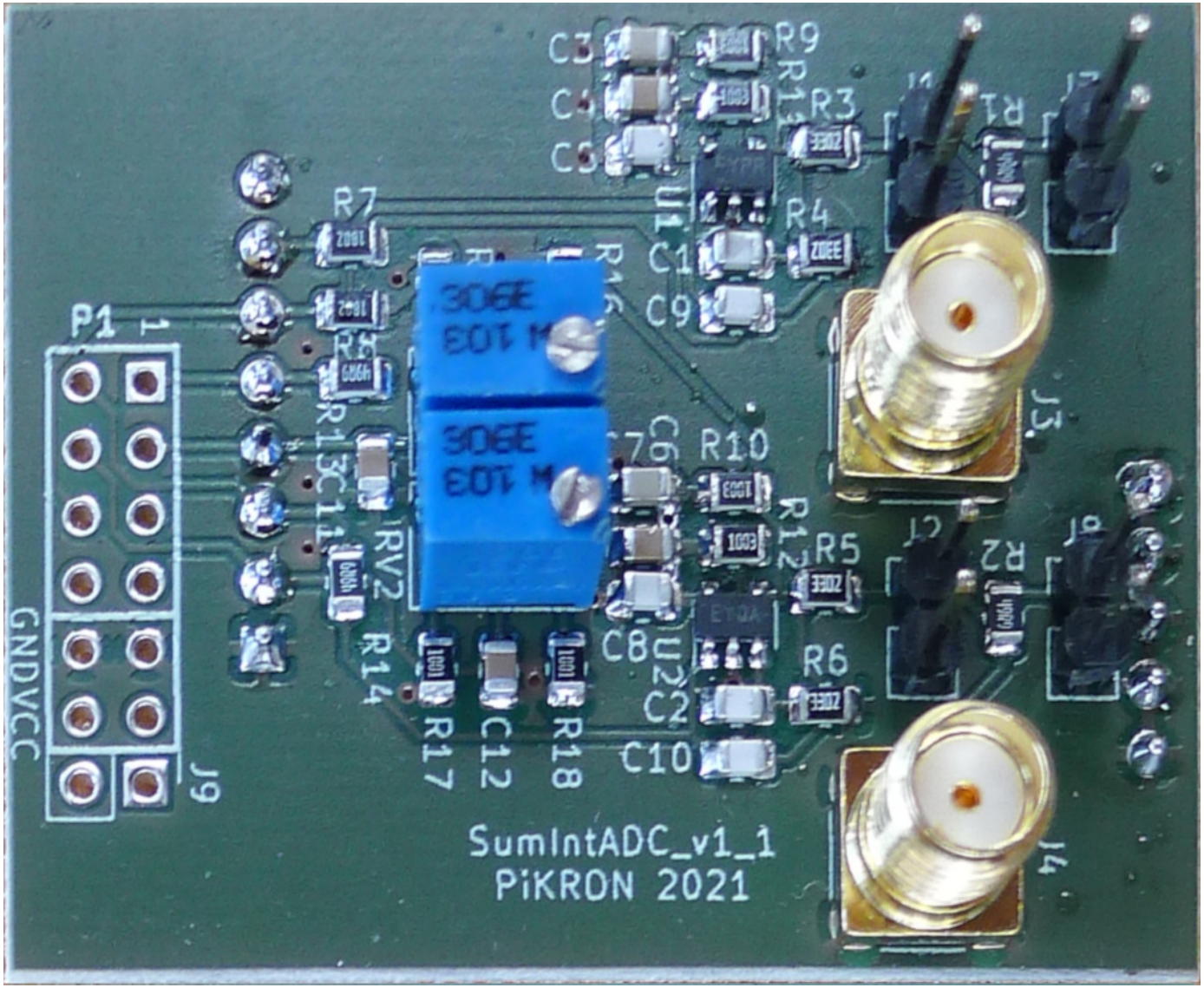


- The complete design schematics and fabrication data in the project repository: simple_adc_cmp_lvds/SumIntADC_v1_1

SumInt ADC Char. – In House

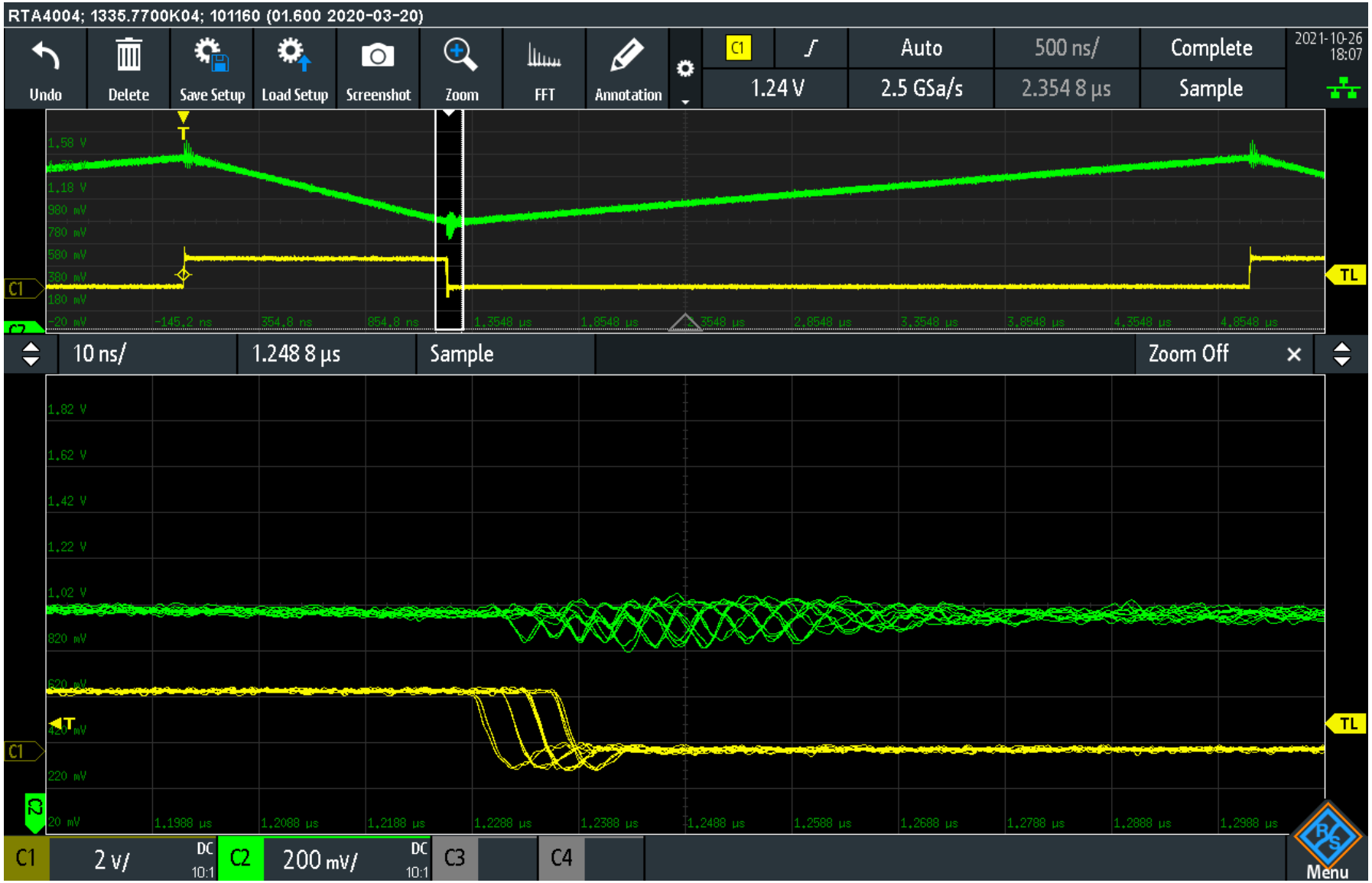


The Test Board 1 Realization



The Test Board 1 Check

The Test Board 1 Check – Detail

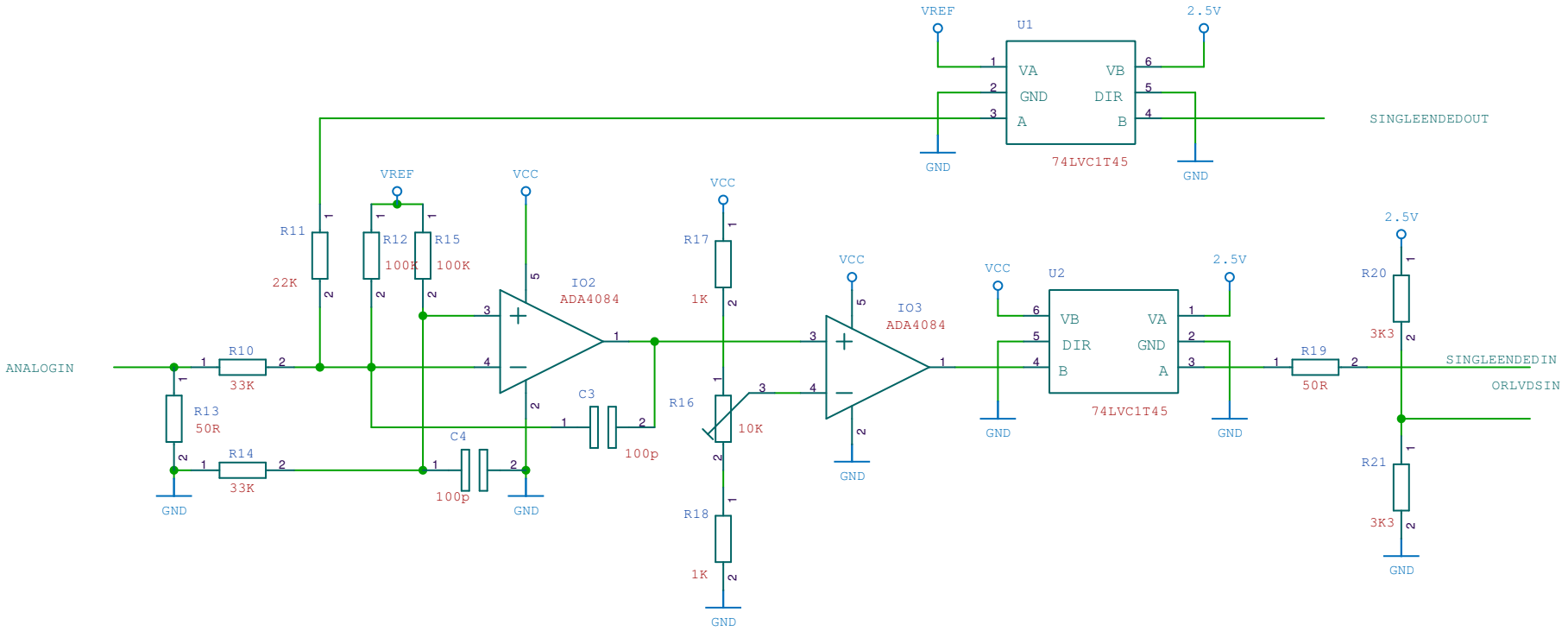


HDL Test Design

- sumint_nx_tp5
- Worked at 400 MHz modulator, 100 MHz logic
- The design taken from lxpwr-agl used on LX_RoCoN

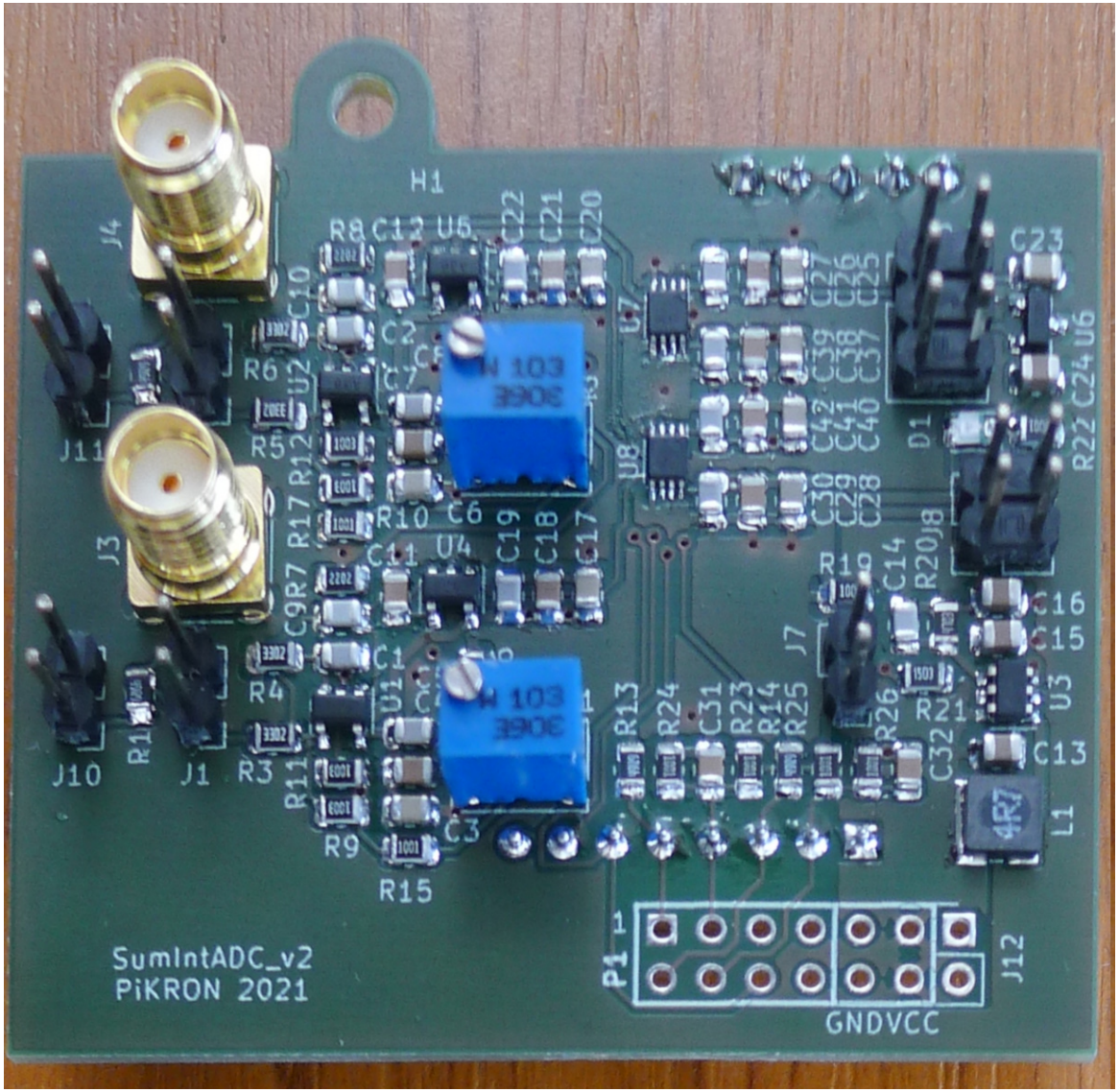
Componet	Lines	Description
pdchain.vhdl	49	pipelined synchronous pulse counter
pdivtwo.vhdl	41	the stage of the counter
siroladc.vhdl	86	sigma-integral rolling ADC digital part
sumint_nx_tp5.vhdl	176	top level test design

Initial Idea with ADA4084



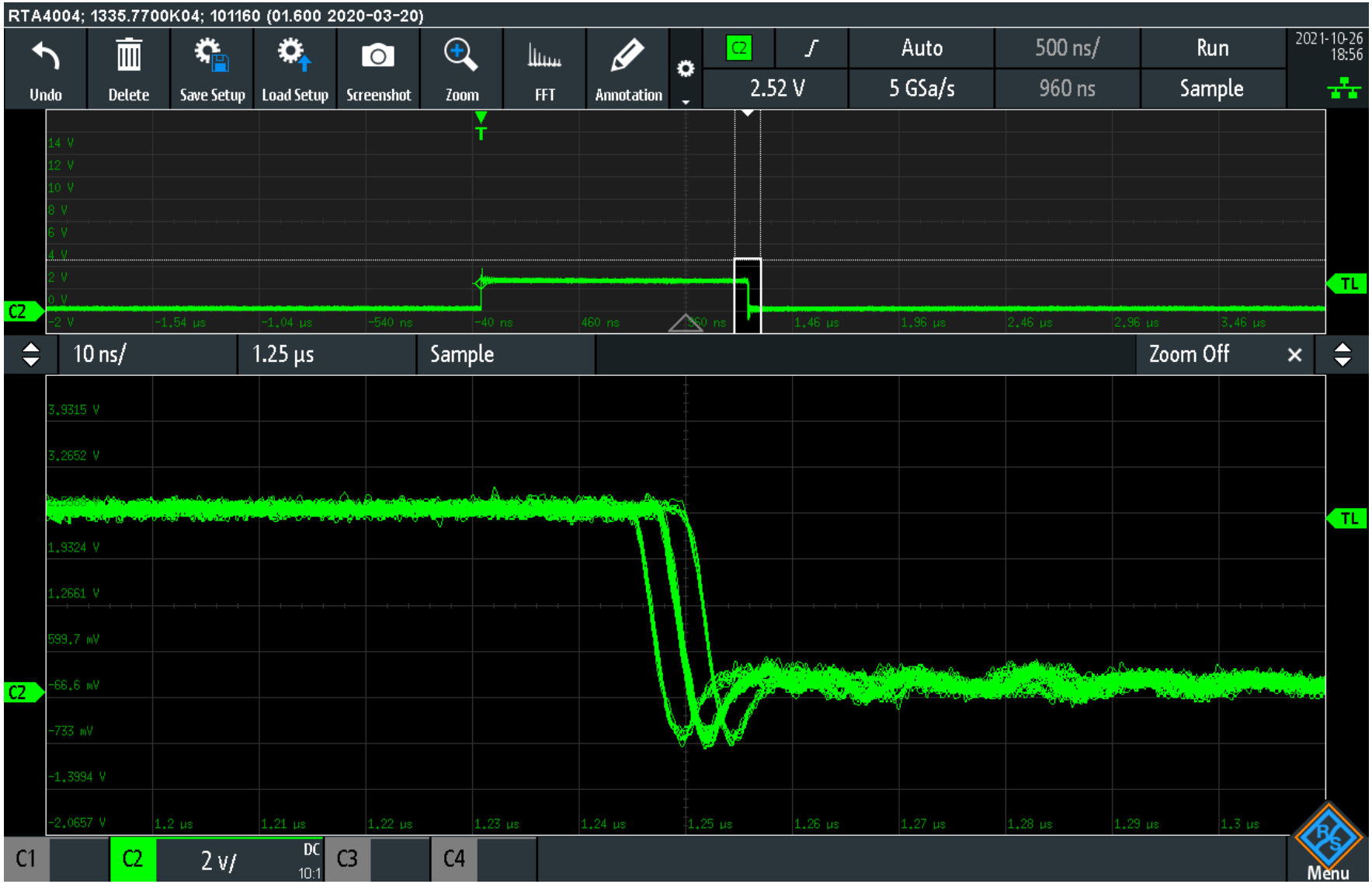
- In this design a digital lever shifter is used as fast reference voltage switch
- Unnoticed problem with ADA4084 diodes on inputs, the second removed
- Complete: simple_adc_cmp_ext/SumIntADC_v2.pdf

The Test Board 2 Realization



The Test Board 2 Check

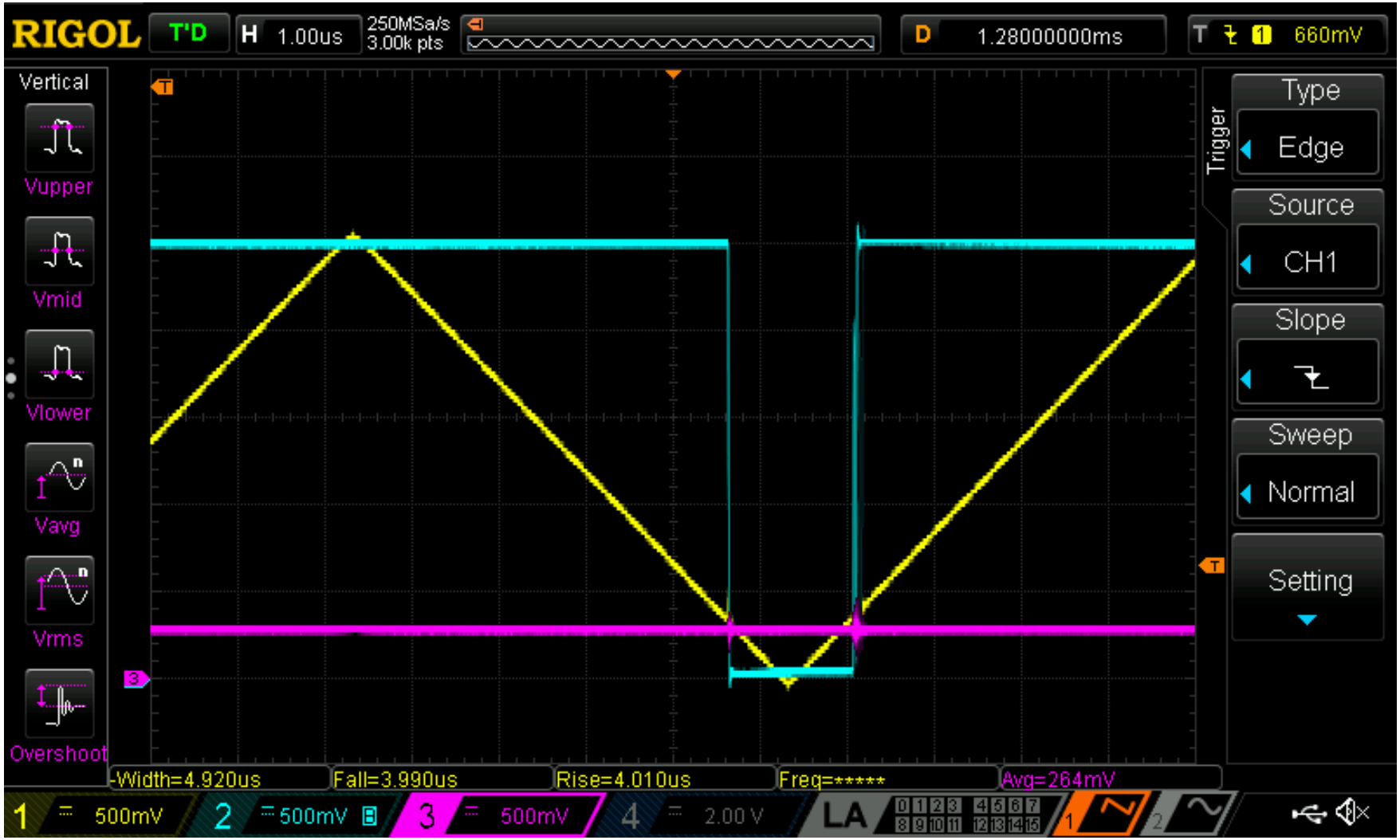
The Test Board 2 Check – Detail



NanoXplore LVDS Pins Assessment

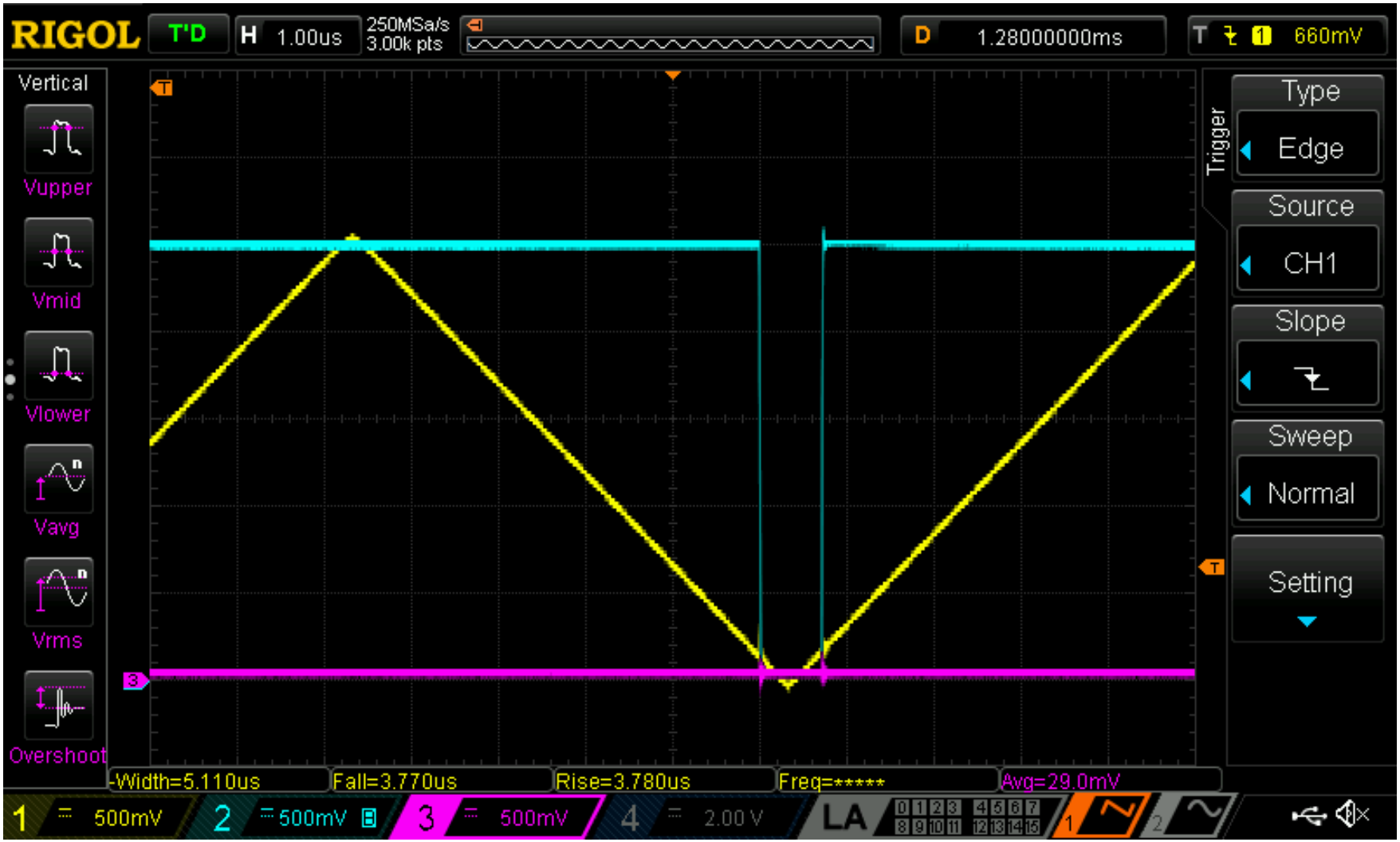
- triangle signal wired input to a positive LVDS terminal
- potentiometer from bank supply to a negative LVDS terminal
- LVDS input fed directly (without FF) to the single ended output
- proved, LVDS input termination is off, no influence to triangular signal on positive pin when negative on is tuned in expected operational range with 100 and 10k Ω signal source
- comparator checked to provide expected performance with minimal delay from 0.2 to 1.9 VDC tuned on the negative input
- for the lower and higher values on the negative input the comparator timing, pulse width does not match intersection between compare level and triangular signal well.
- conclussion: comparator level between 0.5 to 1.5 VDC trig event matches expectations.
- without flip flop on the comparator output observed oscillation after trig event on the direct pas through output
- SumInt ADC react to the comparator by flip flop reset and the set is given by fixed time, so there s no risk that the oscillation influence its corresponding channel channel input
- There can be some risk that oscillation between LVDS comparator and internal FPGA flip flop could have some effect on cross-talk (later confirmed from measurement data)
- oscillations can be caused over power load pulse to the bank power supply

NanoXplore LVDS Pins Assessment



100 Ω pos. source Y, neg. by potentiometer M, out C sumintadc-char/lvds-check

NanoXplore LVDS Pins Assessment



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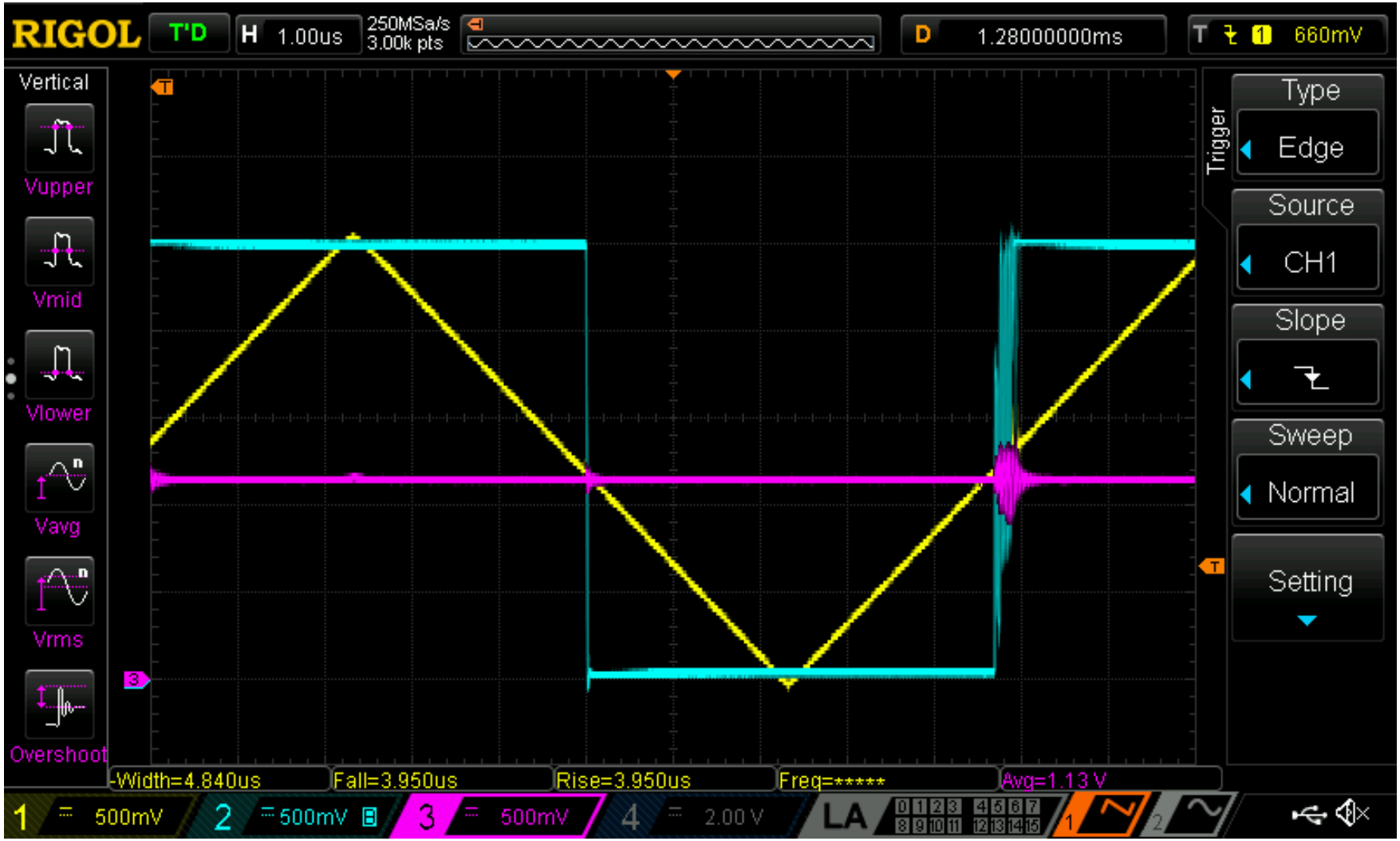
NanoXplore LVDS Pins Assessment



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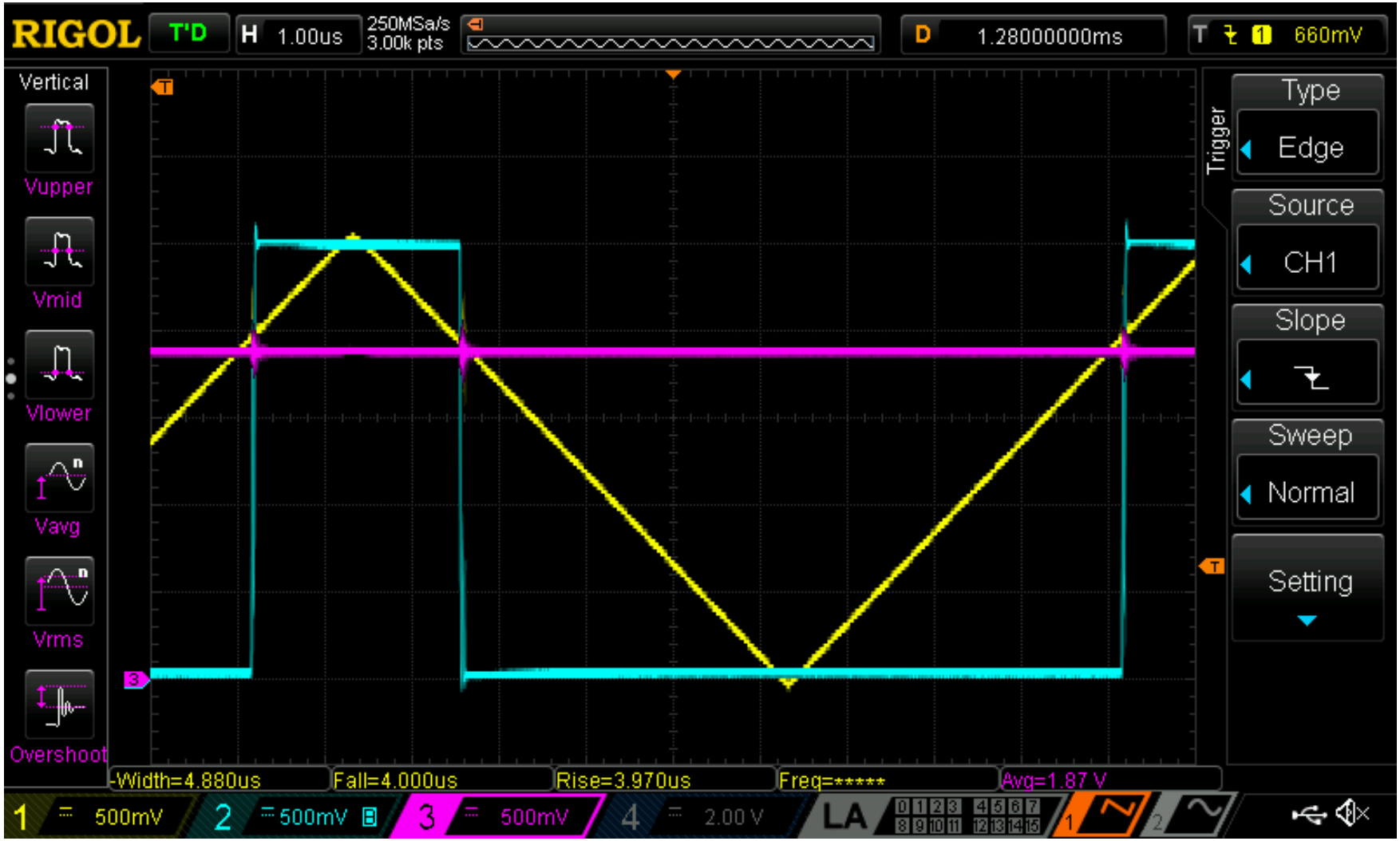
NanoXplore LVDS Pins Assesment



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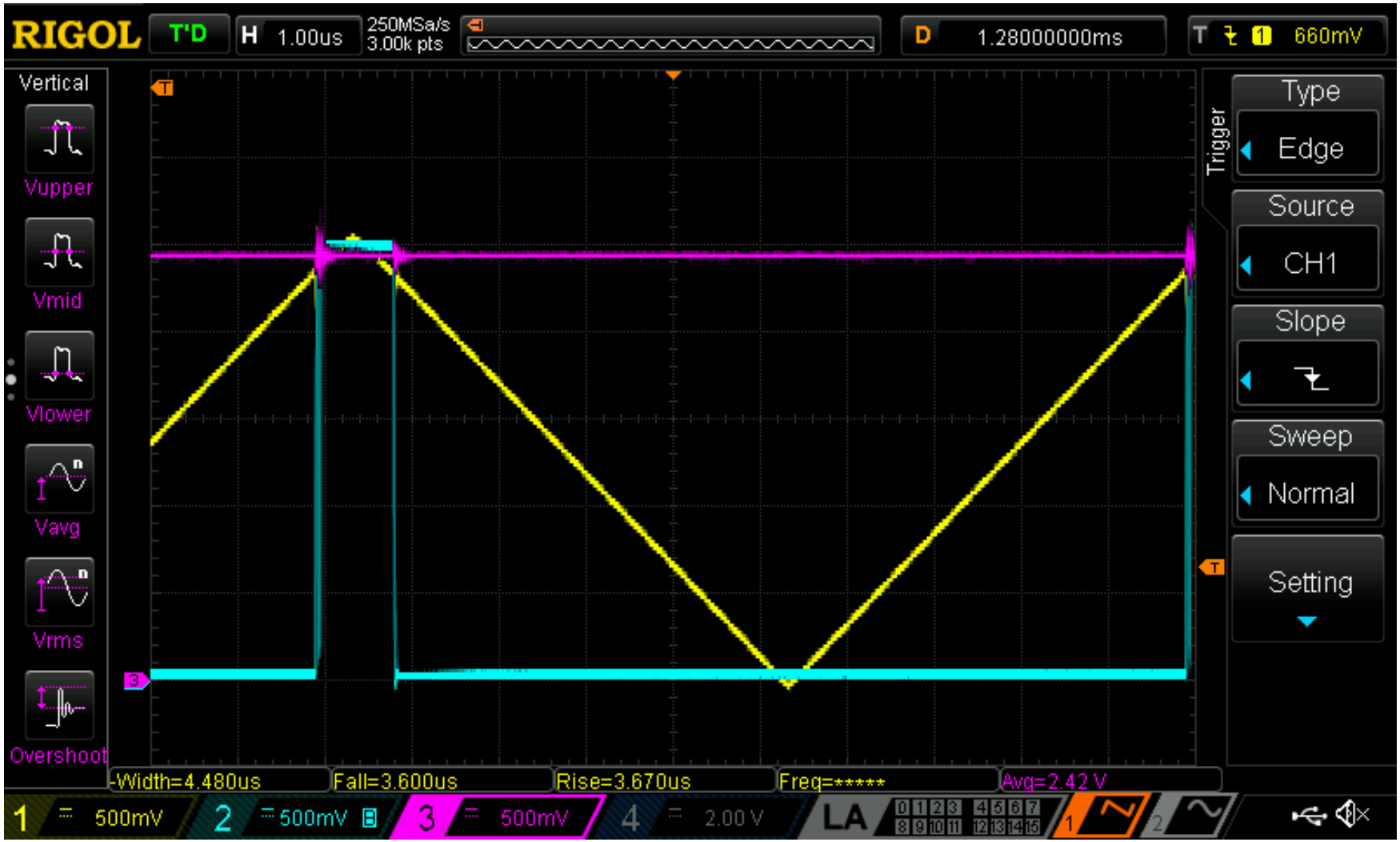

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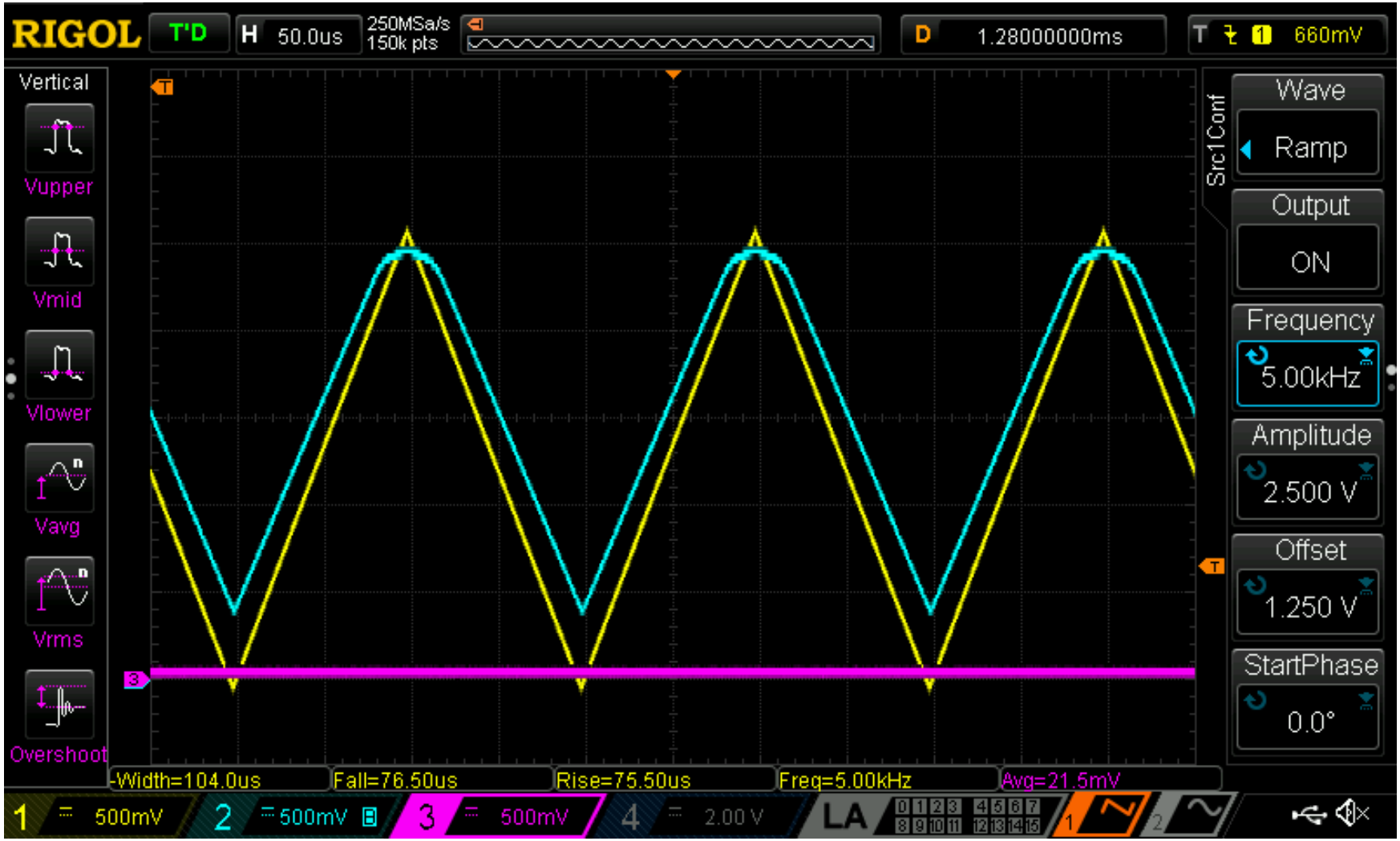
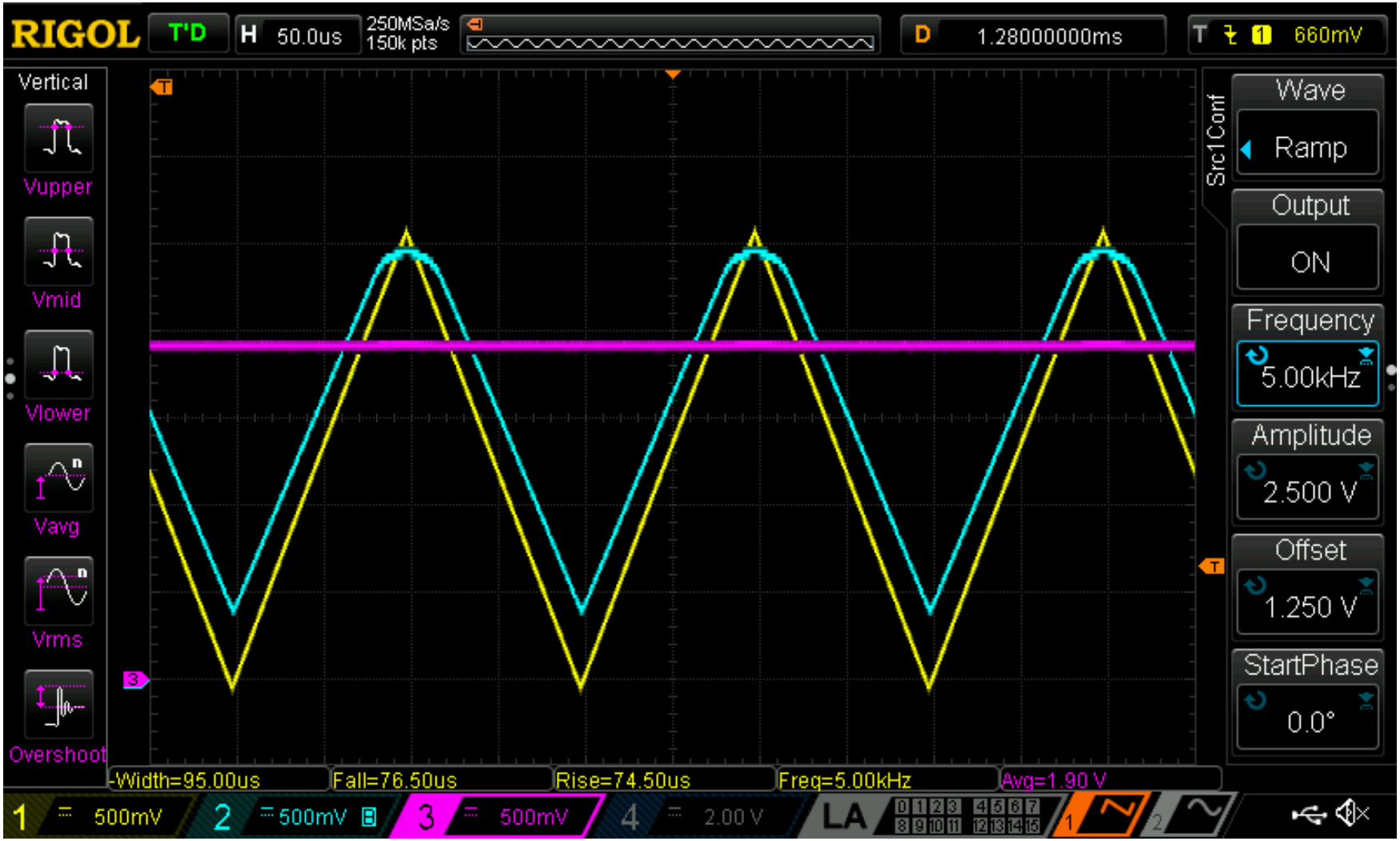


Y before, C after 10 kΩ pos. source, neg. by pot. M sumintadc-char/lvds-check

NanoXplore LVDS Pins Assessment



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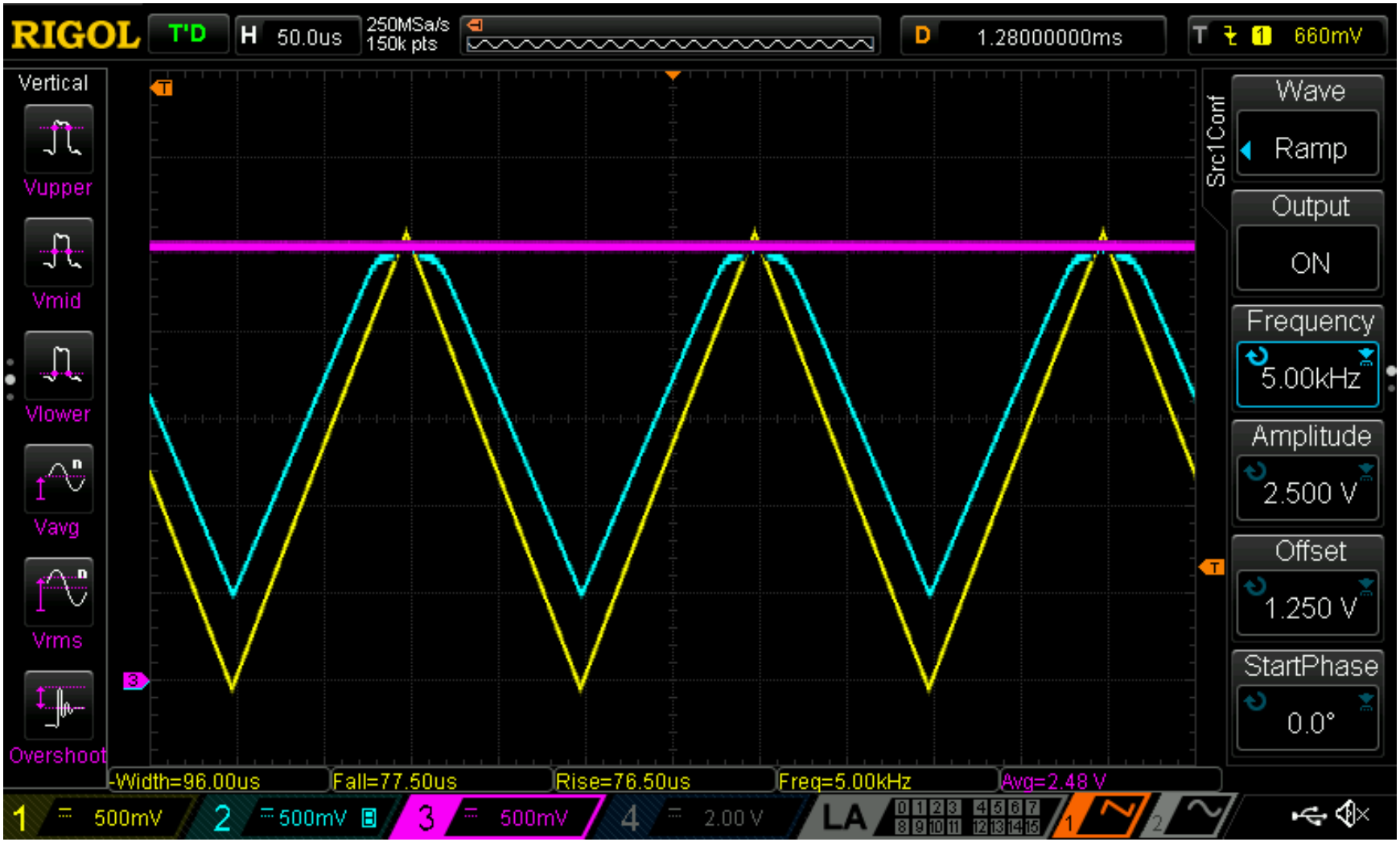

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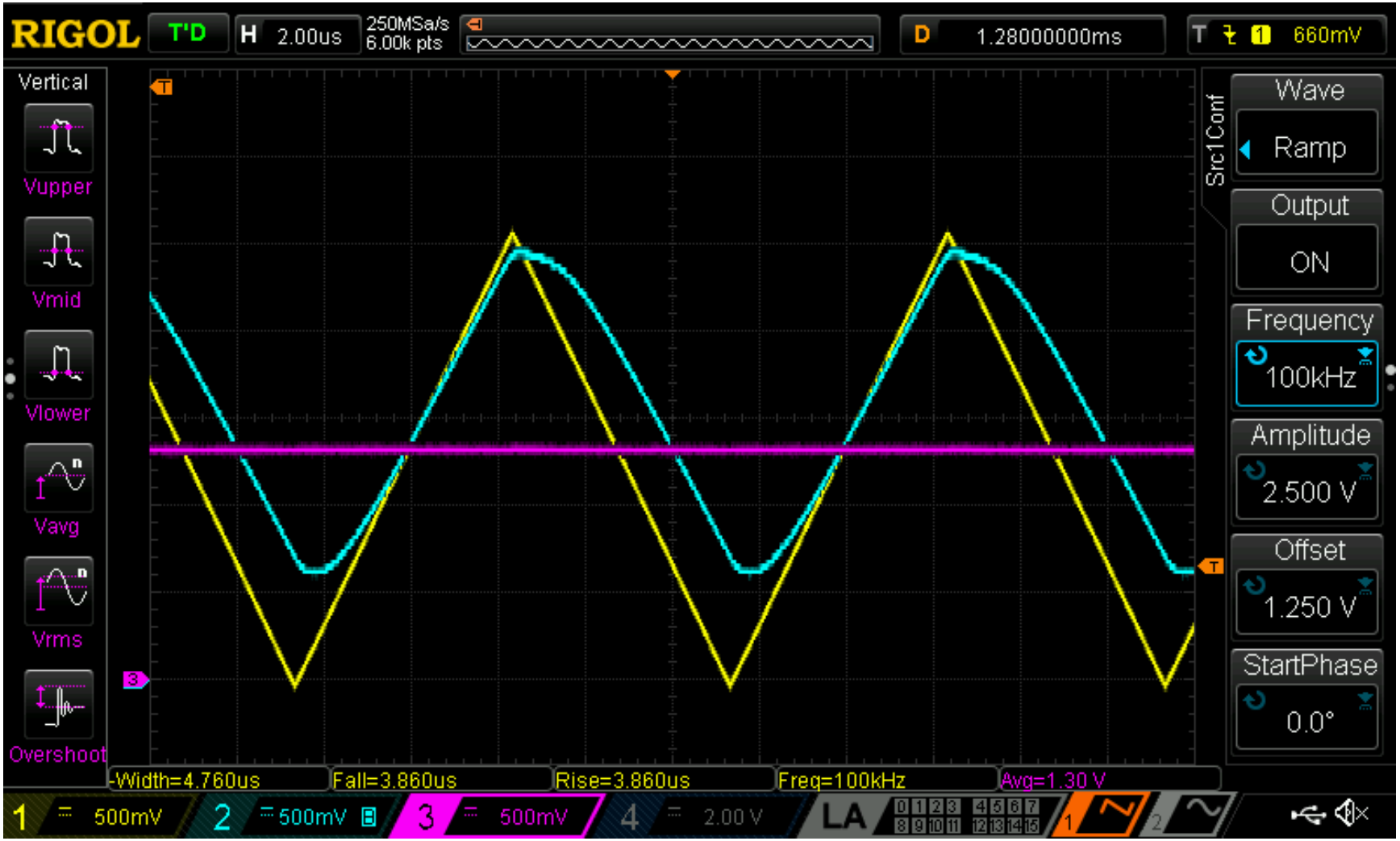
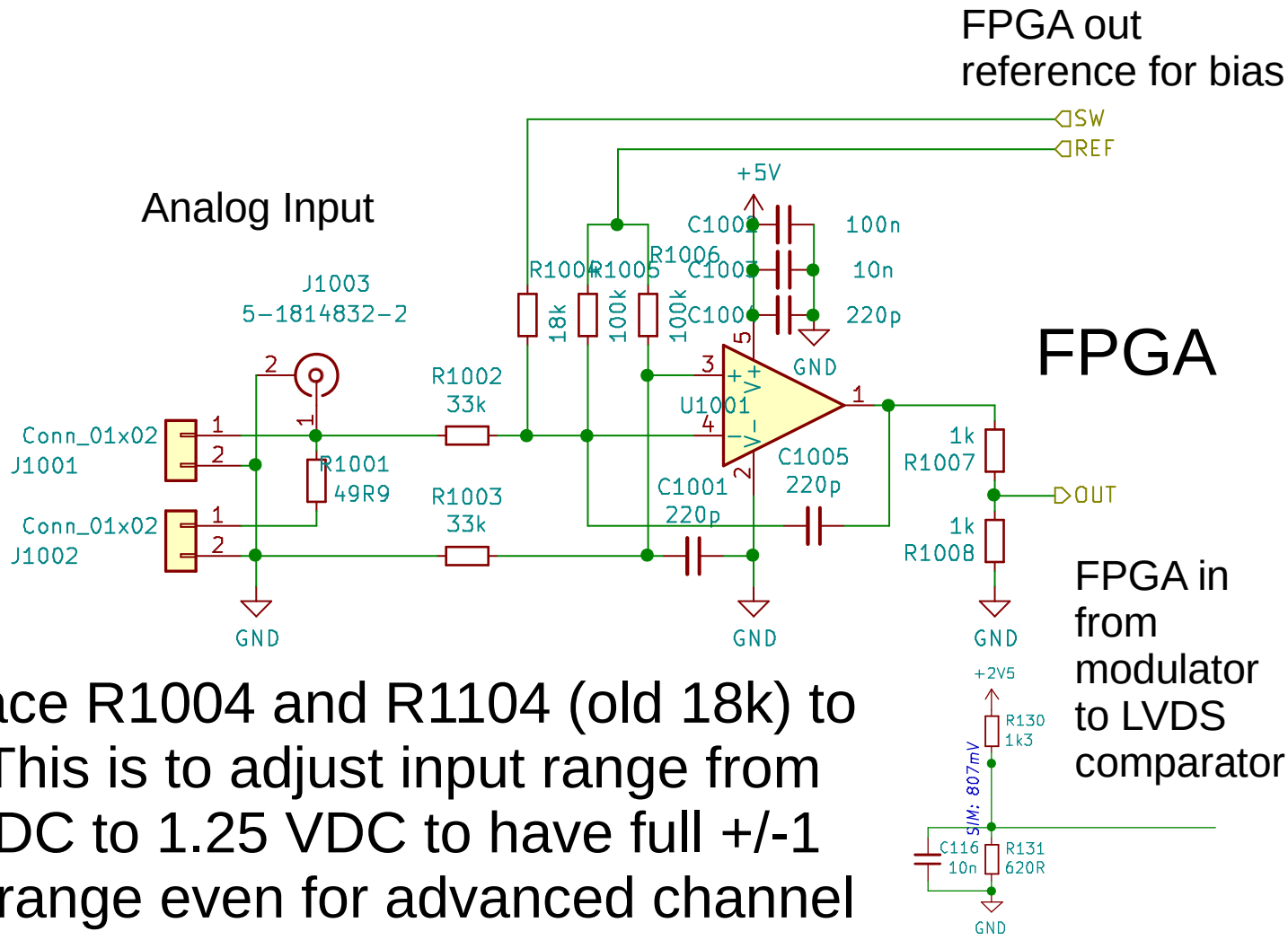


Y before, C after 10 kΩ pos. source, neg. by pot. M sumintadc-char/lvds-check

The Bread Board (v3) Simple Channel

- Simple Version of the A / D Converter with One OA and LVDS Used as Comparator
  - 2 channels
  - components
    - OA ADA4084-1 / ADA4084-2 / ADA4084-2S
  - 5 V powered from LM2940CS (initial idea 3.3 V powered from kit), power sequence should not be problem for input pins even when NX is unpowered
  - reference 2.5 V from bank power supply

The Simple Channel Schematics

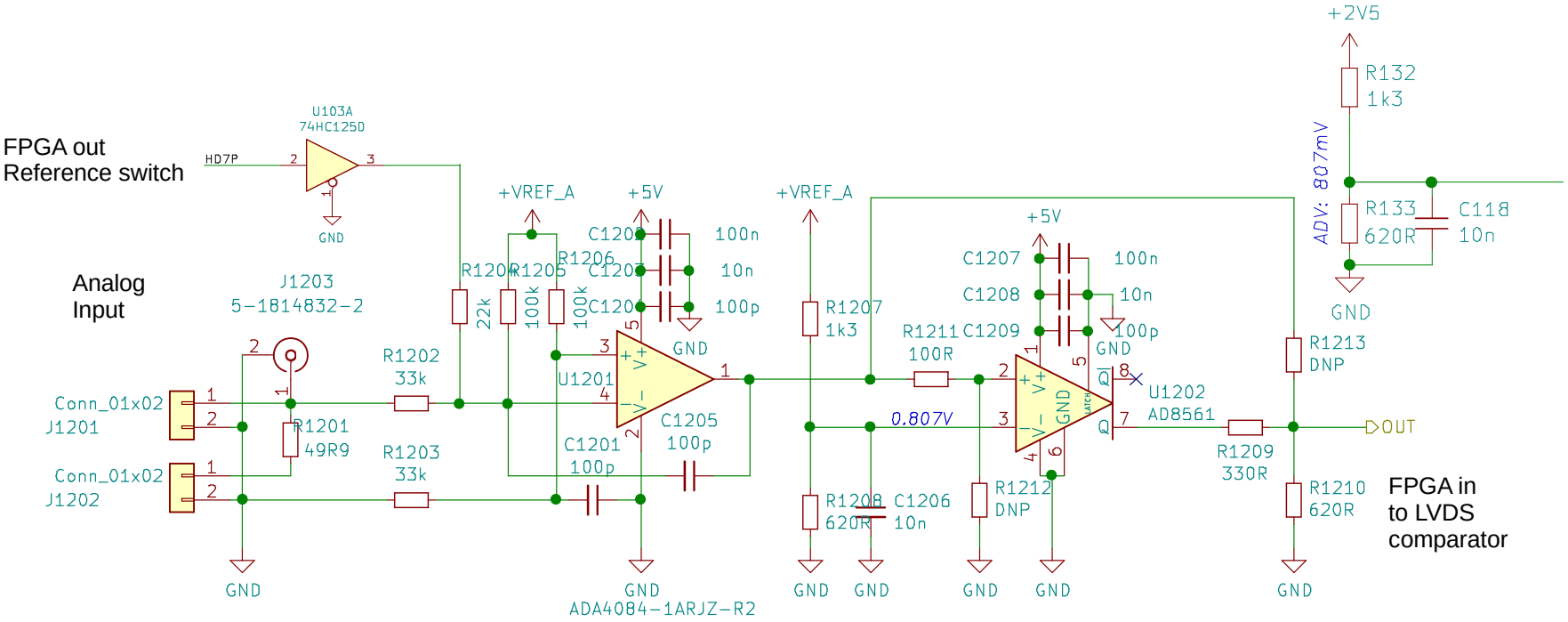


- Replace R1004 and R1104 (old 18k) to 15k. This is to adjust input range from 1.1 VDC to 1.25 VDC to have full +/-1 VDC range even for advanced channel version. (SIMPLE channel 1 and 2)

The Bread Board (v3) Advanced Chan.

- 5V Powered Version of the A / D Converter with External Comparator
  - 4 channels
  - components
    - integrator ADA4084-1 / ADA4084-2 / ADA4084-2S
    - comparator AD8561(S) - be aware that specification is defined for U_{cm} up to 3 V only
    - digital level shifters for reference switching or STM M54HC125/M54AC125 (but reference only up to 3.5 V)
    - reference 2.5 V REF43 SO8 (REF43S 10L CERPAC, ISL71090SEH25)
    - LM2940 TO263 (LM2940QML-SP) for power supply from kit 12V
  - integrator output optionally divided to fit in AD8561(S) 3 V common mode specification
  - other configurable option is to skip discrete compactor and use LVDS FPAG input directly
  - 5 V power supply, linear stabilization from 12 V from kit

Advanced Channel Schematics

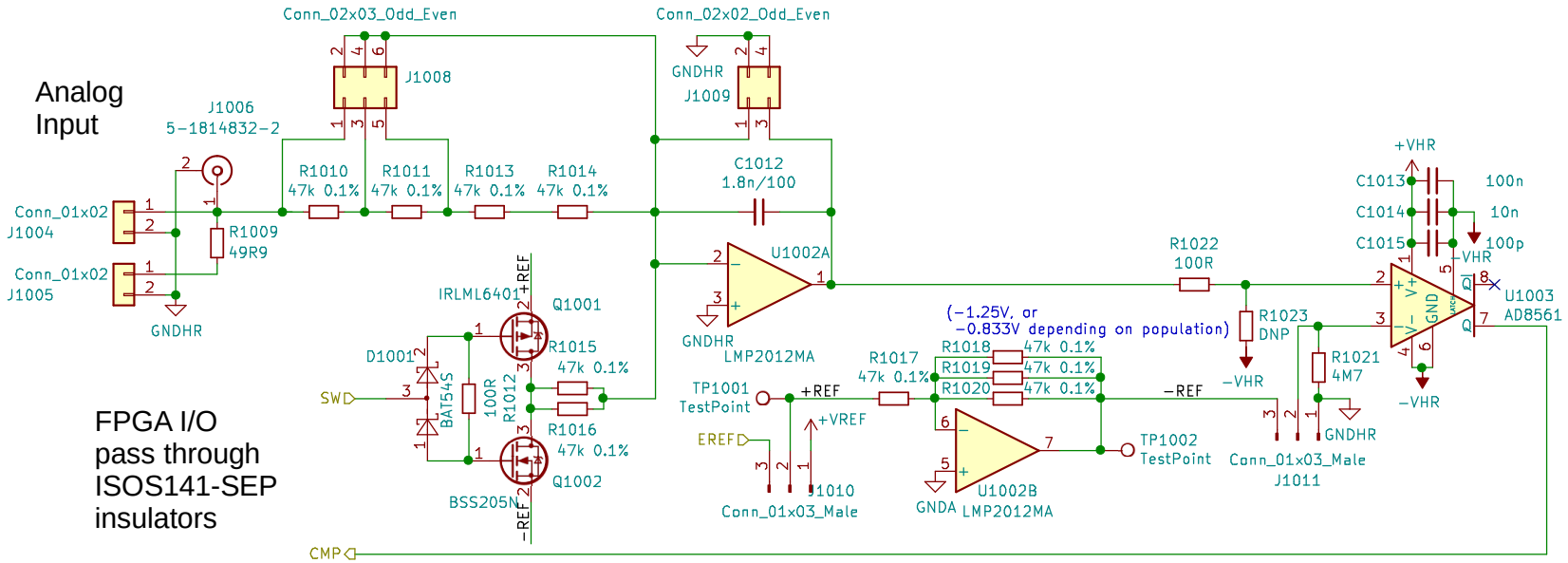


- Replace R204 and R1204 (old 22k) to 15k. This is to adjust input range from 0.9 VDC to 1.25 VDC to have full +/-1 VDC range even for advanced channel version. (ADVANCED channel 1 and 2)
- Replace C1205 (100 pF) to 220 pF to increase margin to slew rate 2.6 V/µs (change will be tested on ADVANCED channel 2)
- Replace C205 (100 pF) to 470 pF to increase margin to slew rate 2.6 V/µs (change will be tested on ADVANCED channel 1) (capture channel 2)

The BB (v3) High Resolution Chan.

- High Resolution Galvanic Isolated A / D Converter – 2 channels
- components
  - digital isolator ISOS141-SEP, powered by +/-2.5V, updated, due unclean LMP2012 specification at higher temperatures shifted to +3.0 V and -2.0 V
  - OA for reference negation and integrator should be chopper stabilized or "zero" offset, TI LMP2012MA SO8 (LMP2012QML-SP) seems to be good option
  - voltage reference REF43 SO8 (REF43S 10L CERPAC, ISL71090SEH25)
  - comparator AD8561(S) - be aware that specification is defined U_cm up to 3 V only
  - analog multiplexer/switch for reference by mosfet, Rdson < 120 mOhm @ 4.5 V, Vds > 6 V, minimal capacity STR2P3LLH6 (alternative STM M54HC125)
  - integrator capacitor 1.8nF (C0G/NP0 i.e. 12061A182FAT2A KYOCERA AVX)
- power supplies, not space qualified
- reference 2.5 V negated to -1.25 by LMP2012, Ra = 47kOhm, direct Ra, feedback Ra/2 (two parallel Ra)
- reference switching by two MOSFETs, N type from from -1.25V and P type one from +2.5V, both through common Ra/2, prevent current shot-through by resistor and Schottky diodes
- output comparator selectable against AGND or -1.25 V

High Resolution Channel Schematics

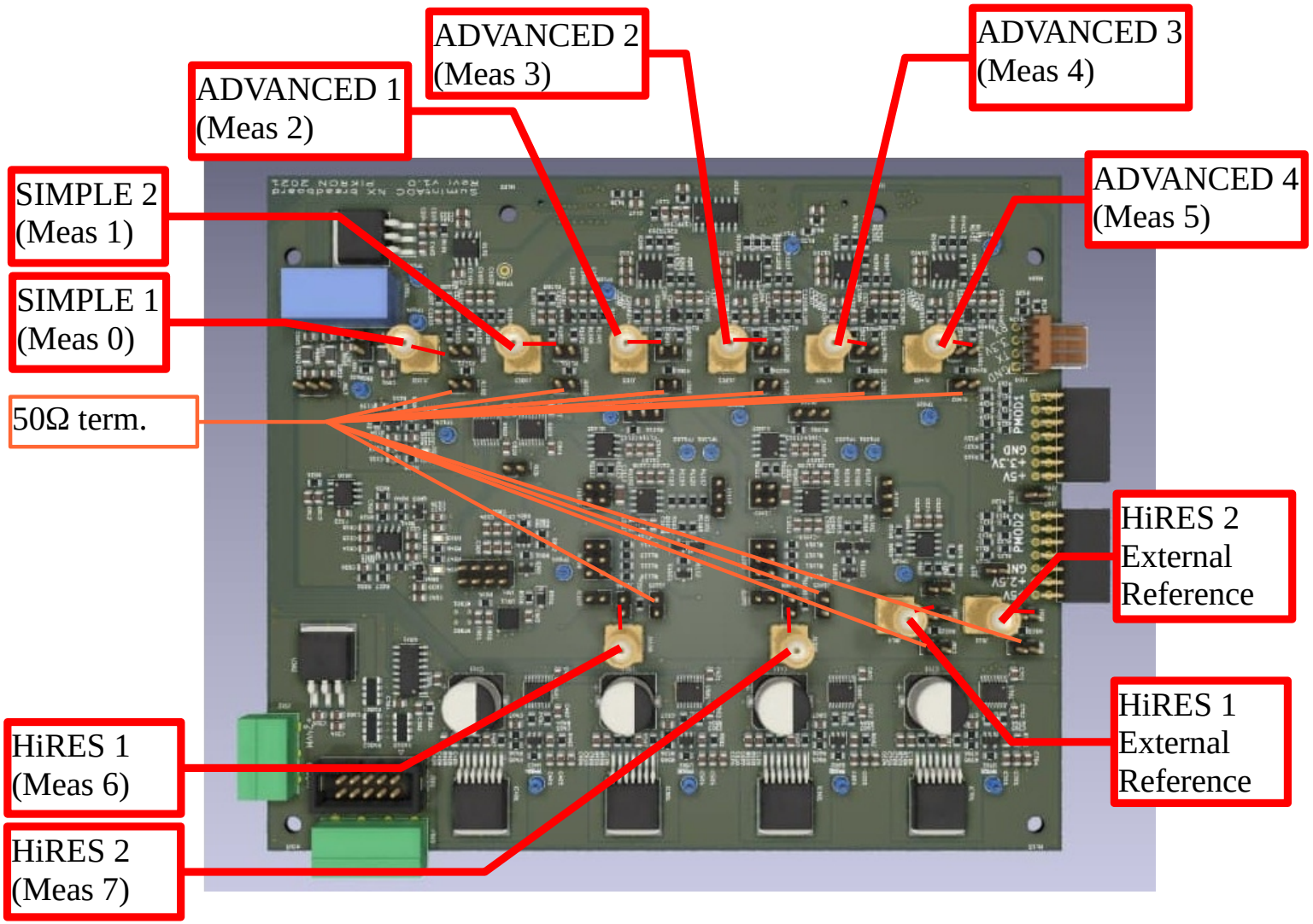


- Replace Q1001 and Q1101 (schematics IRML6401) replaced by Alpha&Omega AO3421E
- Replace C1112 (old 1.8 nF) to 4.7 nF to increase margin to slew rate of LMP2012MA V/µs (HiRes channel 1)

More Design Simulations and Updates

- Power supplies planned but simulation left after submitting to the production
- Prepared by Jakub Ladman, simulation LTSpice
- Inspection and tuning OMICRON Lab Bode 100 Vector Network Analyzer + Picotest J2111A Current Injector
- Remove R102, the 2.5 V from reference should be buffered in 1:1 ratio to 2.5 V rail
- Replace R103 (old 220k) to 2M2 to enhance stability 2.5 VDC supply for isolators and reference LVDS inputs
- Output of operational amplifiers U1102B and U1002B (LPMP2012MA) is blocked by serial combination 10uF+2R2 to the ground.
- Output of U806 (REF43S) is blocked by 3x 47uF to ground. One directly parallel to C822 other on input 1 of jumpers J1010 and J1110.
- Replaced R839 (old 4M7) to 1M0
- Replaced R838 (old 220k) to 470k
- Replaced C829 and C830 (old 100pF and 47pF) to 220pF.

SumIntADC BreadBoard v3 Model



Reasons to Choose Professional Lab

- The setup integration with measurement instruments orchestration required more time, initial negotiated two days for characterization at ESA lab unrealistic and equivalent price of two or three ESA personnel work for one month work would be probably above whole SumInt ADC contract budget
- ESA requested full temperature range, 1000+ points and sweep in both directions. This enlarges earch run time. Number of the long series reduced.
- The work on connection of the board to already prepared setup started at 2022-01-23 and the last samples series was acquired at 2022-02-21 (over 100 hours of the instruments time in actual acquisitions, trial runs and personnel time not recorded in **measurements-diarry**)

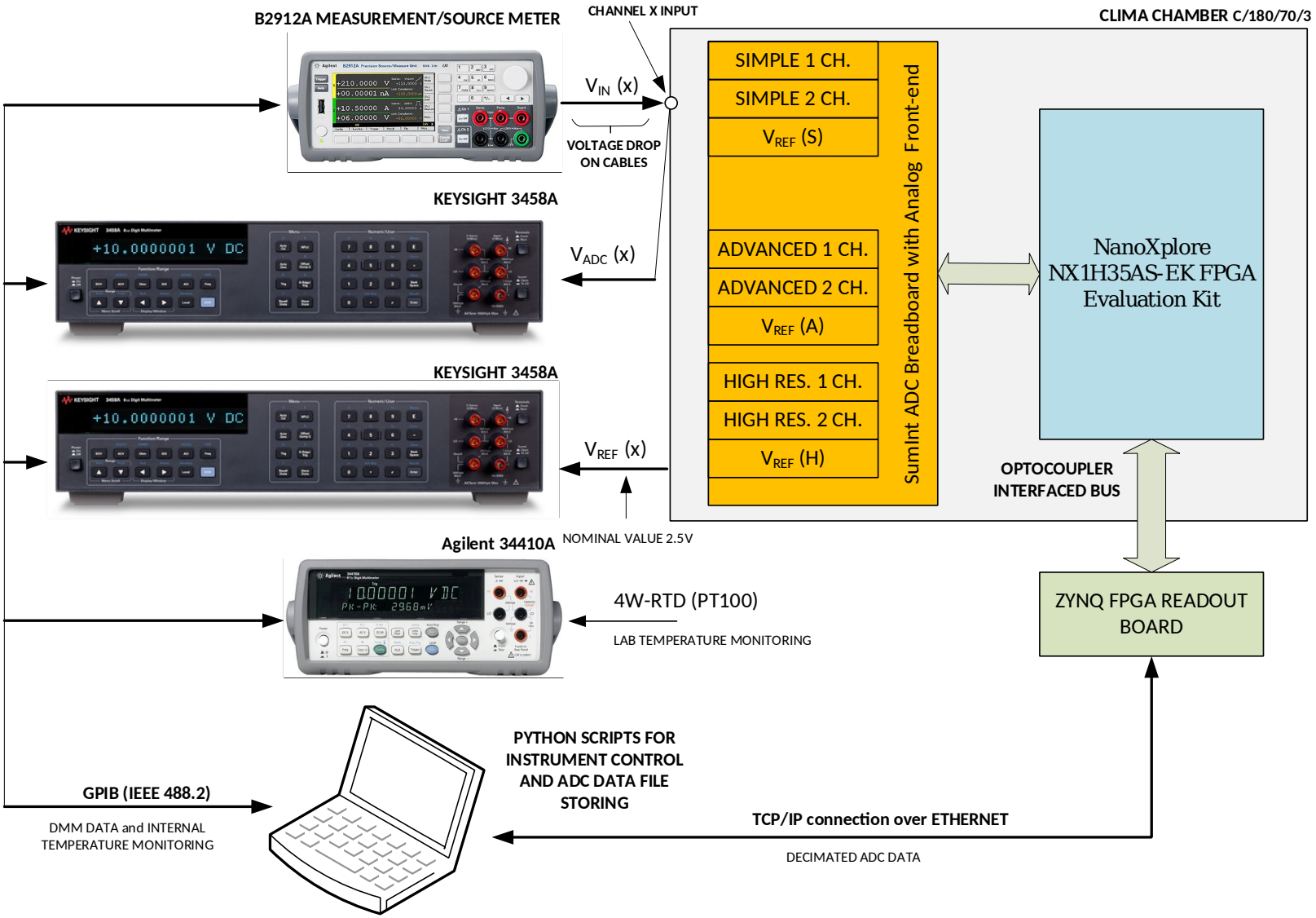
Laboratory of precise electrical measurement

- Department of Measurement
- Faculty of Electrical Engineering
- Czech Technical University in Prague
- Ing. Radek Sedláček, Ph.D.
- Doc. Ing. Josef Vedral, Csc.
- Ing. Michal Špaček
- https://meas.fel.cvut.cz/research/metlab

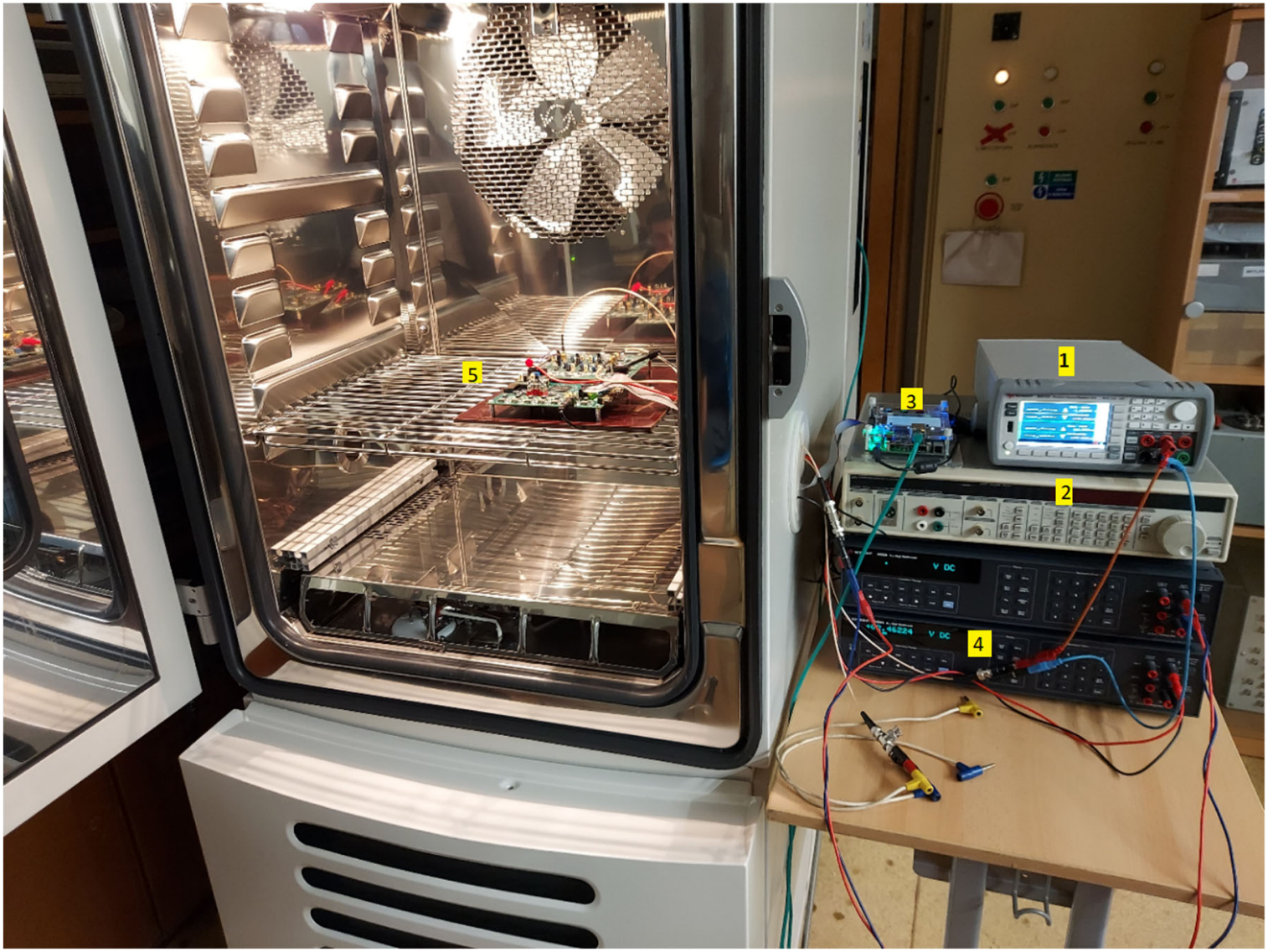
Static Characteristics

- Used method: direct comparison of the tested A/D converter with the reference voltmeter Keysight 3458A
- Measurement of the conversion characteristic (including the reference voltage of the converter) at 1101 points (~1 s/measurements – 3495 SumInt 4 kHz samples, three independent acquisitions for each point, sweep up and down, full range -1.1 to +1.1 VDC, nominal -1.0 tp +1.0 VDC → 1 µV step). For comparisons SumInt ADC calibrated by 25°C curve.
- Keysight B2912A source meter / measurement unit used as a source of testing voltage
- the tested A/D converters was placed in a climate chamber ClimaEvent C/180/70/3
- conversion characteristic measured in 5 temperature points (-40 ° C, 0° C, 25 °C, 40 °C, 85 °C)

Static Characterization Setup



Clima Chamber, Keysight 3458A …

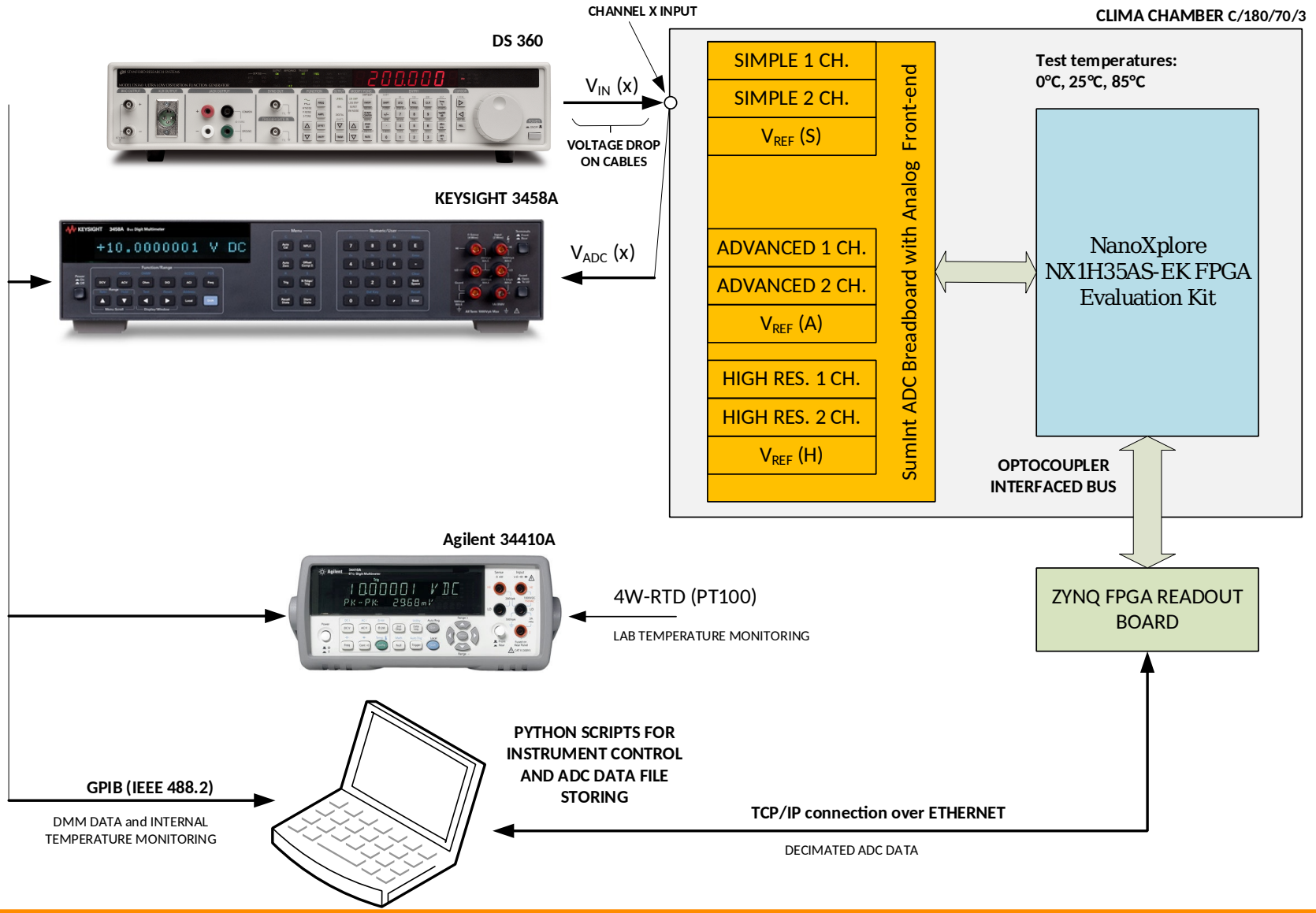


Dynamic Characteristics

- Used method: excitation of the A/D converter input by a harmonic signal at a given frequency and with a constant amplitude close to the full range.

  Tasks and equipment:
- perform "sinewave fit test" - interpolation of measured values by an ideal sine wave – as digitizer will be used Keysight 3458A
- calculation of SINAD, ENOB parameters for each frequency at the full range of the converter
- type of used generator: Stanford Research Systems DS 360 (THD <100 dBc for f < 20 kHz)
- frequency points for dynamic testing: 10 Hz, 15 Hz, 22 Hz, 33 Hz, 47 Hz, 68 Hz, 100 Hz, 150 Hz, 220 Hz, 330 Hz, 470 Hz, 680 Hz, 1000 Hz, 1500 Hz, data for each frequency captured three times
- data processing – evaluation all key parameters (SINAD, ENOB)

Dynamic Characterization Setup



Main/Presented Acquisition Series (1)

Test #	Type	HW rev	Meas Ch	Blind Ch	Start	Stop
1	static (DC)	0	simple 1 (0)	simple 2 (1)	22-02-02 9:43	22-02-04 4:41
	sumintadc-char/220203/ch0_signal_ch1_blind					
2	static (DC)	0	advanced 2 (3)	advanced 1 (2)	22-02-04 16:42	22-02-05 21:42
	sumintadc-char/220205/ch3_signal_ch2_blind					
3	static (DC)	0	hi-res 1 (6)	hi-res 2 (7)	22-02-14 18:37	22=02-14 22:02
	sumintadc-char/220214/ch6_signal_ch7_blind					
4	dynamic (AC)	0	simple 1 (0)	simple 2 (1)	22-02-18 12:40	22-02-18 13:31
	sumintadc-char/220219/dynamic_channel0_blind_channel1					
5	dynamic (AC)	0	advanced 2 (3)	advanced 1 (2)	22-02-18 14:30	22-02-18 15:20
	sumintadc-char/220219/dynamic_channel3_blind_channel2					
6	static (DC)	1	all		22-02-18 16:47	22-02-18 19:31
	sumintadc-char/220219/bb-069100108597-ch012345					
7	static (DC)	1	hi-res 1 (6)	hi-res 2 (7)	22-02-21 14:56	22-02-21 15:25
	sumintadc-char/220221/bb-069100108597-ch6_blind_ch7-1n8					
8	static (DC)	2	hi-res 1 (6)	hi-res 2 (7)	22-02021 18:25	22-02-21 21:31
	sumintadc-char/220221/bb-069100108597-ch6_blind_ch7-10n					

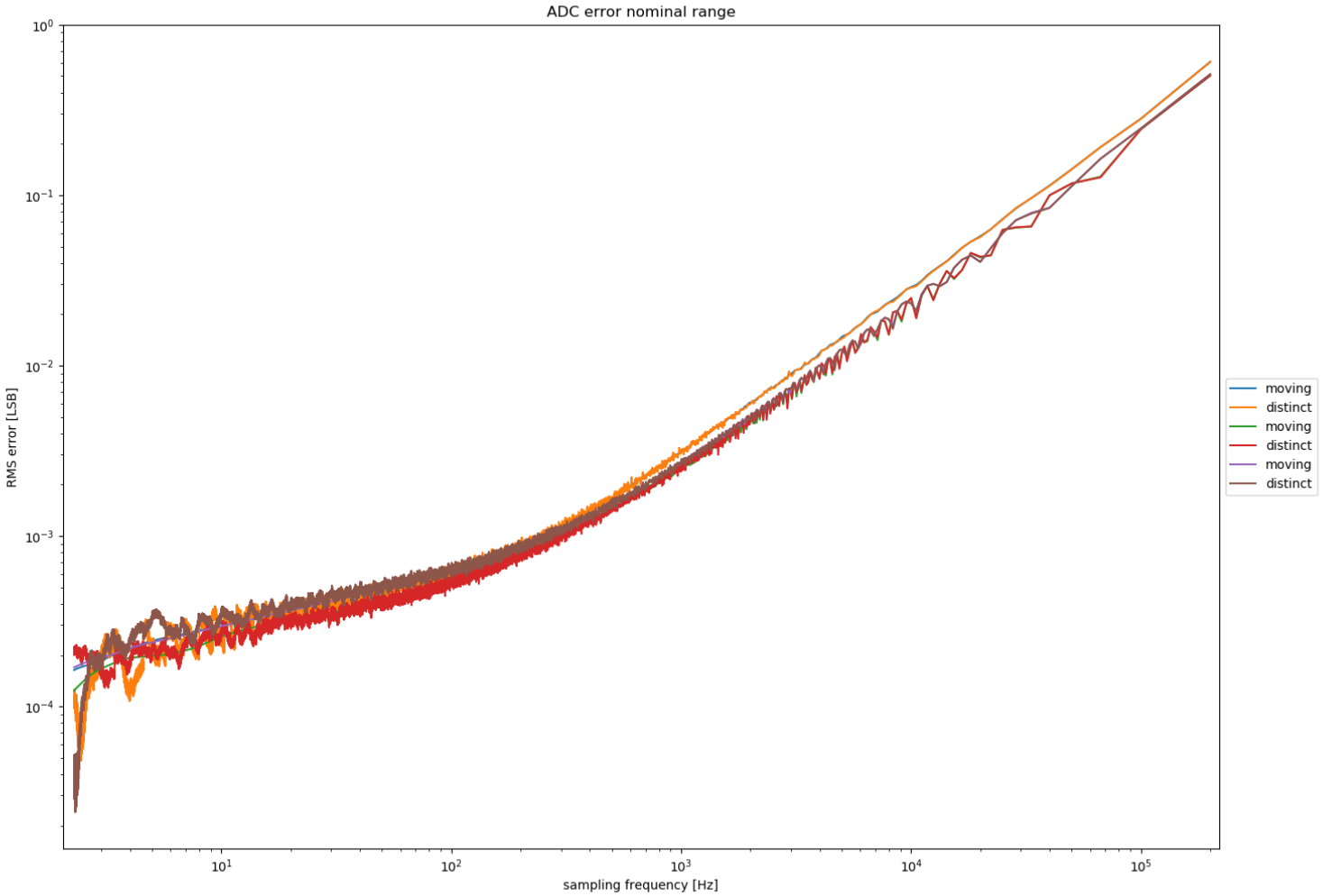
HW Revisions Remarks

- HW rev.0 – SumInt ADC AFE breadboard, S/N: EVERMAX 0020 0010 8595
- HW rev.1 – SumInt ADC AFE breadboard, S/N: EVERMAX 00691 0010 8597 (used OPA140 in case of ADVANCED 1 (acquisition channel 2))
- HW rev.2 – SumInt ADC AFE breadboard, S/N: EVERMAX 00691 0010 8597 (used a new value feedback capacitor for integrator)

When OPA140 in proper packages obtained later

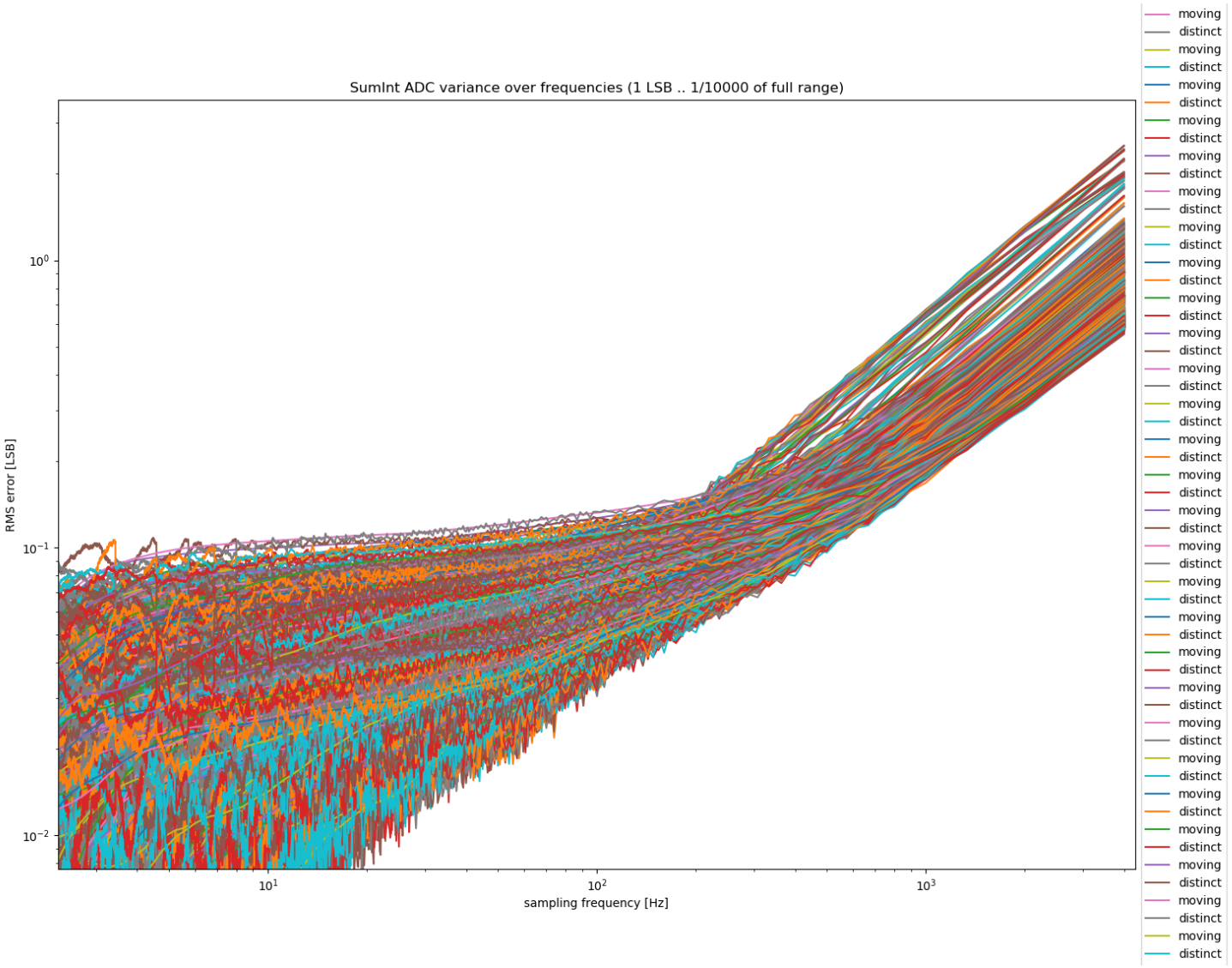
- HW rev.3 – SumInt ADC AFE breadboard, S/N: EVERMAX 00449 0010 8596 (Simple and Advanced channels with OPA140 – varied RC network for test)

Growth of Resolution with Averaging

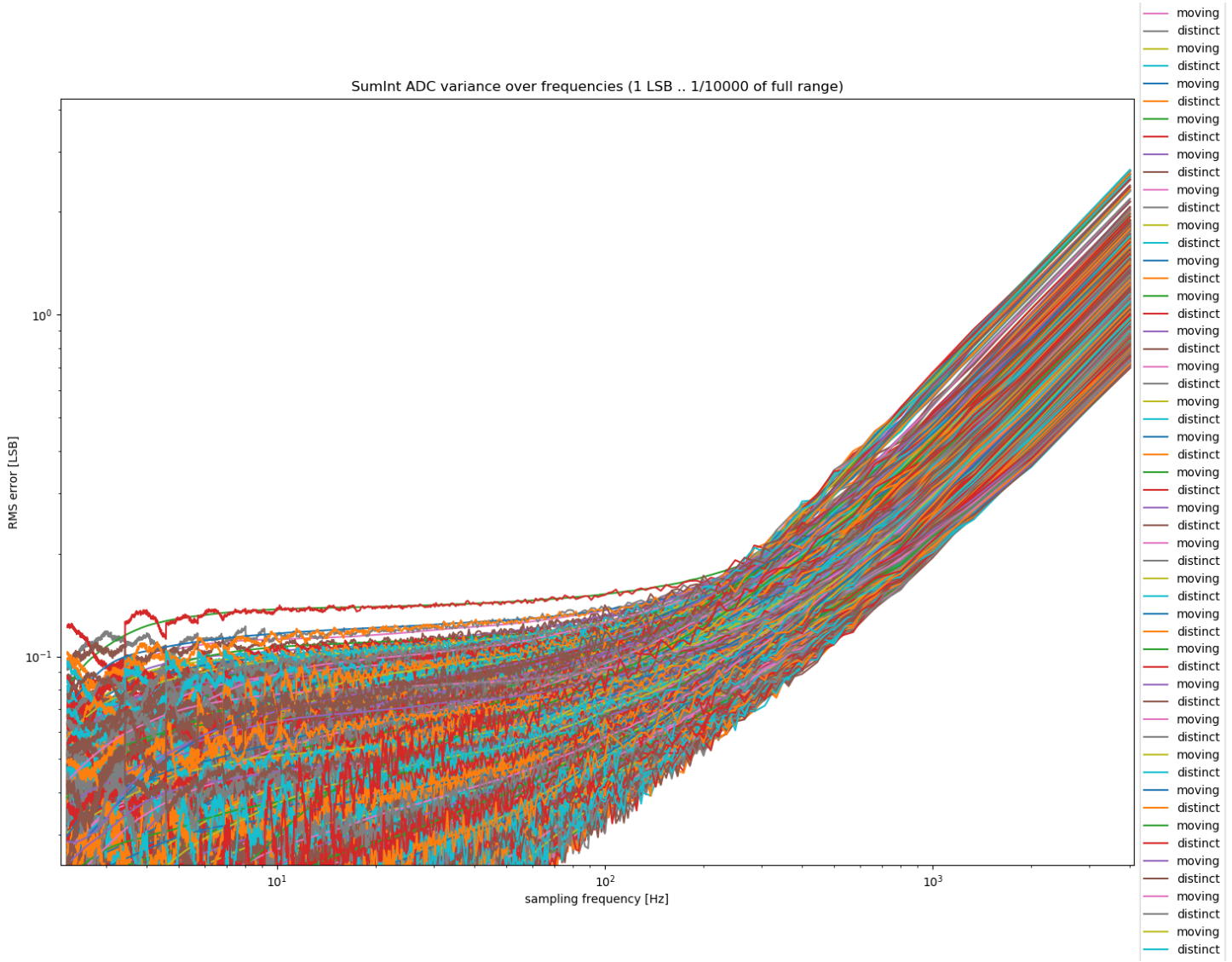


Demonstration of the linear growth of resolution from 200 kHz till 1 kHz

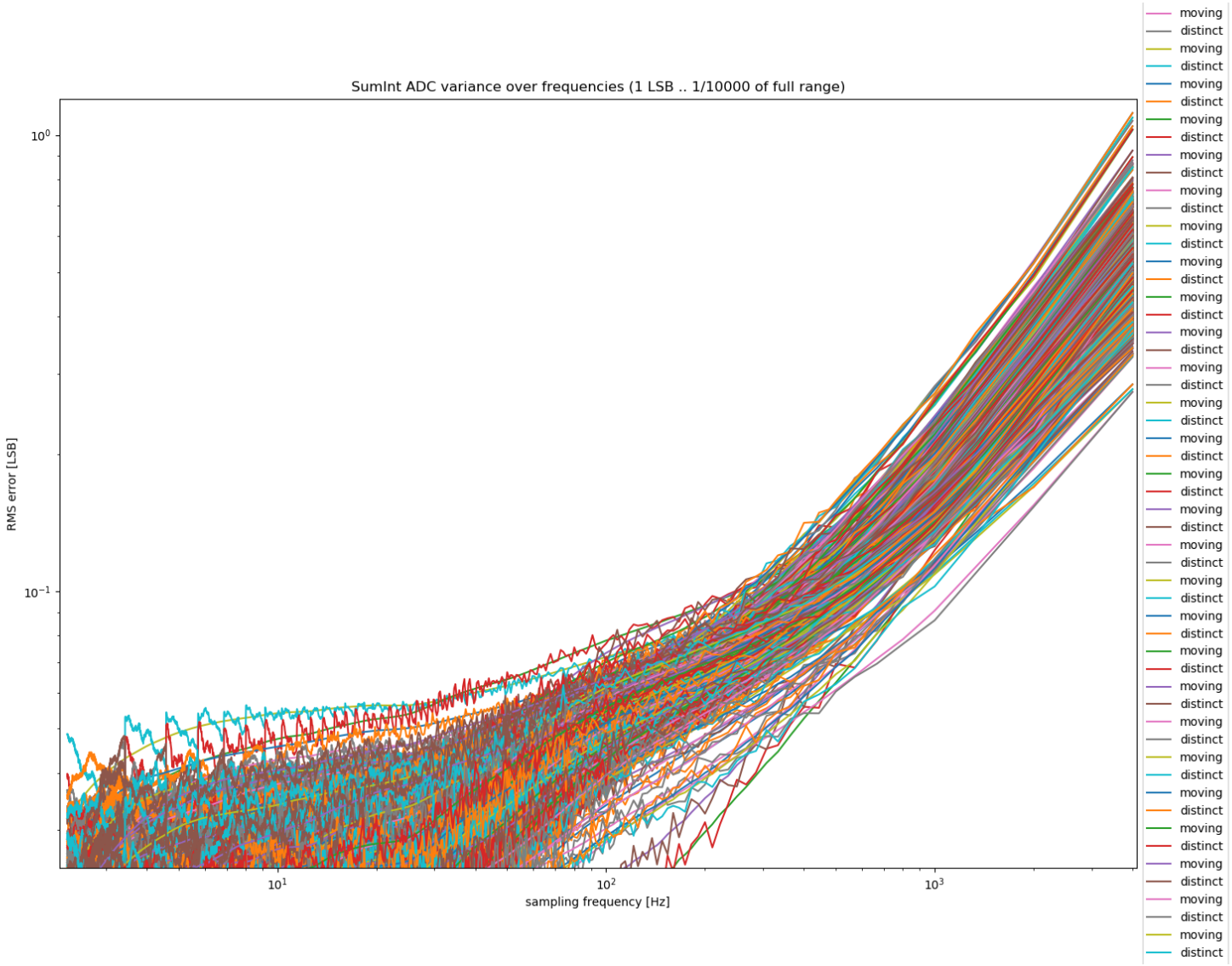
Simple 1 at -40°C, All 3k of 3k4 Series



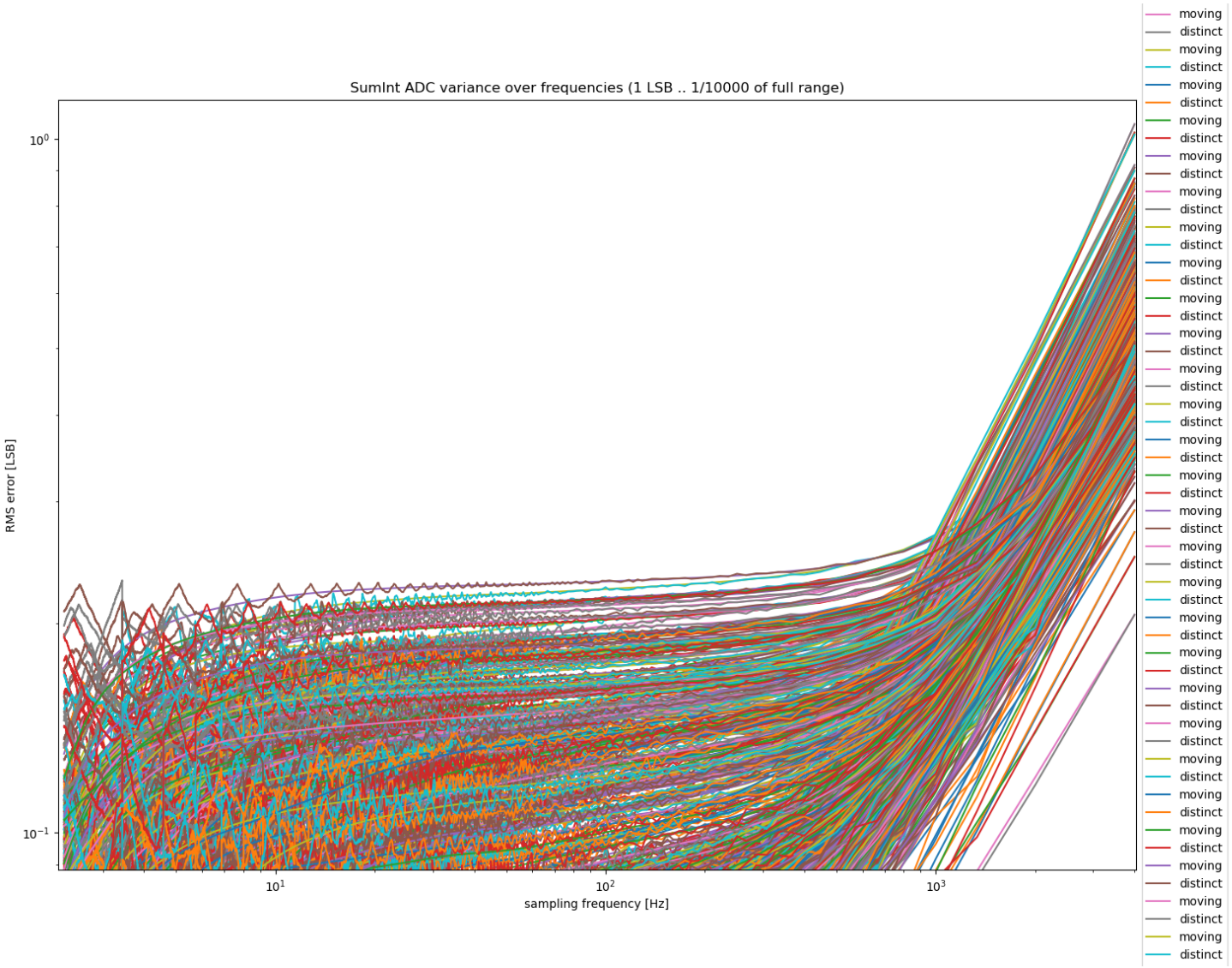
Simple 1 at 85°C, All 3k of 3k4 Series



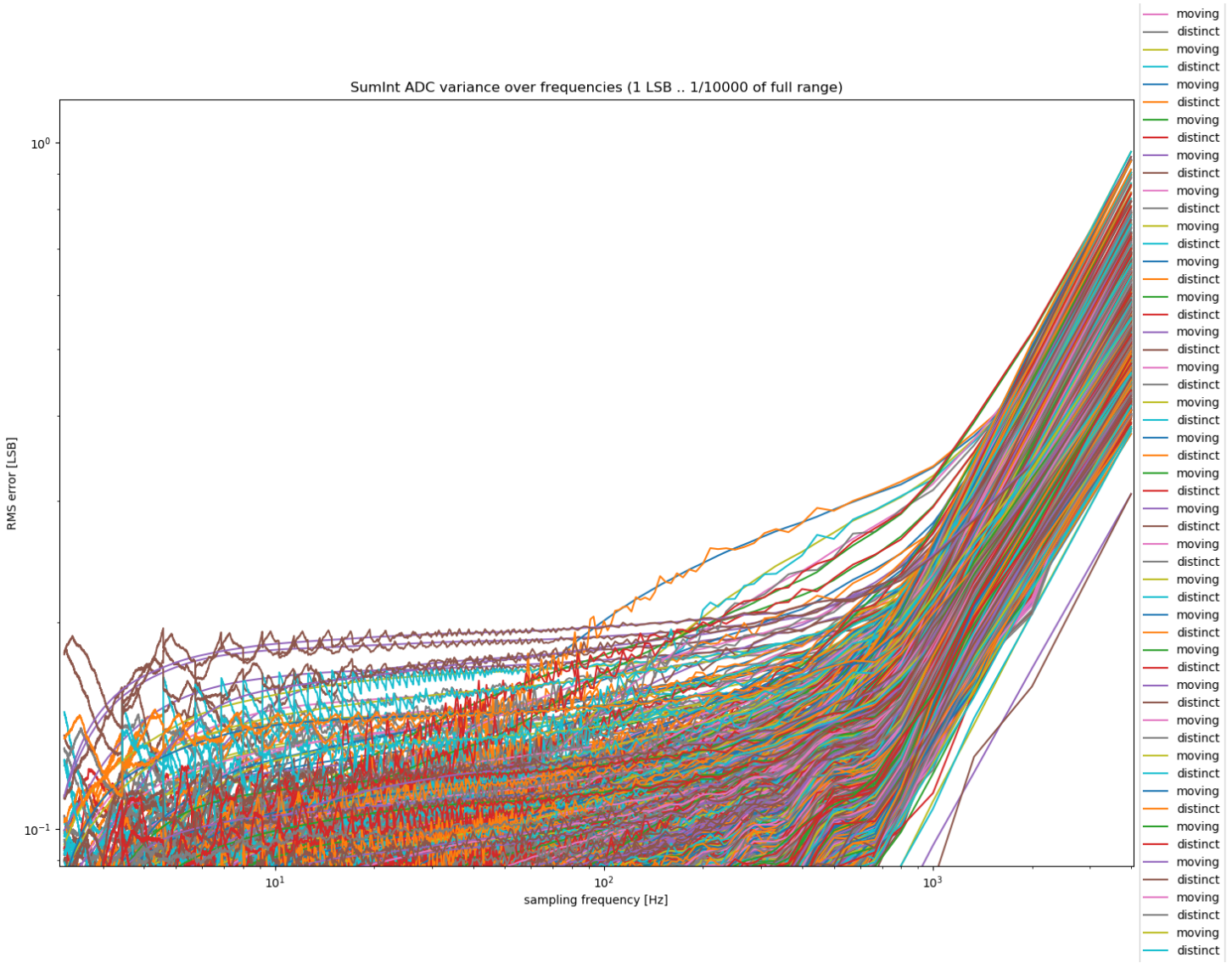
Advanced 2 at -40°C, All 3k of 3k4 Ser.



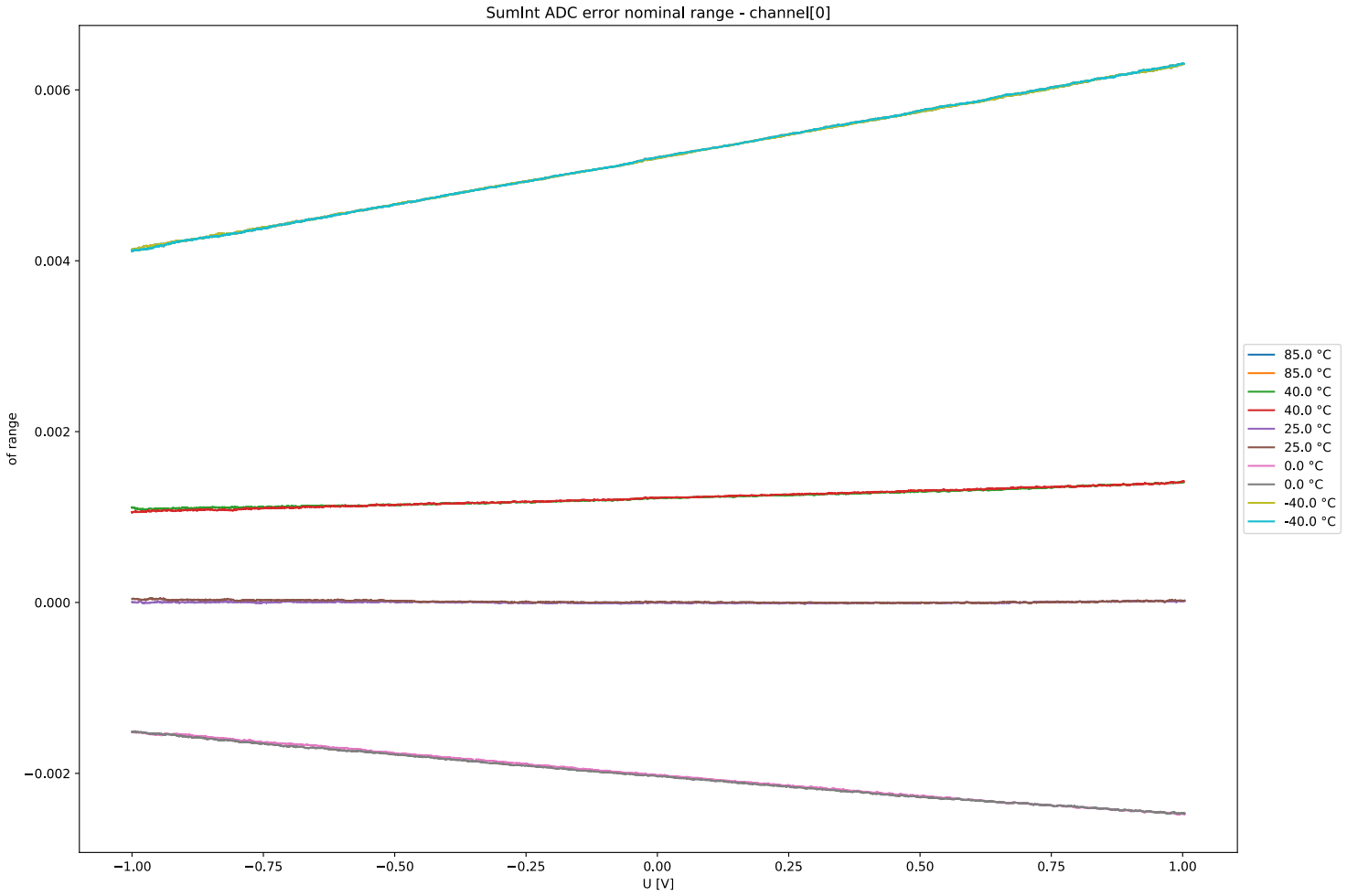
Advanced 2 at 25°C, All 3k of 3k4 Ser.



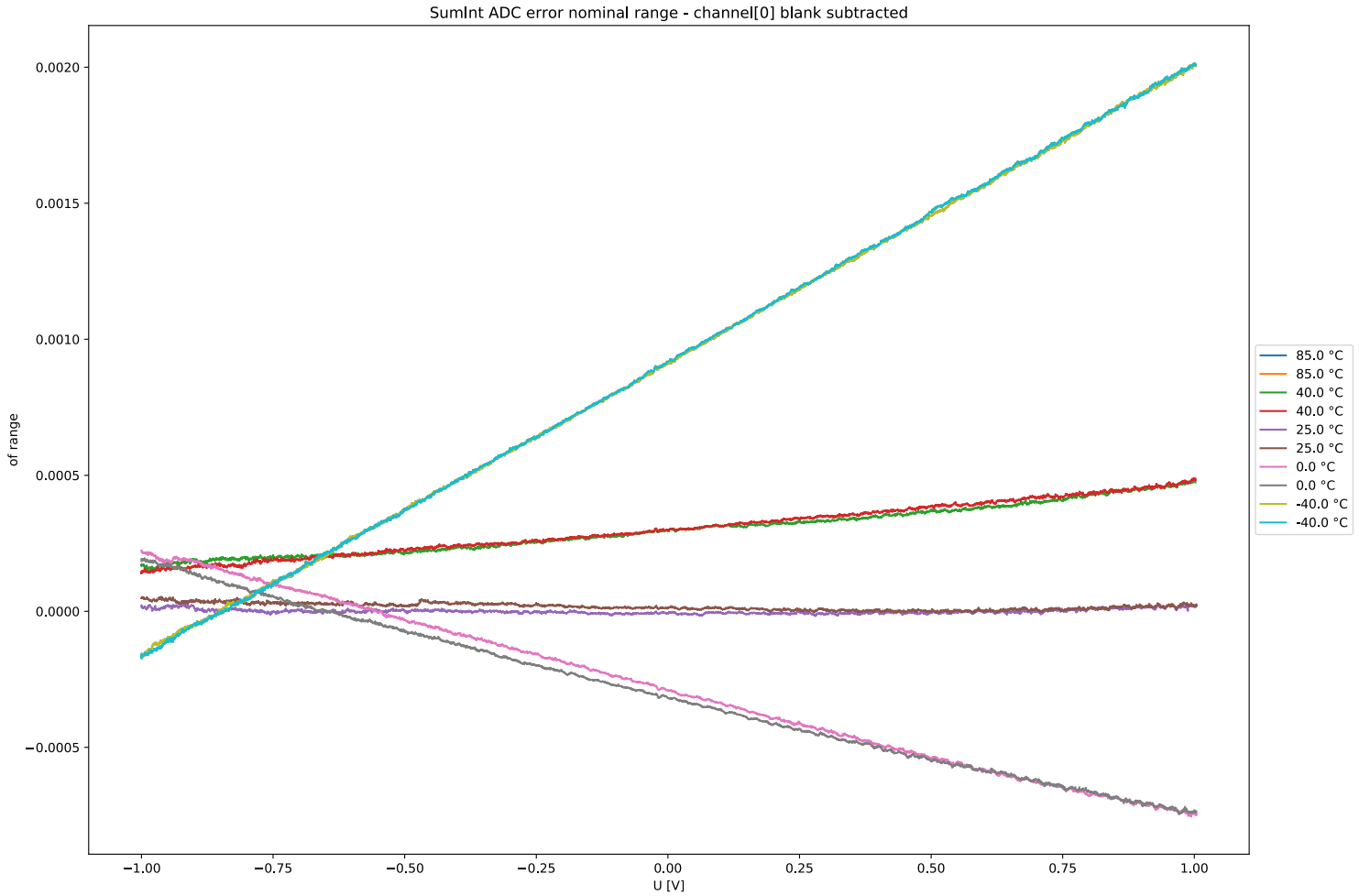
Advanced 2 at 85°C, All 3k of 3k4 Ser.



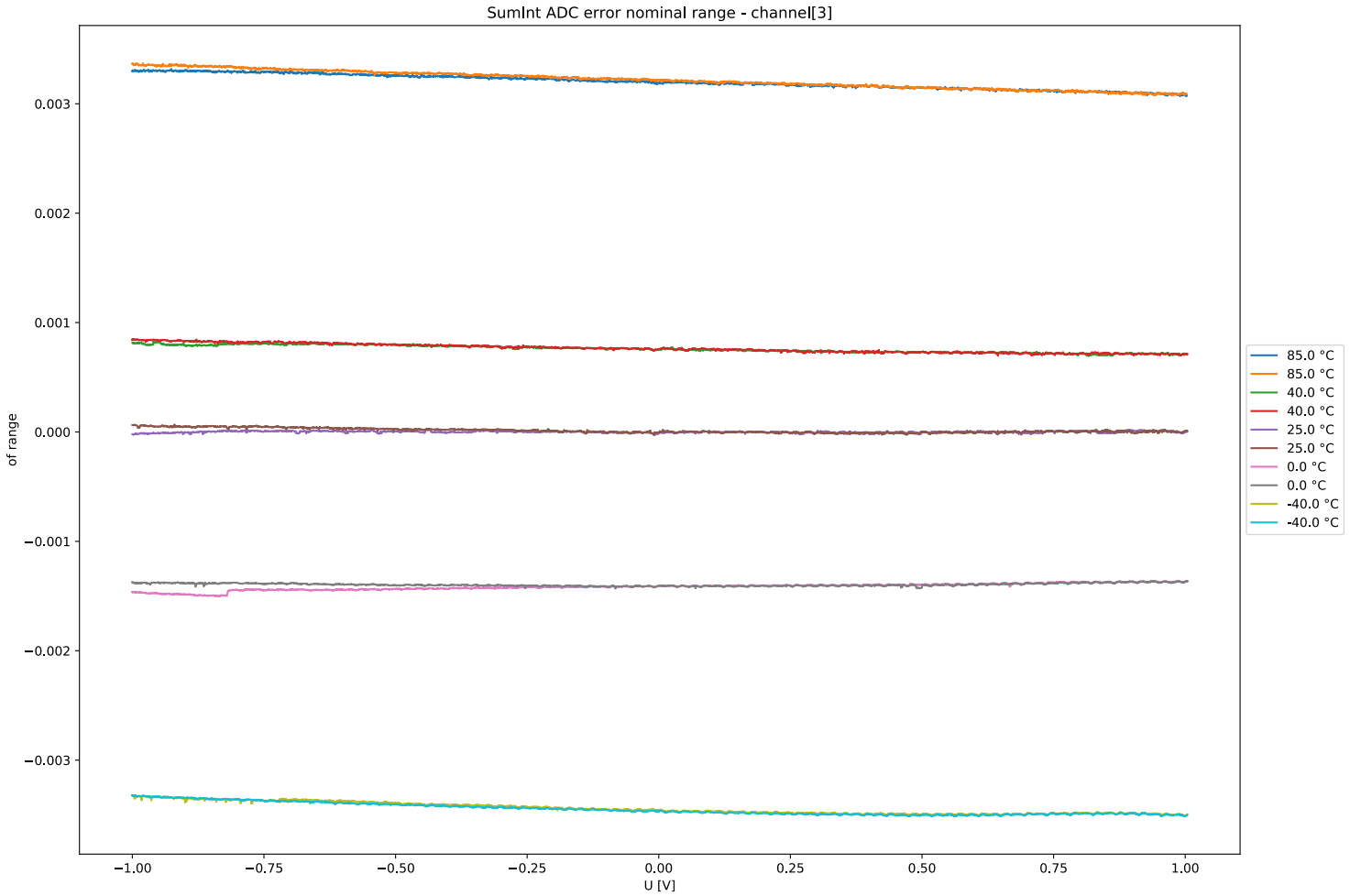
Simple 1 (0) Error -40°C to 85°C



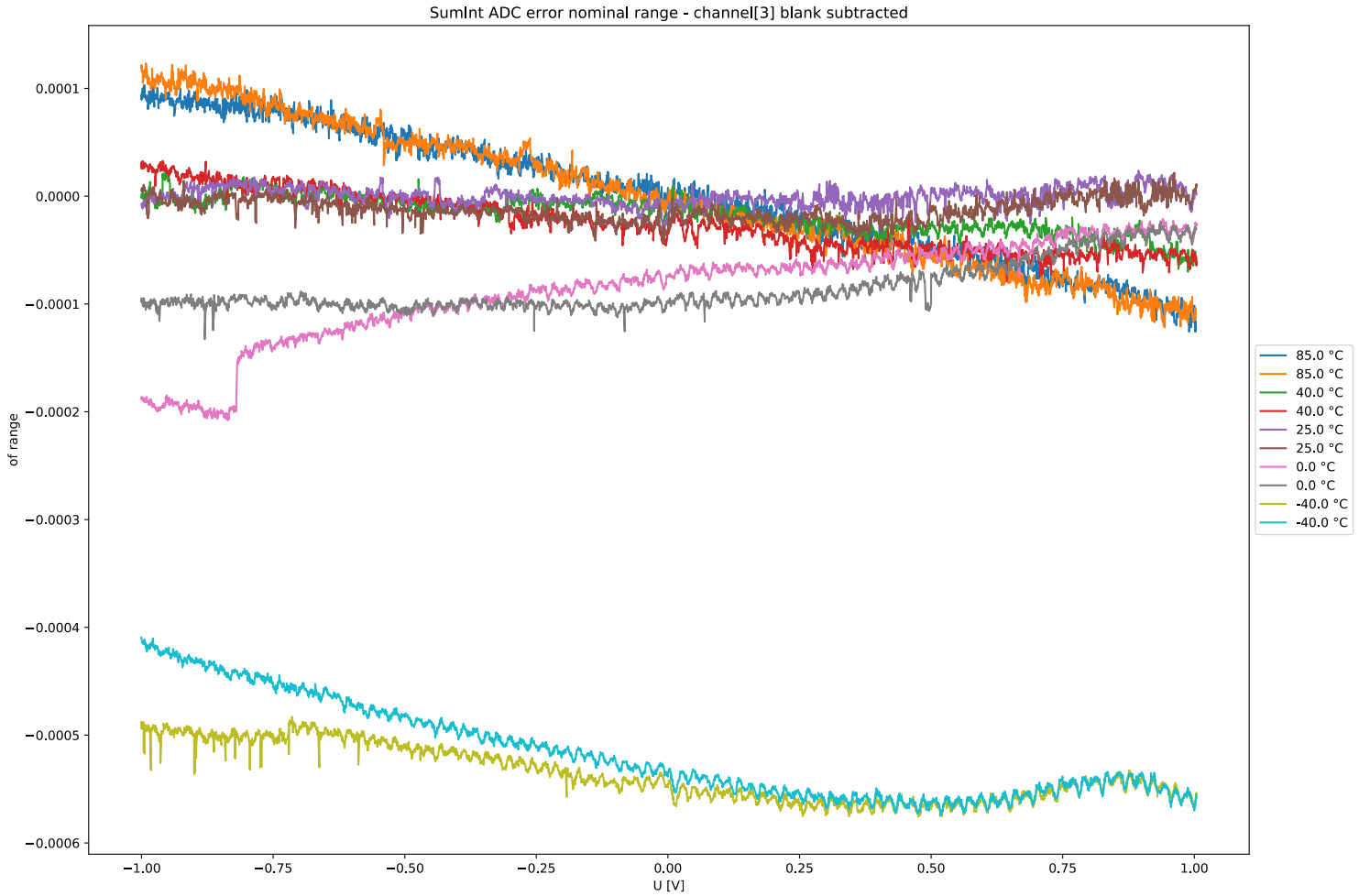
Simple 1 (0) – 2 (1) Error -40°C to 85°C



Advanced 2 (3) – Error -40°C to 85°C



Advanced 2 (3) - 1 (2), -40°C to 85°C



Static Characteristic Error Analysis

- Main source of error is the conversion characteristics offset (shift) in response to the temperature change which is accounted to the ADA4084 high input bias current which changes significantly with temperature. It is partially compensated by resistor network design but not fully for asymmetric power supply and input offset current is not compensated at all.

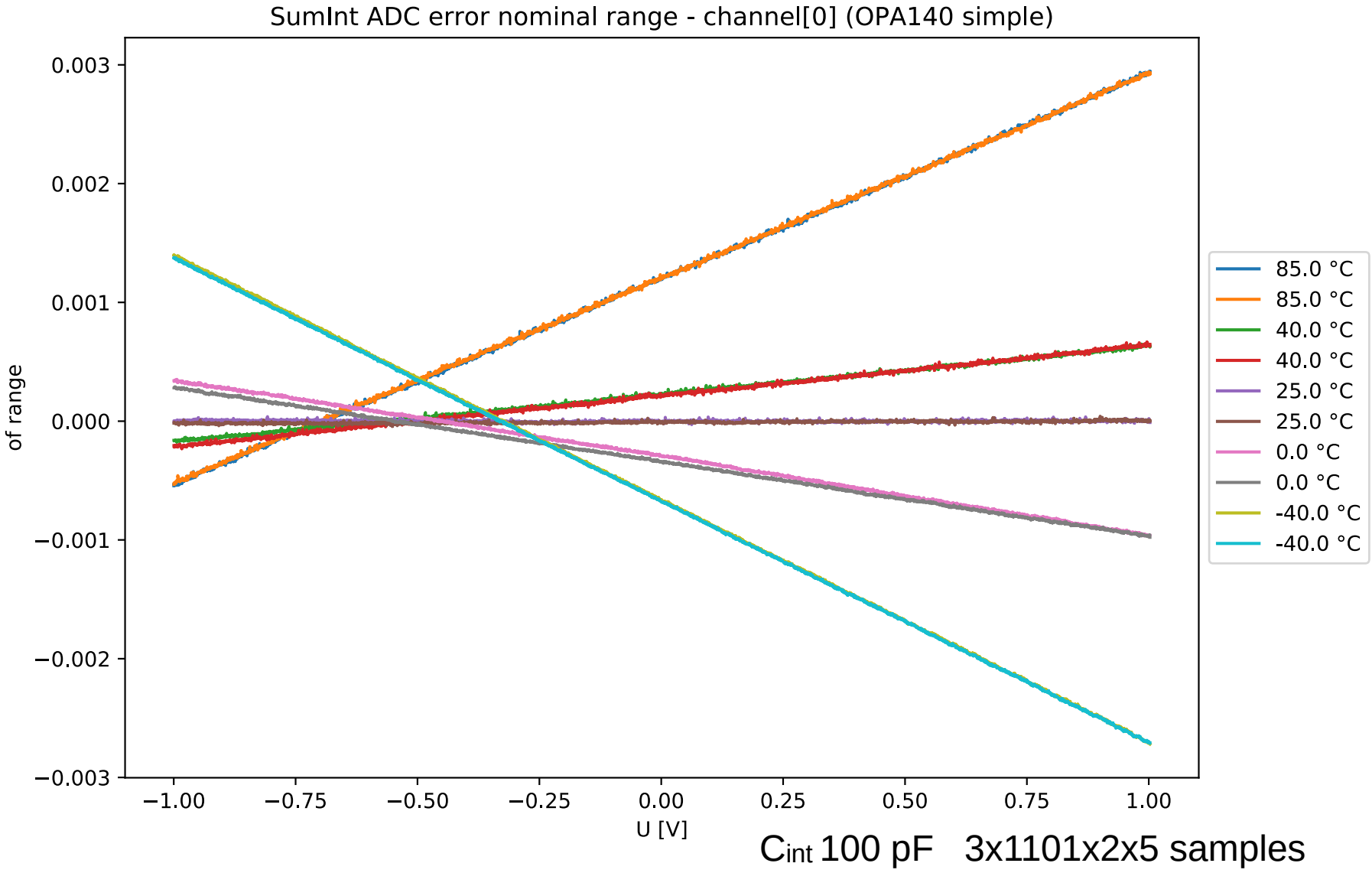
  Can be enhanced by use of OPA140/OPA4H014-SEP

- The conversion characteristic slope change is accounted to the resistors value change over temperature and mainly to the change of the R_{swon} resistance of the analog switch (realized NanoXplore pins for the simple case and M54HC125 for advanced)

  With contemporary OpAmp the resistors network can recomputed for higher resistance and ratio to R_{swon} will be favorable

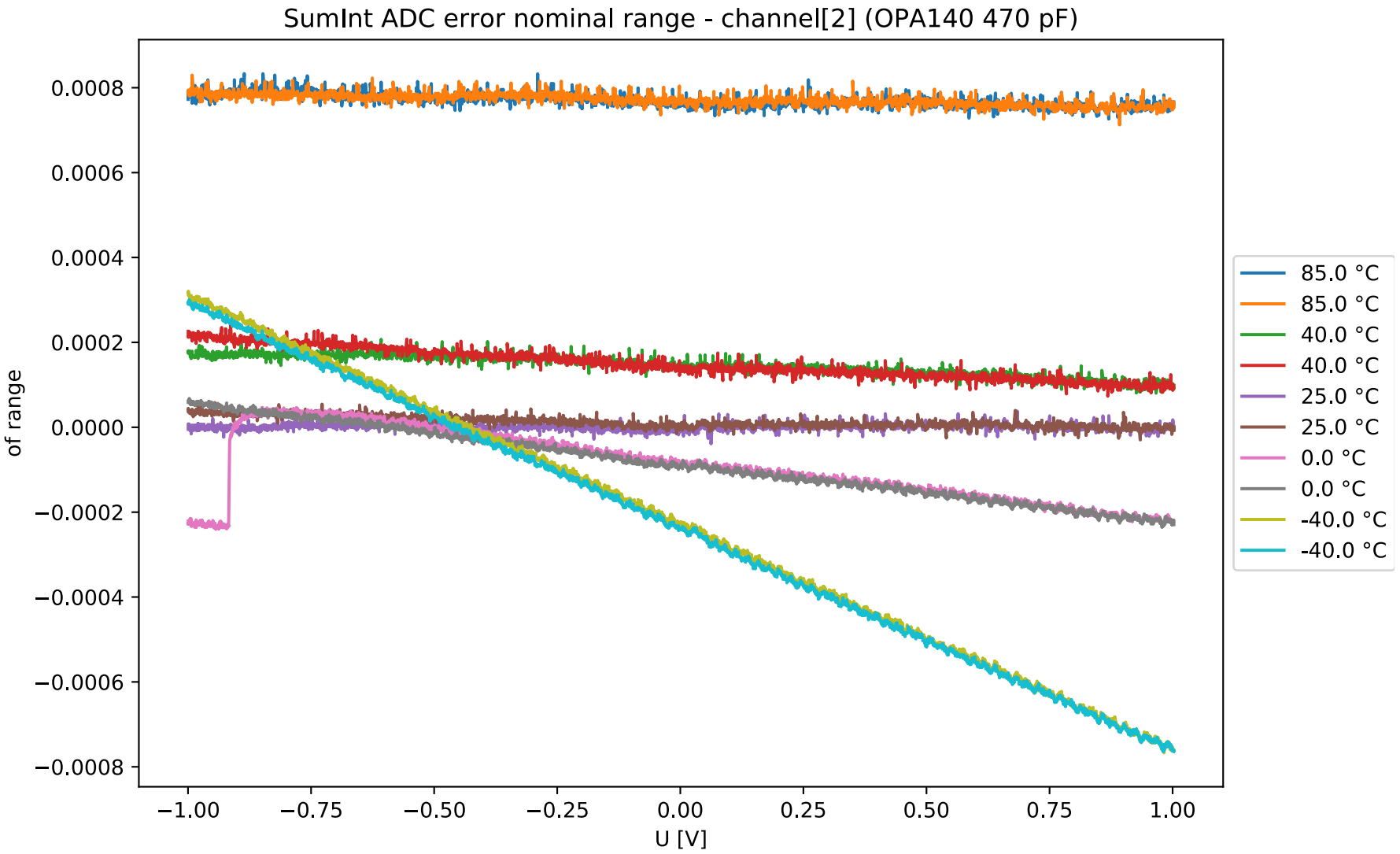
- Second round of tests with OPA140 provides better results

Short Test of OPA140 on Simple 1 (0)



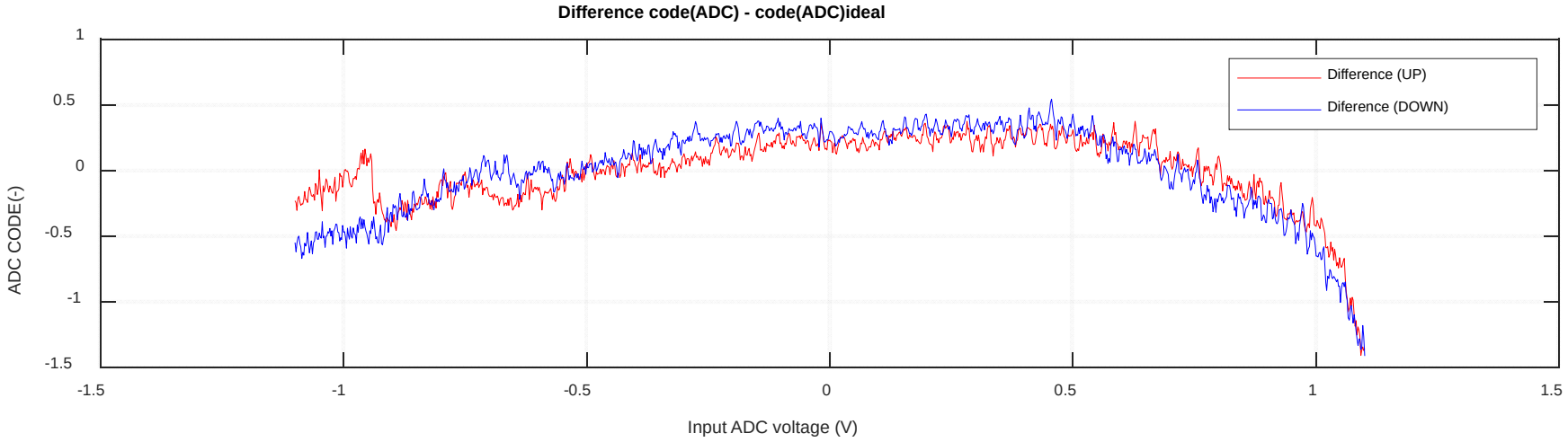
C_{int} 100 pF 3x1101x2x5 samples

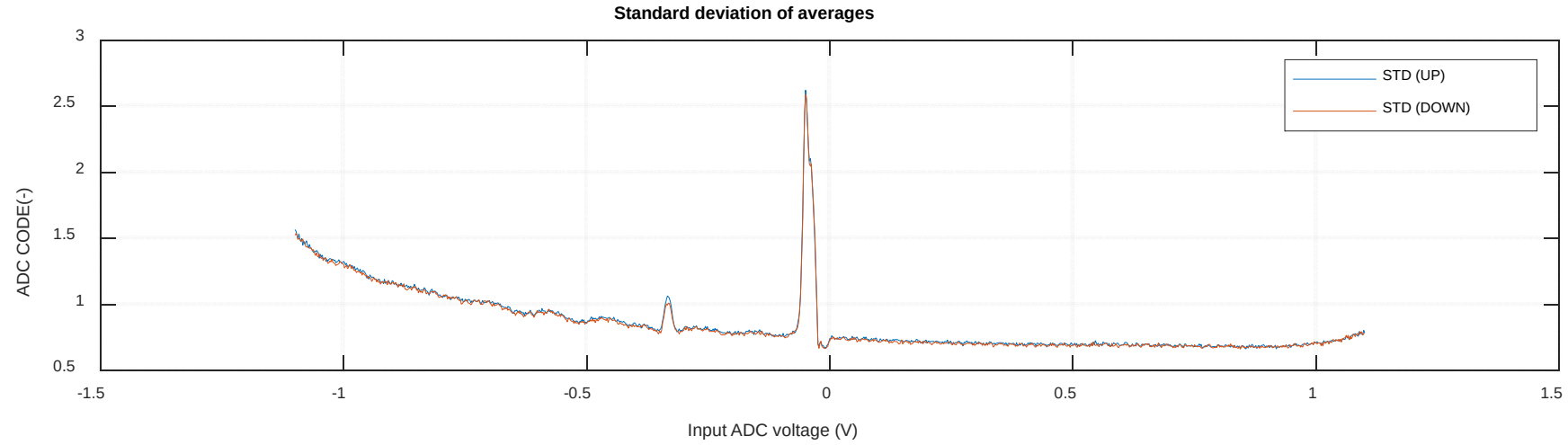
OPA140 Test on Advanced Channel 1



C_{int} 470 pF 3x1101x2x5 samples

Simple Channel Mutual Influence for Same Input Value – Aliasing of Switching Time





Noticed on measurement 1 when blind connected to 0V, can be on NanoXplore LVDS input comparators, outputs or FPGA bank power supply, advanced OK

Advanced Static Characterization

OpAmp type	Linearity at single temp.		Single raw sample at temp		Single raw sample, all temp	
	aver err	raw std	min	max	min	max
1. OPA140 ch2 470 pF	2.51e-04	5.11e-04	-1.09e-03	9.88e-04	-1.24e-03	1.77e-03
1. OPA140 noisy 0 °C removed	5.72e-05	5.11e-04	-1.09e-03	9.88e-04	-1.24e-03	1.77E-03
2. OPA140 ch3 100 pF	5.49e-05	5.10e-04	-1.09e-03	9.68e-04	-3.00e-03	2.90e-03
2. OPA140 blind subs	5.45e-05	5.10e-04	-1.10e-03	9.56e-04	-1.46e-03	1.57e-03
ADA4084	4.62e-05	4.78e-05	-1.78e-04	2.09e-04	-3.60e-03	3.53e-03

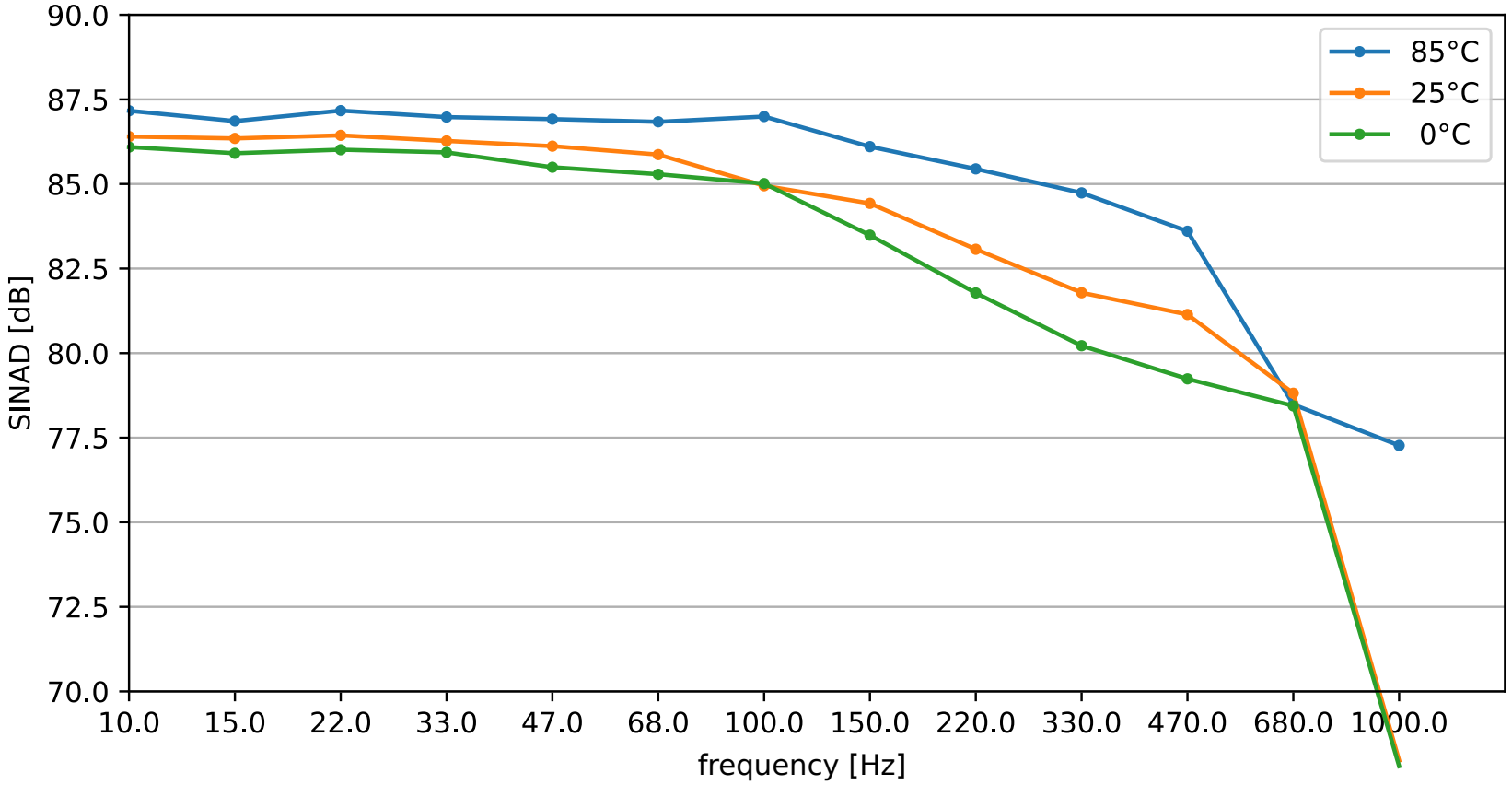
The OPA140 setup 1. uses C_{int} 470 pF, setup 2. C_{int} 100 pF
Values in the table represent ADC error relative to the Full Scale

Simple Chan. – Static Characterization

OpAmp type	Linearity at single temp.		Single raw sample at temp		Single raw sample, all temp	
	aver err	raw std	min	max	min	max
OPA140	5.78e-05	5.17e-04	-1.19e-03	1.10e-03	-3.25e-03	3.84e-03
ADA4084	4.69e-05	1.44e-04	-4.27e-04	4.70e-04	-2.68e-03	6.45e-03

Values in the table represent ADC error relative to the Full Scale

Results of Dynamic Testing



- Advanced Channel, on ADA4084 only for now
- The sine fitting modified to take non-equidistant sampling
- Value computed by from ref+ divided by individual sampling intervals
  x_val = 2*Tclk*x_samp[2:end]./(Tsamp .+ Tclk*(x_subs[2:end] - x_subs[1:end-1]))

Dynamic Characterization Summary

- ADC input excitation – a harmonic signal, constant amplitude close to the full range
- frequencies 10, 15, 22, 33, 47, 68, 100, 150, 220, 330, 470, 680, 1000 Hz
- Raw data, no floating sampling interval accounted, resolution unusable.
- When SumInt principle accounted:
- SINAD for the advanced > 78 dB up to 680 Hz, SINAD > 85 Hz up to 100 Hz.
- simple (on FPGA pins) SINAD > 80 dB till 100 Hz, lower to 75 dB at 680 Hz
- actual integrating character is not modeled during fitting – for integration applications can provide even better results
- ENOB = (SINAD_dB – 1.76)/6.02
- resolution in range between 13 and 14 bits is confirmed.
- from previous quantization noise is suppressed by factor 1/n for given setup from modulator frequency down to the area about 1 kHz where curve switches to the standard $1/\sqrt{n}$ slope

References/Links

- PiKRON.com: Spectrophotometric detector LCD 5000 – User manual
  http://pikron.com/pages/products/hplc/lcd_5000.html
- P. Píša, P. Porazil, Σ-Integration analog to digital converter, Idea, implementation and results, IFAC Proceedings Volumes, 2005, 38.1: 85-90., 16th World Congress of the International Federation of Automatic Control
  https://www.sciencedirect.com/science/article/pii/S1474667016372056
- PiKRON LX_CPU board documentation and schematics
  https://www.pikron.com/pages/products/cpu_boards/lx_cpu.htm l
- PiKRON LX_RoCoN motion controller system documentation
  http://www.pikron.com/pages/products/motion_control/lx_rocon.html
- nanoXplore BRAVE NG-MEDIUM FPGA and NX1H35AS-EK evaluation kit
  https://www.nanoxplore.com/
- XilinX Zynq MZ_APO education kit
  https://cw.fel.cvut.cz/wiki/courses/b35apo/en/documentation/mz_apo/start
- PiKRON SumInt ADC GitLab project
  https://gitlab.com/pikron/projects/sumintadc