Sum-Integration Analog to Digital

Implementation and Evaluation of Sum-Int ADC IP-core on NanoXplore FPGA

9th International Workshop on Analogue and Mixed-Signal Integrated Circuits for Space Applications – AMICSA 2022

Company: PiKRON, s.r.o. (Czech Republic)
Project page: https://gitlab.com/pikron/projects/sumintadc
ESA De-Risk 4000134870/21/NL/GLC/rk

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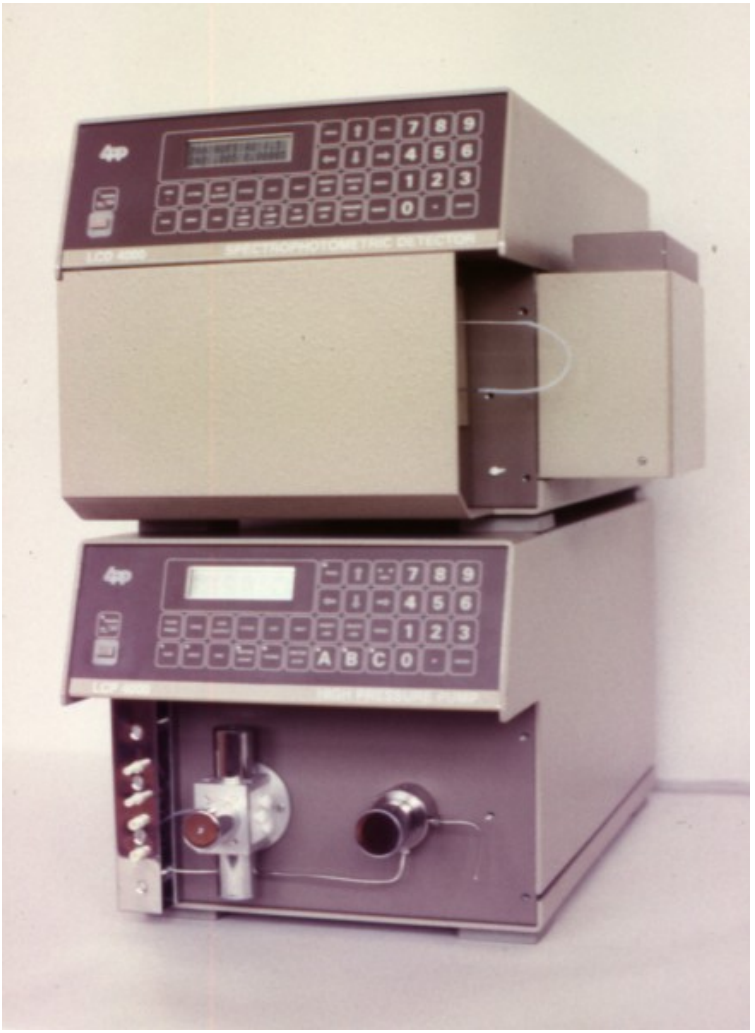
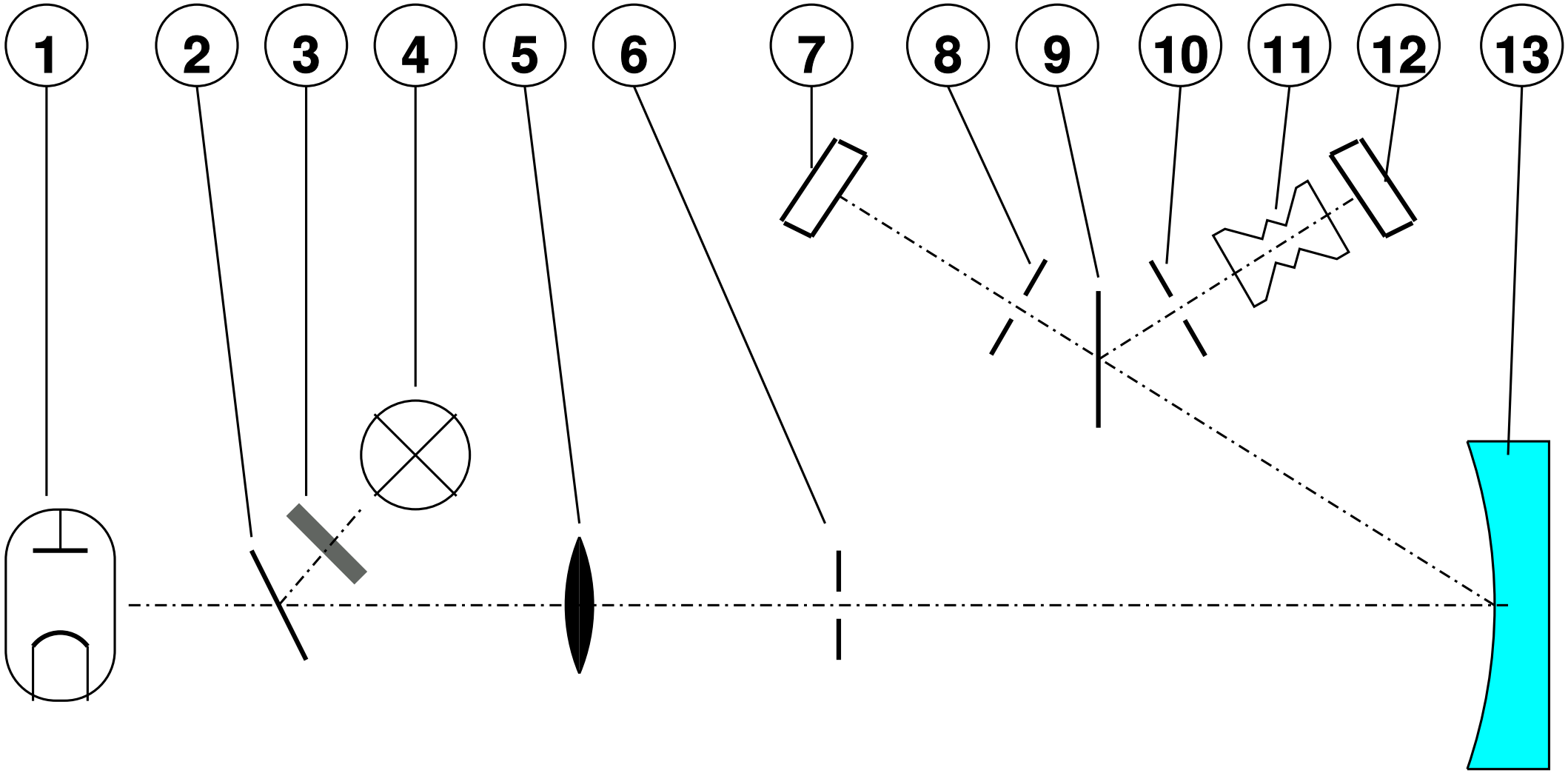
LCD 4000 UV VIS HPLC Detector – before SumInt

- **Laboratory Instruments Praha – 1989/1990**
- Classical double integration principle has been used, the first based on five 74193 chips then on combination of 74193 chip combined with 16-bit counter in Intel 8253
- Many LC 4000 systems has been delivered and served for more than 20 years in daily routine on polypeptide, cancer cure and other research
- Typical system setup
  - LCD 4000 HPLC UV VIS detector
  - LCP 4000 high performance (40 MPa) HPLC pump
  - CHROMuLAN – open source chromatograhy station system

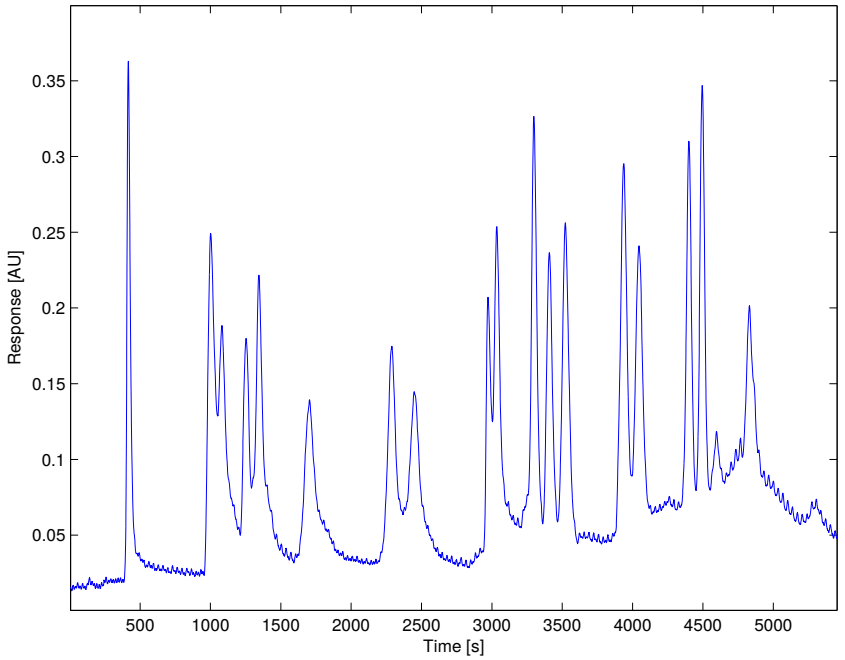


Source: http://pikron.com/pages/company/history.html

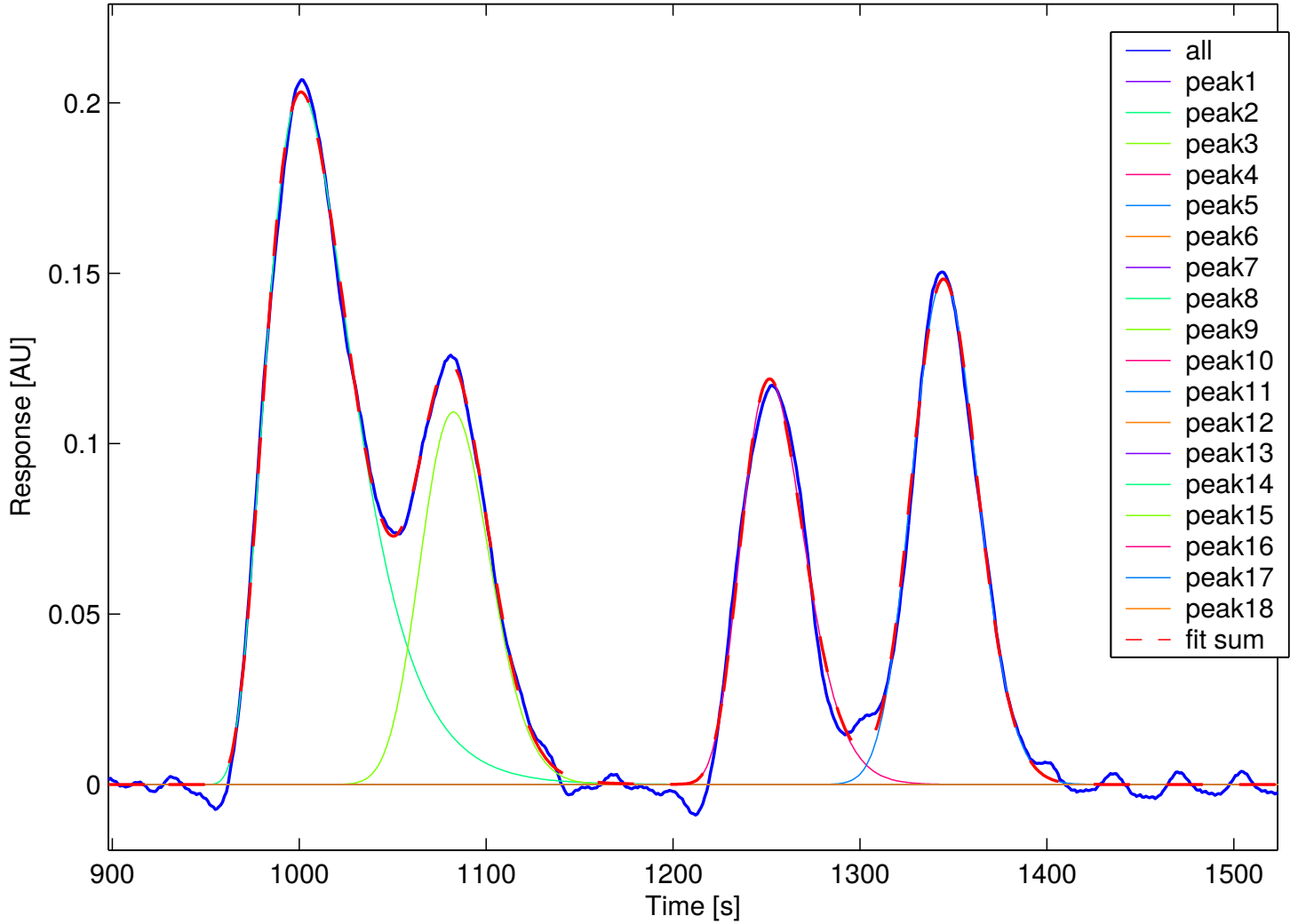
HPLC Detector Optical Setup



HPLC Signal and Areas under Peaks

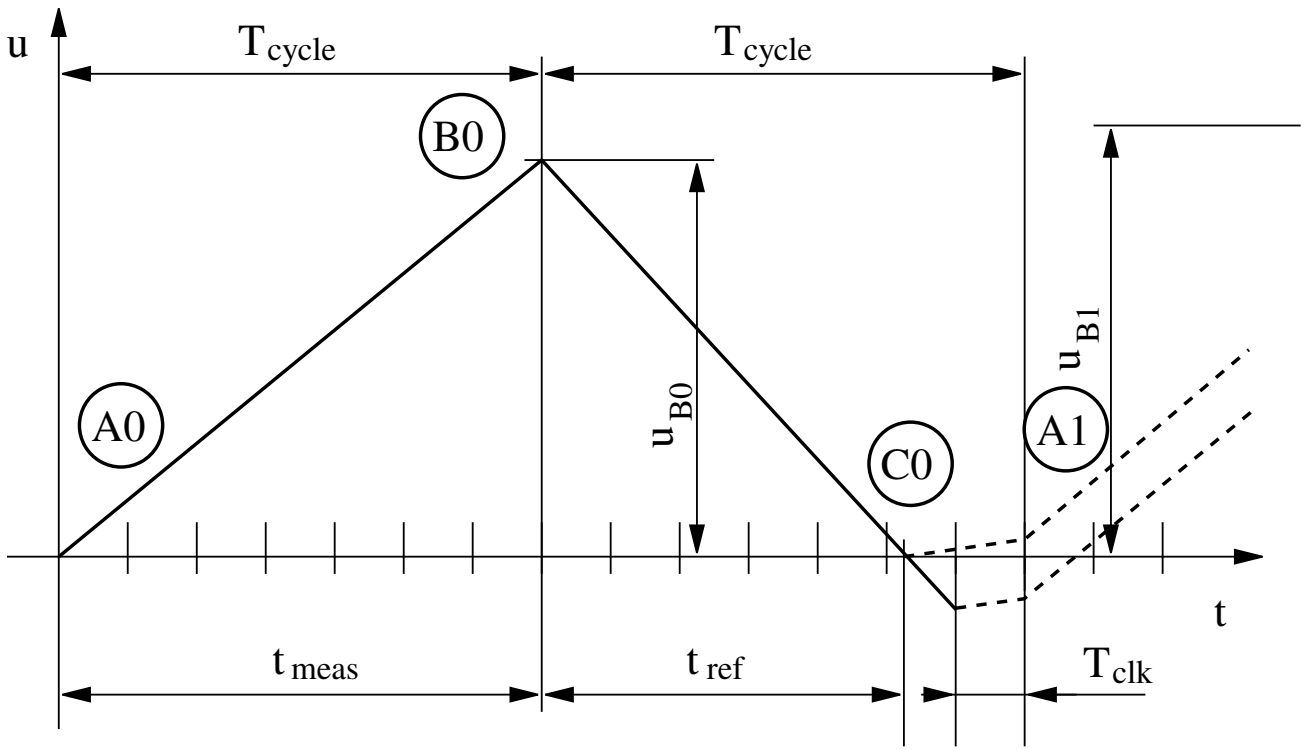


The assay output is integral/area under each peak which is proportional to the chemical compound concentration in the original sample



Double Integration ADC Challenges and New Goals

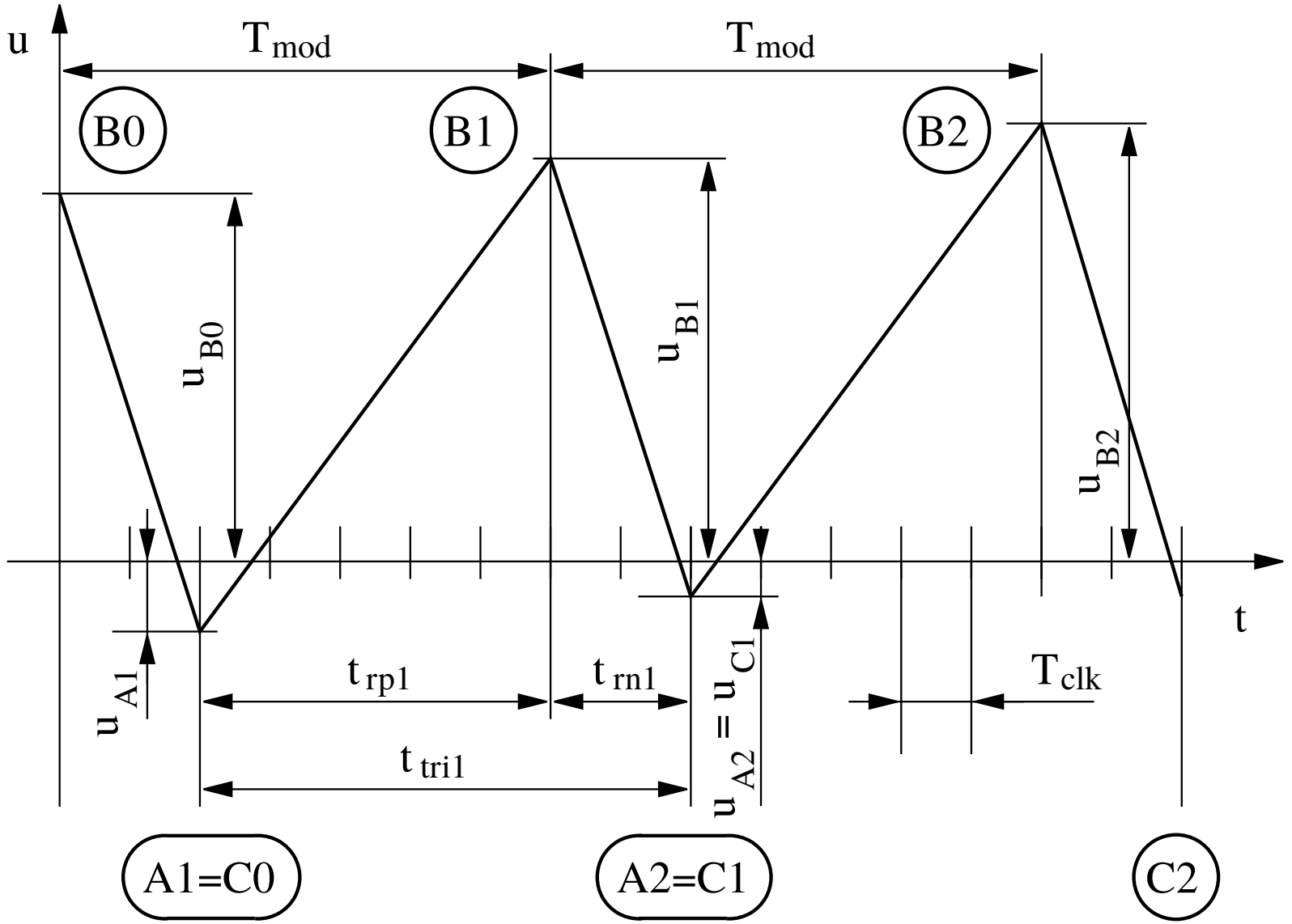
- The input is integrated only part of time between A_i and B_i
- Start of new cycle at A_{i+1}
- The second problem can be solved by active zeroing but each semiconductor electronic switch injects some charge during changing between conductive and insulator states. Problem is not easy to resolve.



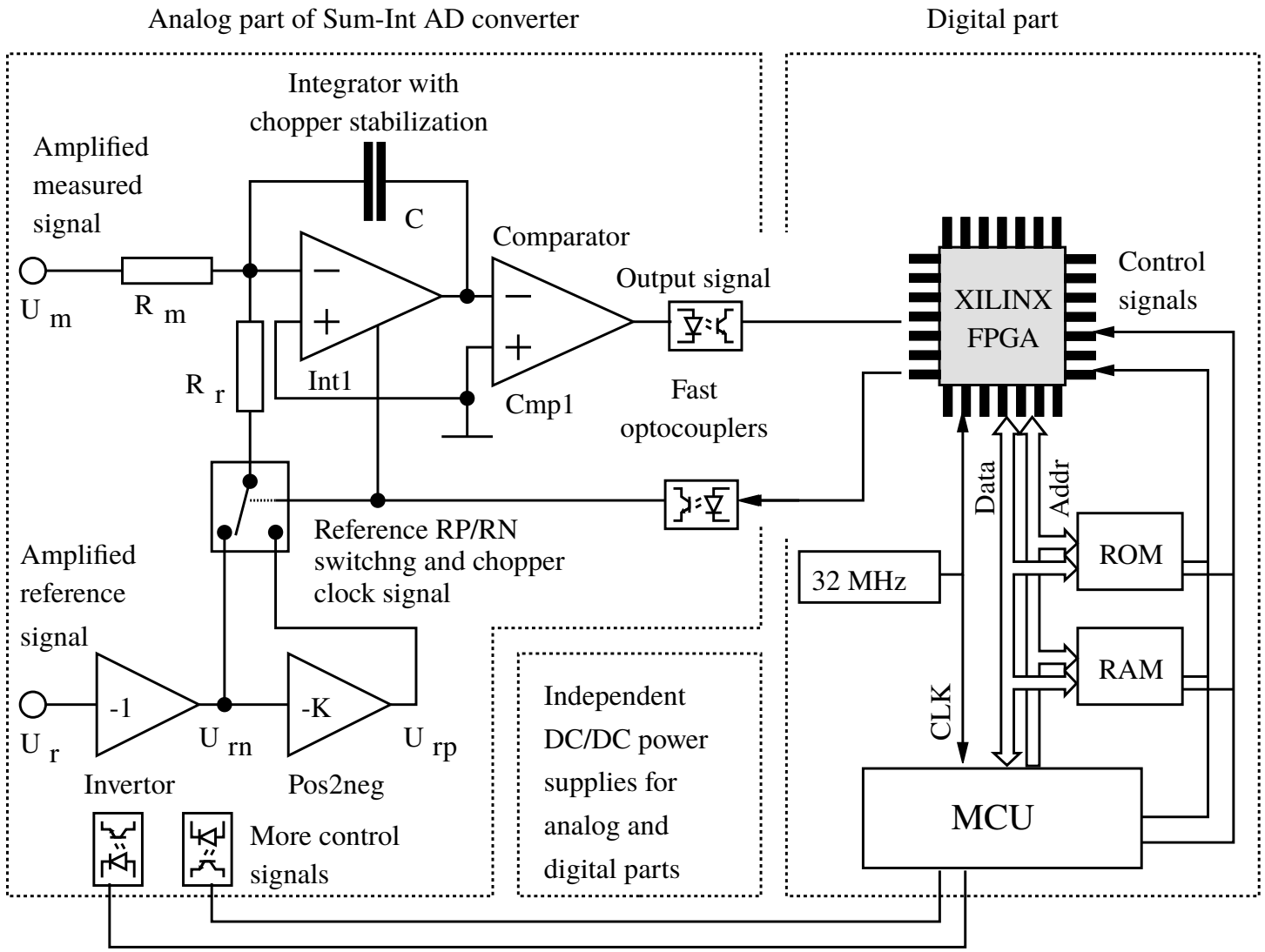
- LCD 5000 – required resolution better than $1 \cdot 10^{-5}$ AU.
- Primary digital signals filtering with noise suppress better than $1/\sqrt{n}$
- Continuously integration of input, ratio conversion (1 ms ref. Stability)
- 25 Hz uncorrelated, filtering 22 bits @1 Hz

Suma-Integration ADC Principle

- Never reset the integrator
- Continuous integration of input signal
- Switching only application of positive and negative reference
- Error/unconverted charge/voltage reminder preserved into next cycle – zero integral error in theory

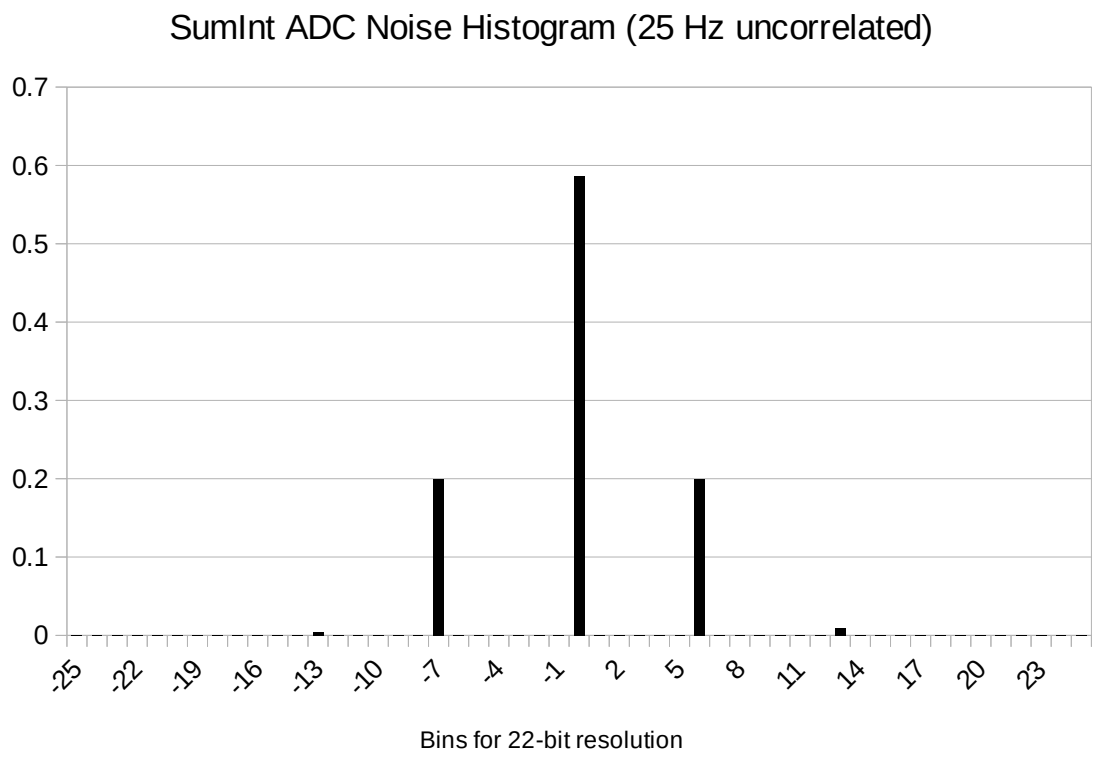


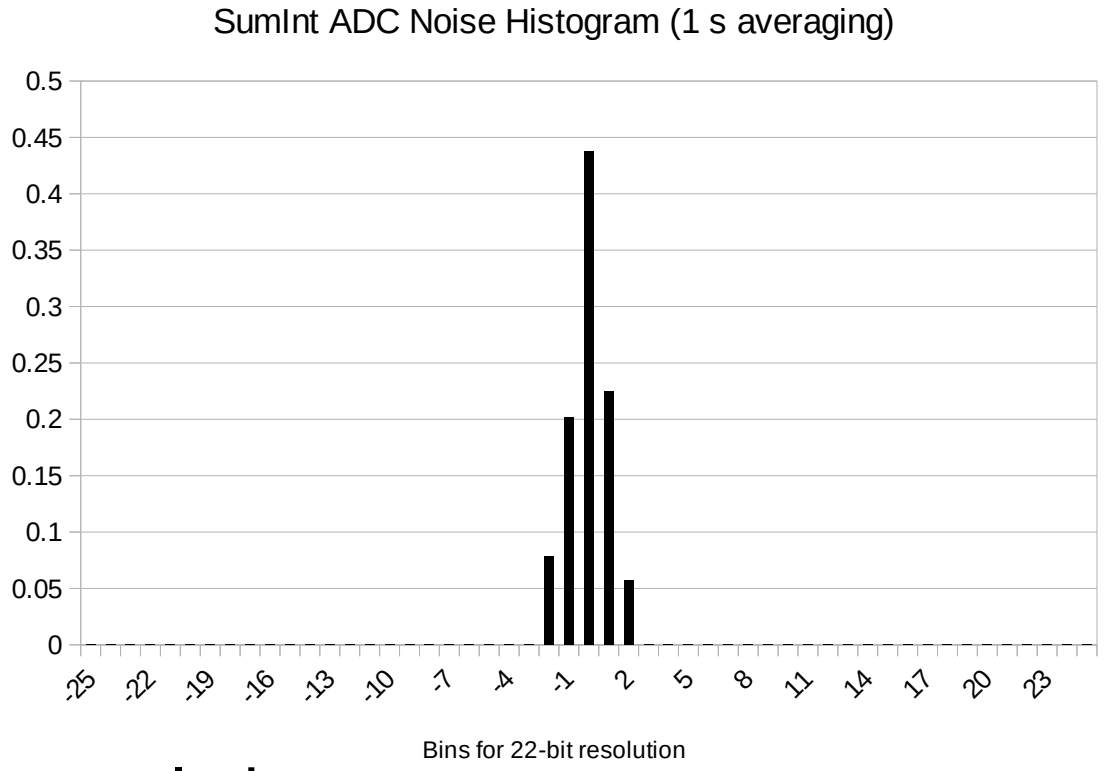
SumIntADC Realization In 1999 Year



- OPA129 – electrometric inputs
- OP07 – ref. conditioning
- ADG444 – ref. and inp. switch
- TLC2652 – integrator, chopper stabilized synchronized with conversion cycle
- LM311 – comparator
- HCPL7721 – optocoupler, in ref. switch, out. comparator
- Digital side, 32 MHz driven XC3064-PQ160 and SAB-C509-LM

SumInt ADC Achieved HPLC Results

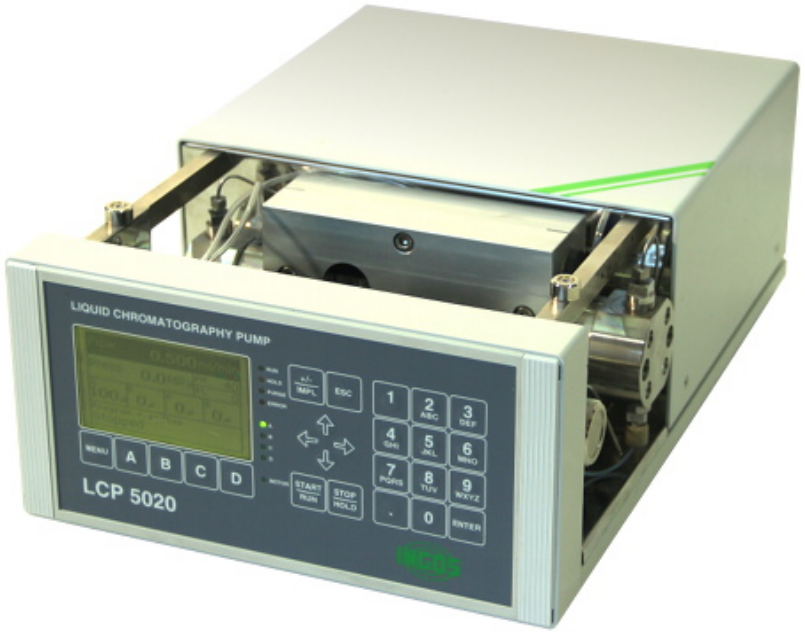


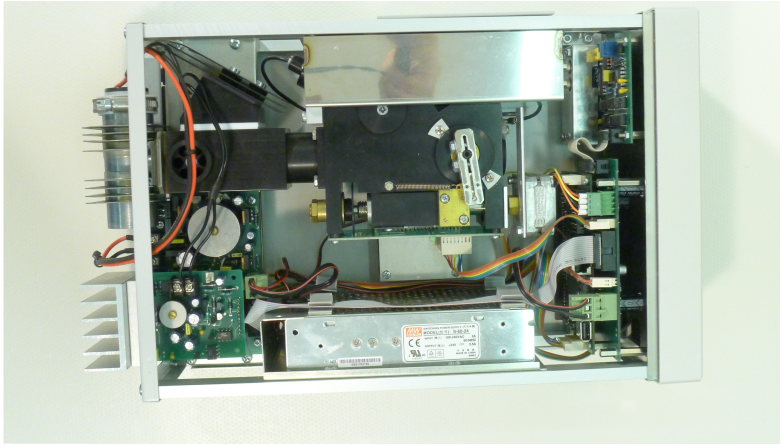


- The bins on graphs correspond to 22-bit resolution
- The signal has been acquired for 300 second
- Raw samples (25 Hz) falls into bins equivalent 19 bits resolution. Simple moving average enhances resolution to almost 22 bits. Better than $1/\sqrt{n}$

Digital Design Updated in 2013 Year

- LX_CPU processor board
  - LPC4088 (Cortex-M4F)
  - Xilinx XC6SLX9 – optional
- For HPLC UV VIS detector application FPGA not required
- Whole SumIntADC principle impeded with a half of 74LVC112, 74LVC1G86 and LPC4088 internal counter/timer capture and compare units
- Fast ADC clock (modulator time quanta) frequency increased to 72 MHz

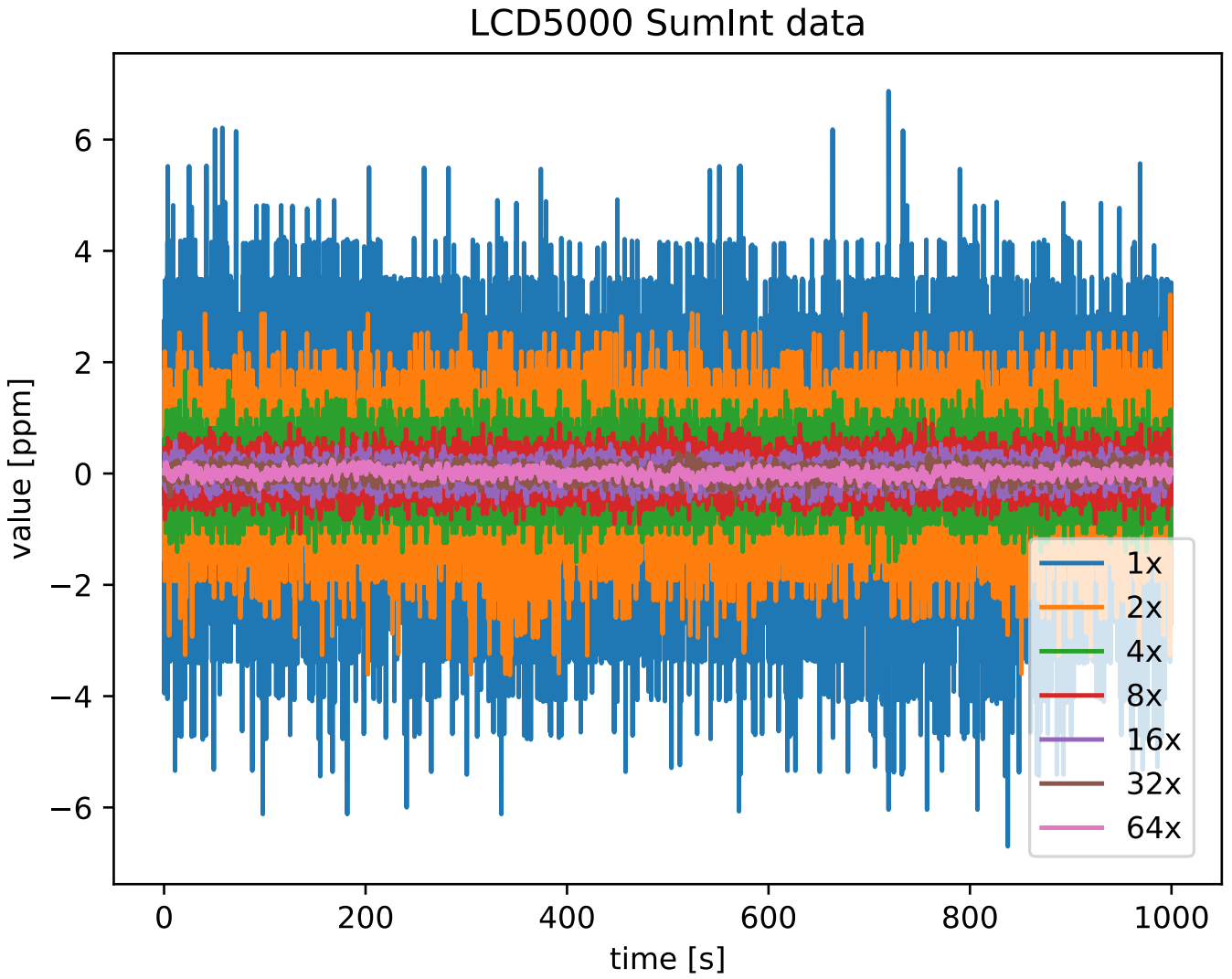




source: http://pikron.com/pages/products/cpu_boards/lx_cpu.html
source: http://www.pikron.com/pages/products/hplc/lcd_5000.html

Complete PiKRON's HPLC Setup

Updated System Zero/Null Signal

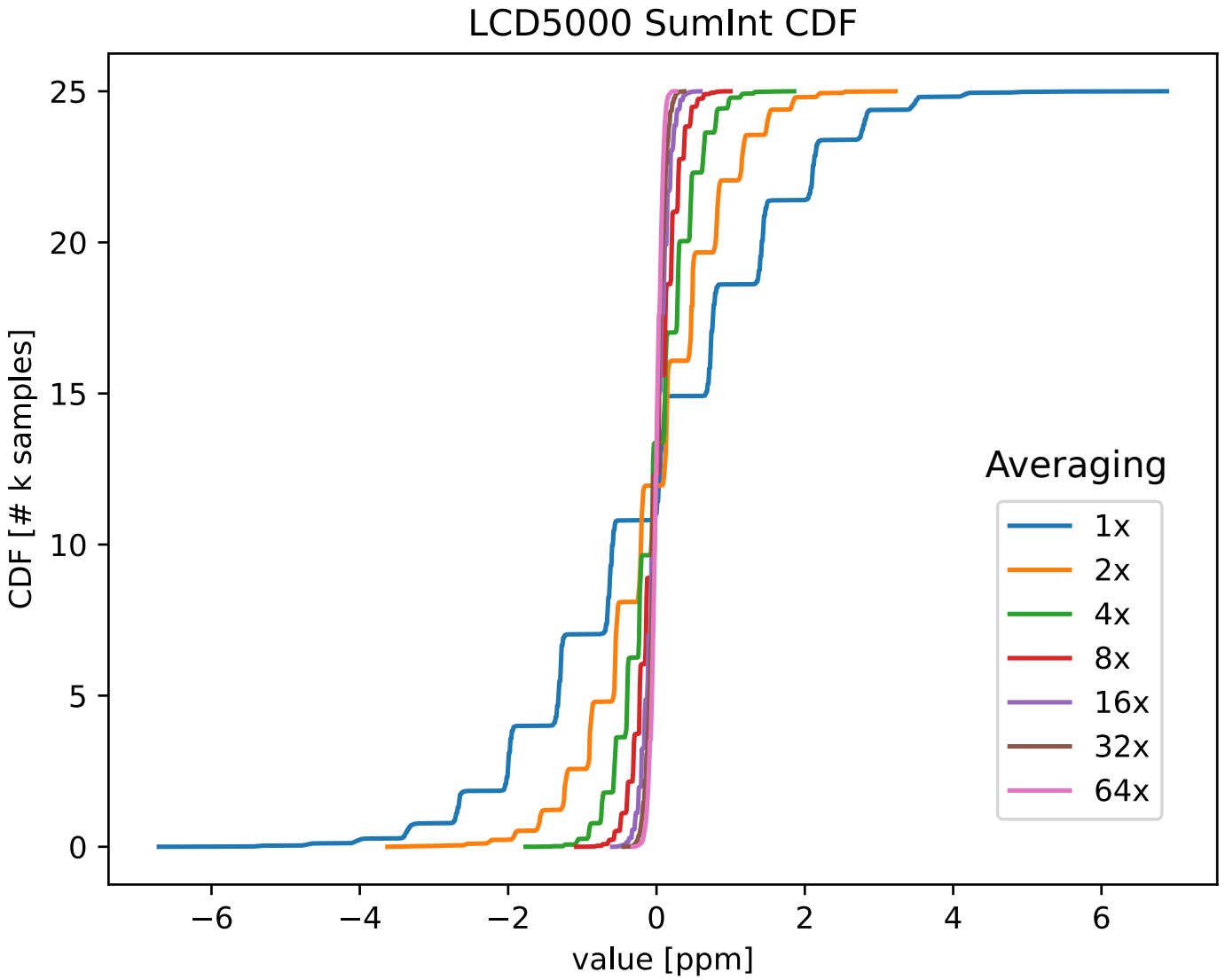


LCD 5000/
LCD 61 HW

f_{adcclk} = 72 MHz
f_{adcmod} = 5 kHz
$f_{averaging}$ = 25 Hz

output moving averaging
0.04 s to 2.56 s

Updated System Zero/Null Signal CDF

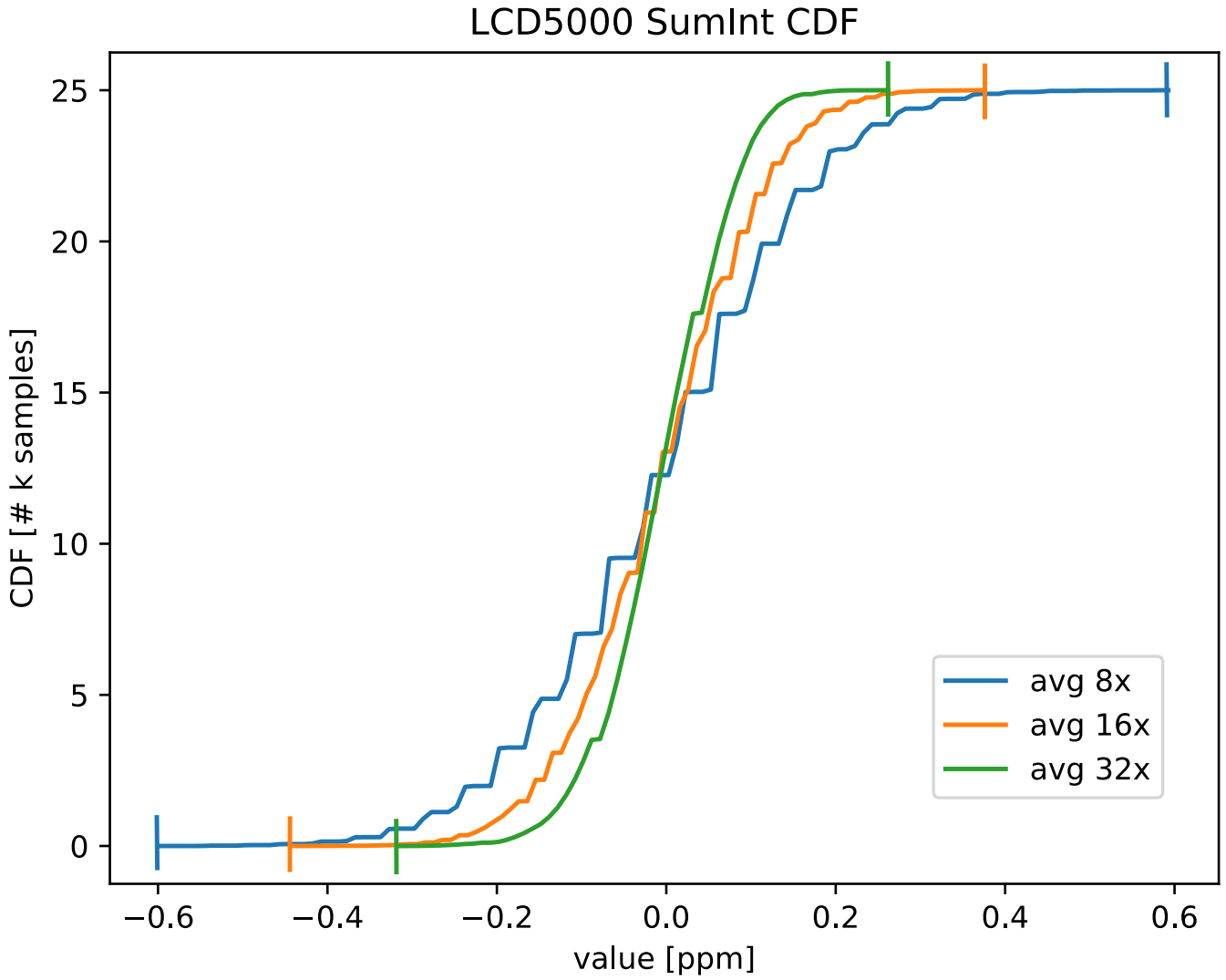


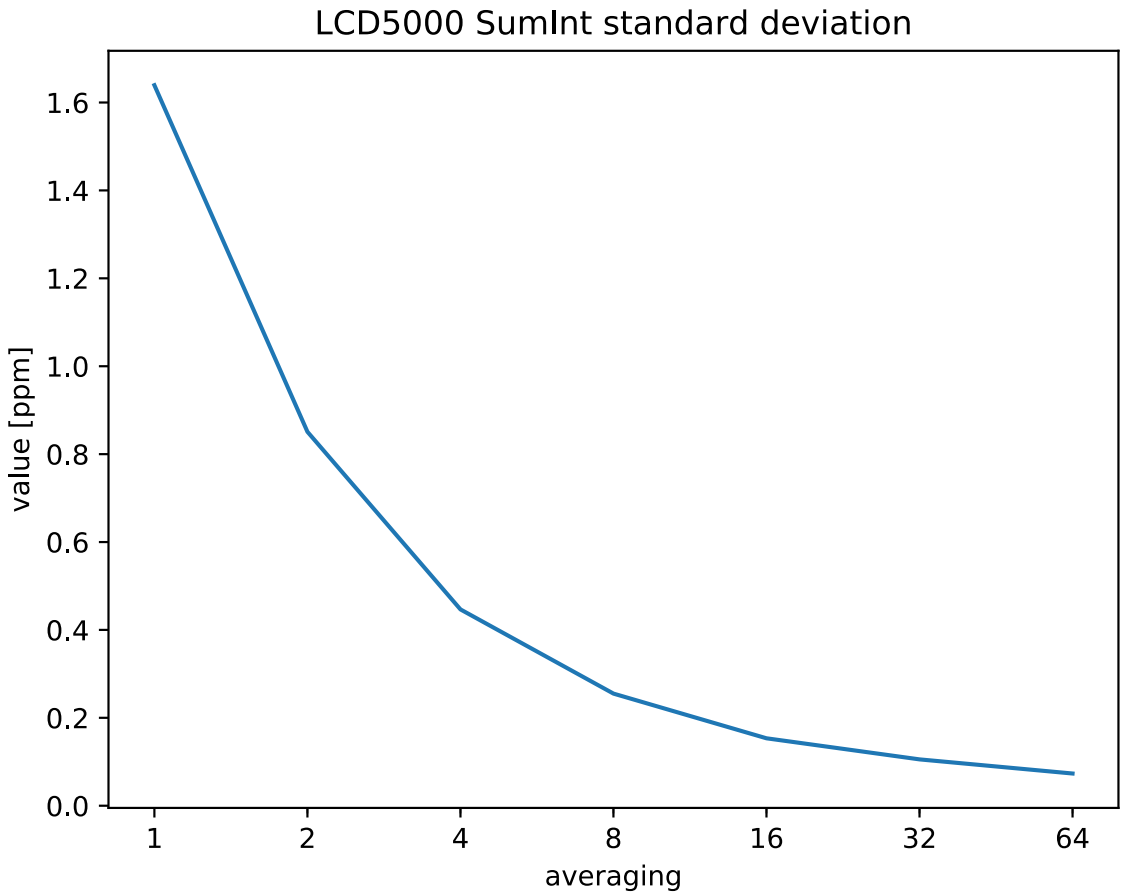
LCD 5000/
LCD 61 HW

f_{adcclk} = 72 MHz
f_{adcmod} = 5 kHz
$f_{averaging}$ = 25 Hz

output moving averaging
0.04 s to 2.56 s

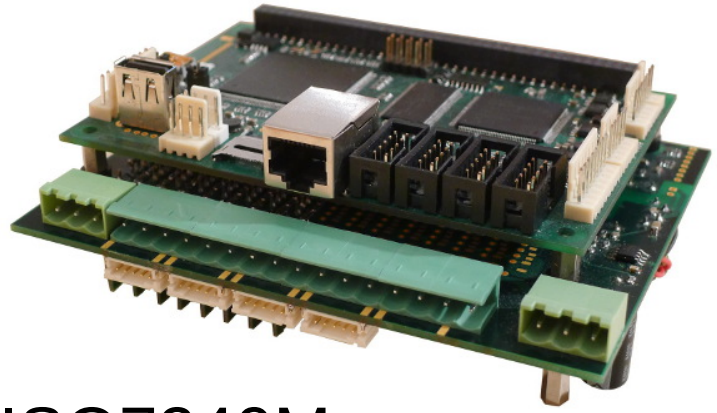
Null Signal CDF Zoom 0.64 to 2.56 s and STD





LX_RoCoN Motion Controller

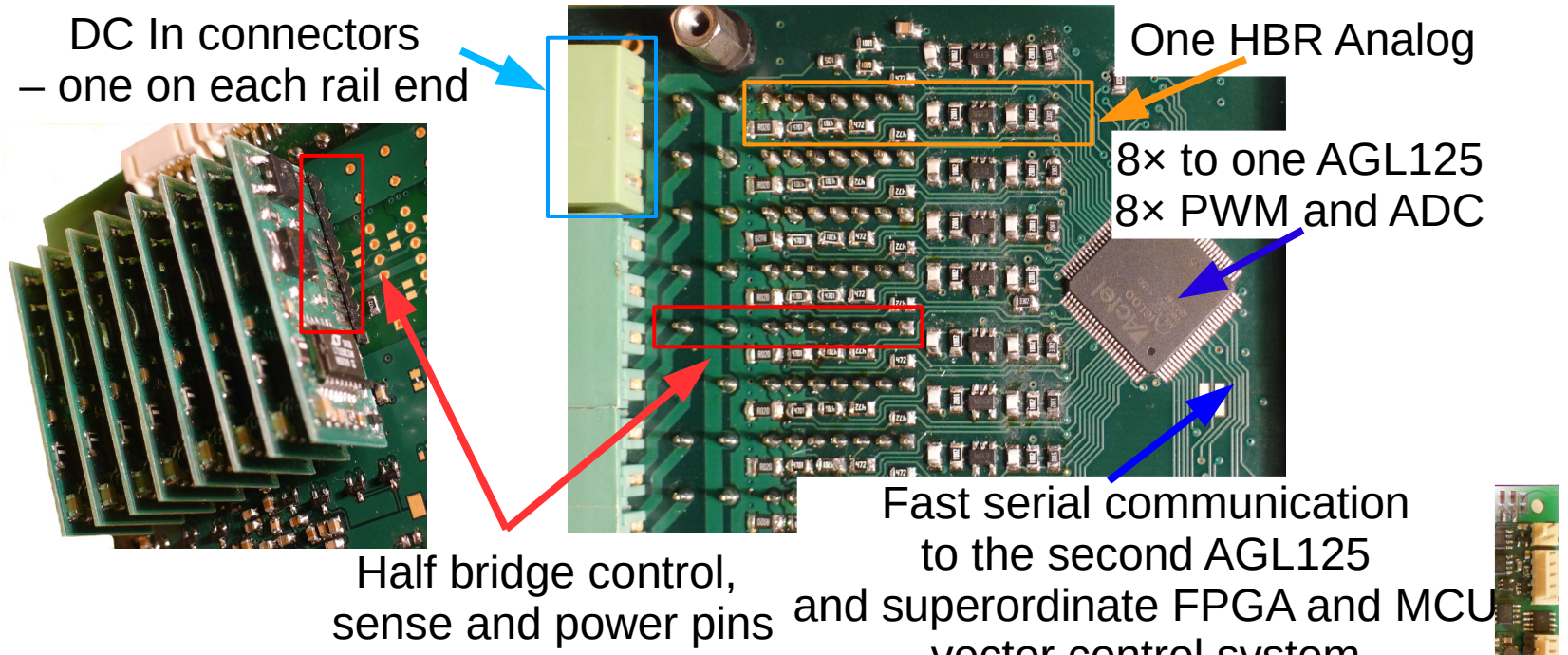
- LX_CPU processor board
  - LPC4088 (Cortex-M4F)
  - Xilinx XC6SLX9



- 16× 5 A, up to 28 VDC
- 16× Microsemi IGLOO and 2× ISO7240M
- SPI like communication between XC6SLX9 and IGLOO
- Return clock signal to match data on 50 MHz
- SumInt ADC realization on MCP6021T-E/OT
- In production from 2016

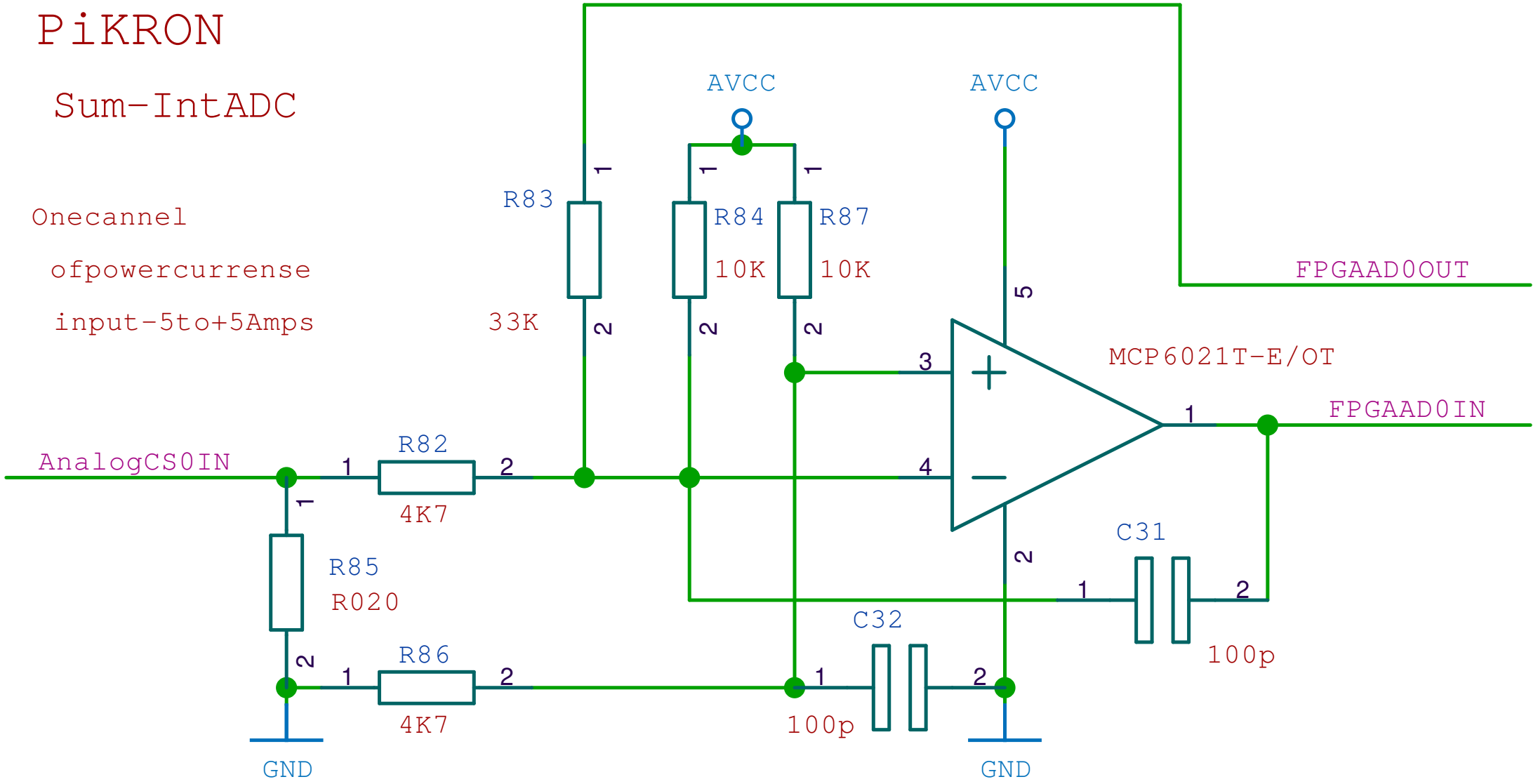
LX_RoCoN SumInt ADC Solution

- Example: up to 4 BDLC/PMSM and IRC equipped or sensor-less stepper motor control (16× 5 A, up to 28 VDC, fully protected phase half-bridges)

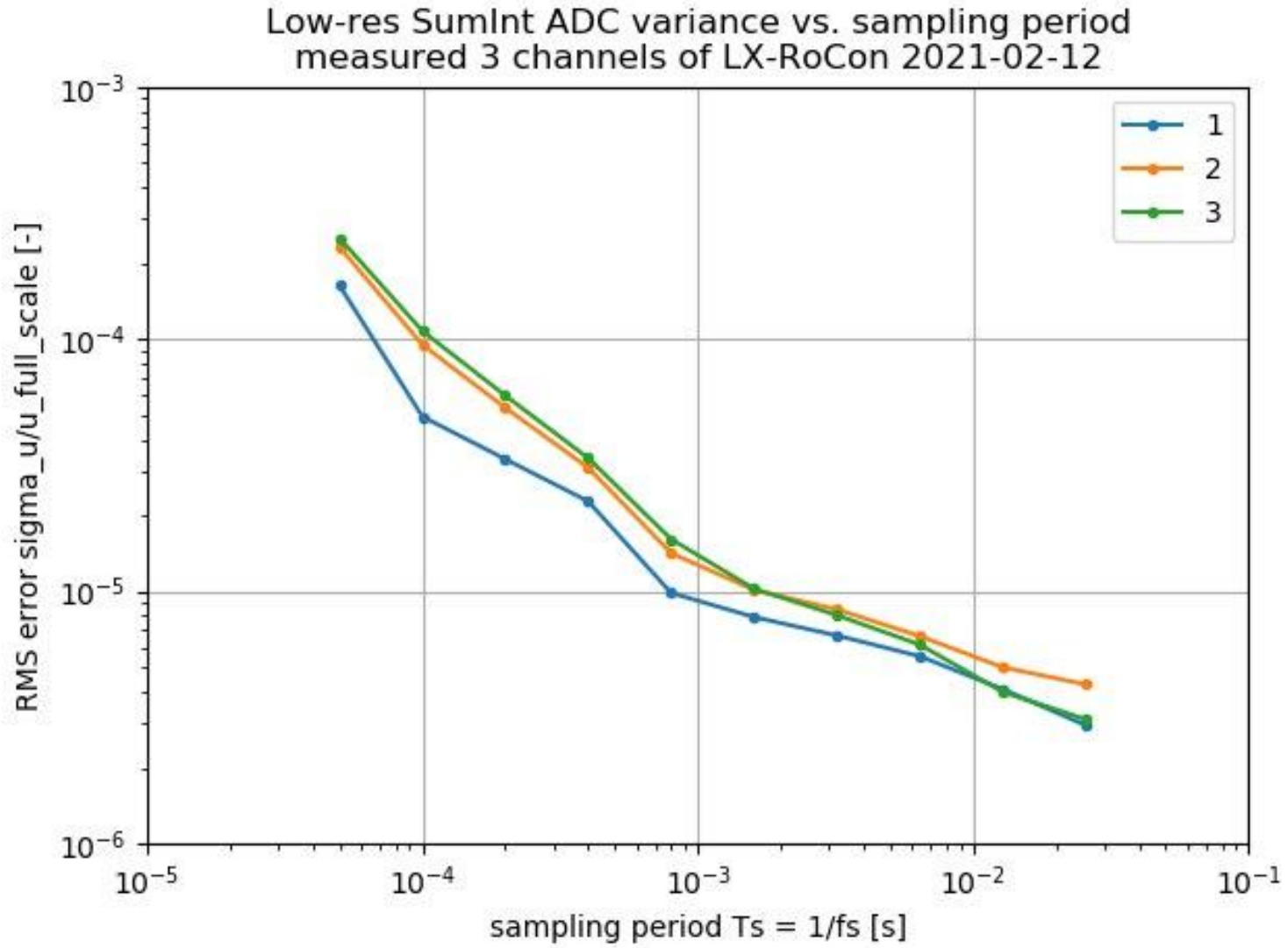


- Current and PWM D-Q transformations and commutation completely driven by Xilinx FPGA

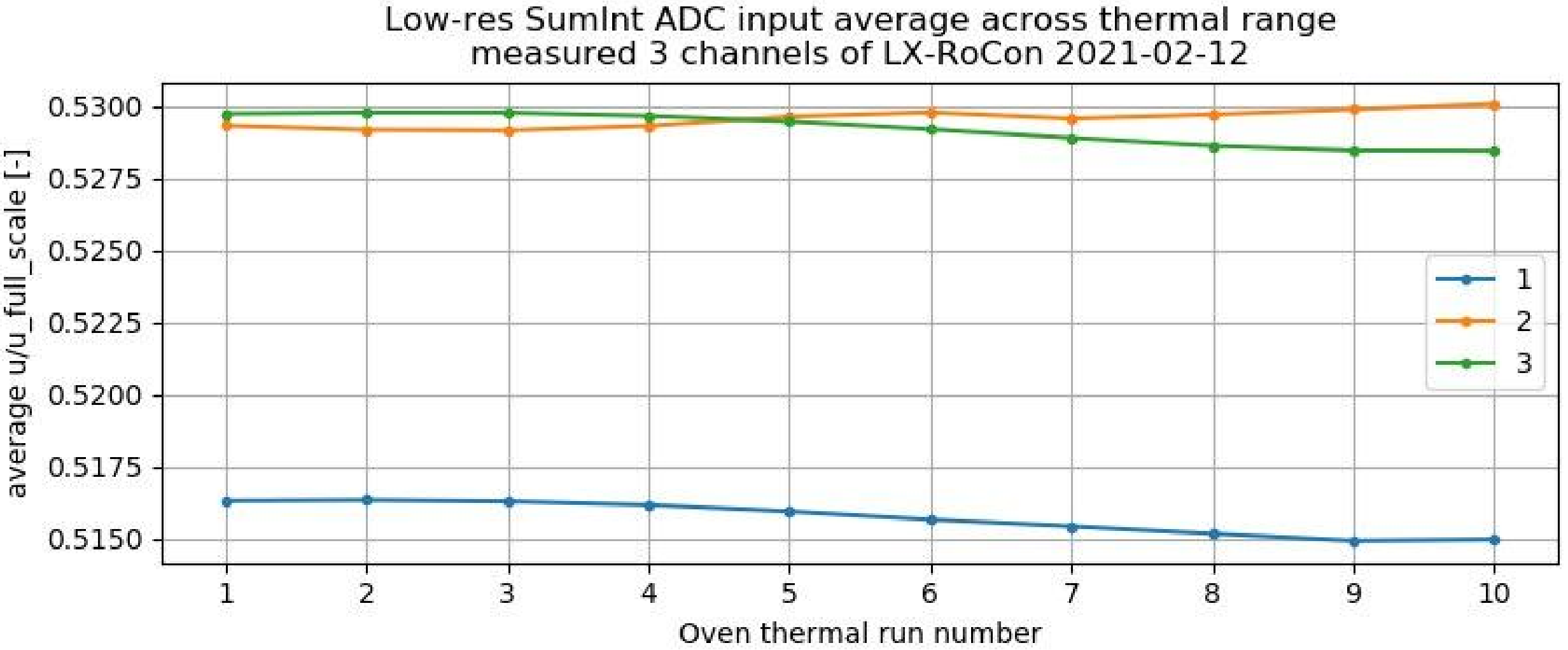
LX_RoCoN SumInt ADC Channel



LX_RoCoN – Noise for Zero/Null Input



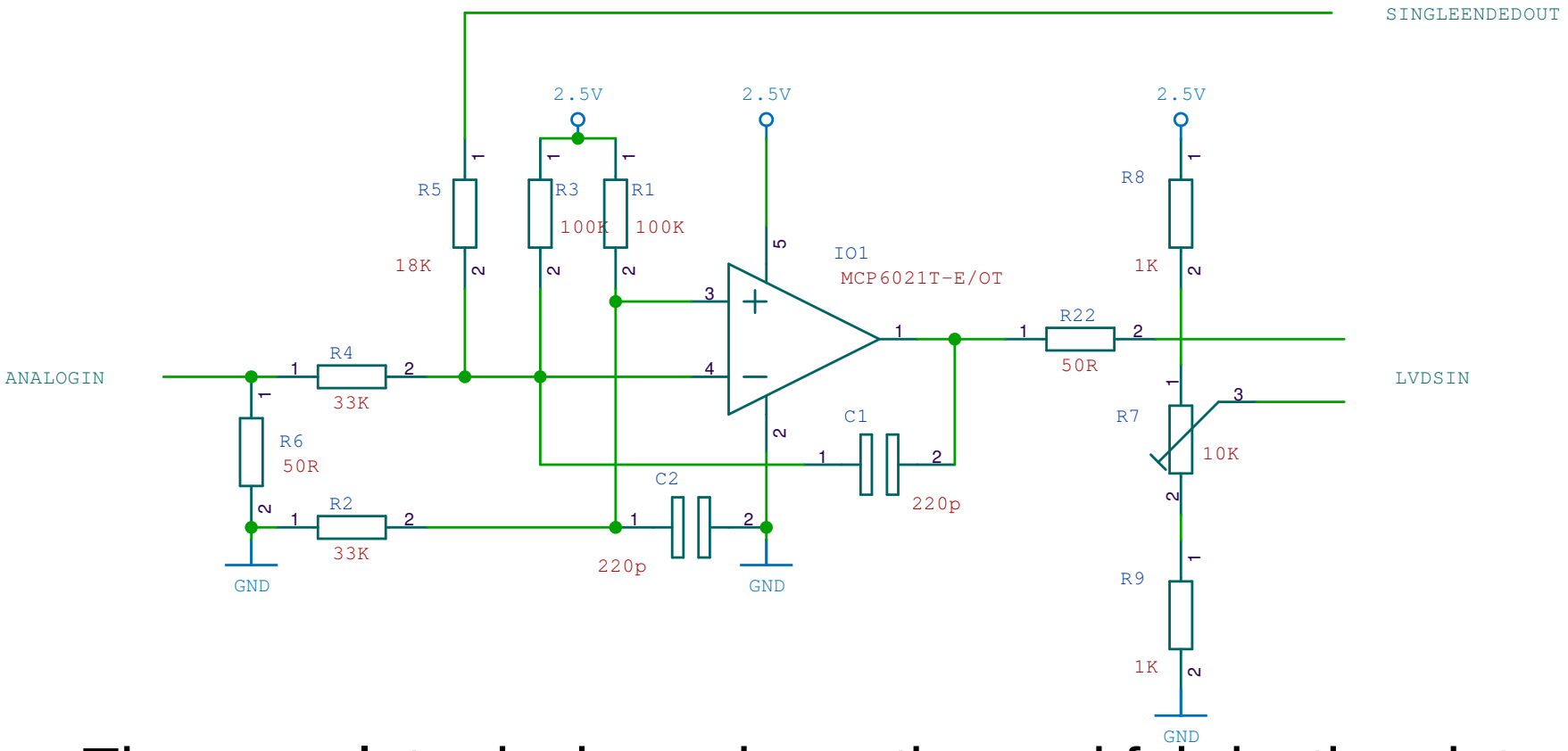
LX_RoCoN – Test fom 24°C to 74°C



Space Grade Operational Amplifiers

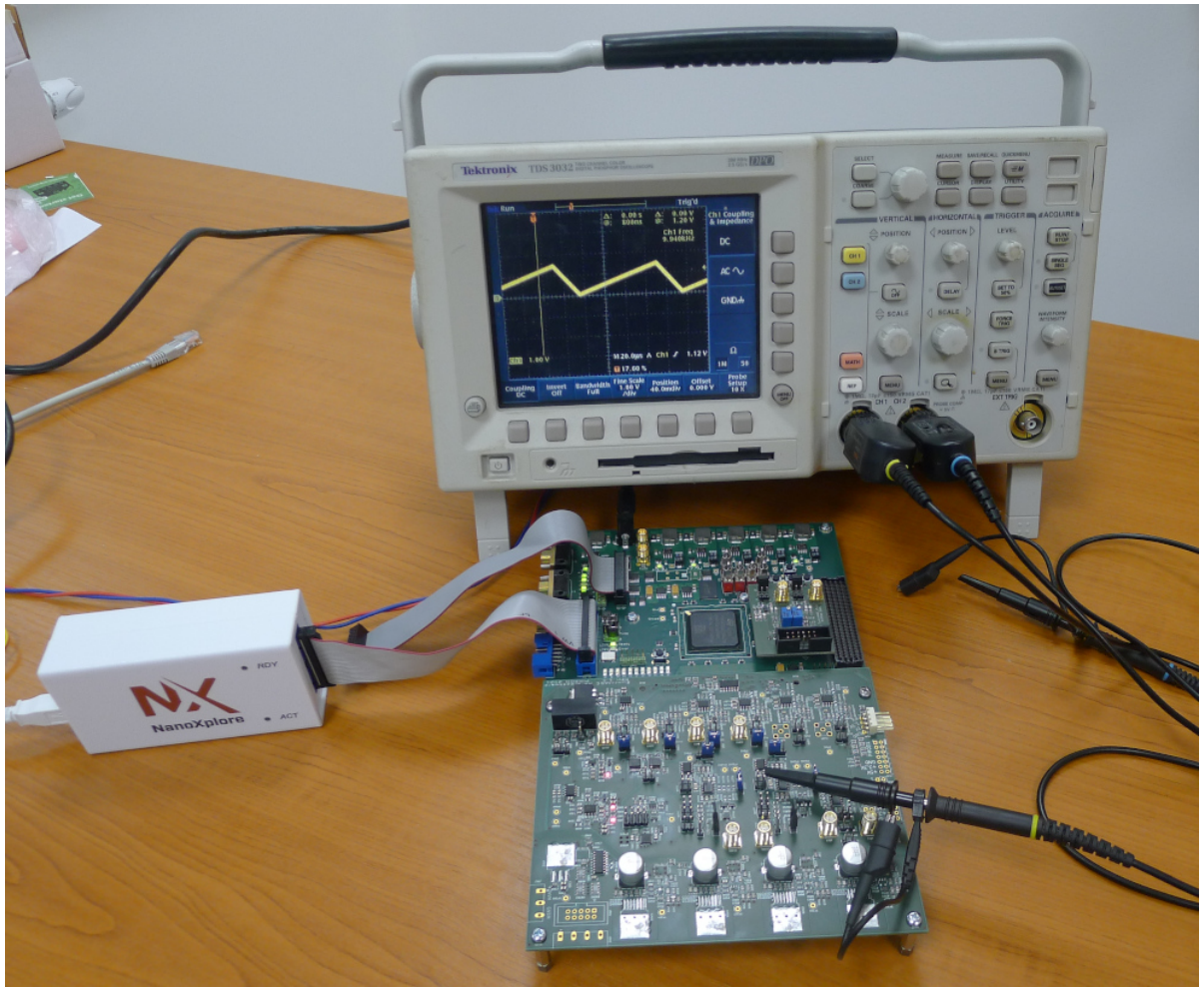
- ADA4084-2S VCC 3V to 36V, Offset Voltage typ 20µV, max 100µV, but up to 400 nA input bias at +125°C, declared as rail to rail, fast recovery and comparator, but it clamps inputs over diodes together, declares CMRR @3VDC single supply from 0 to 3 VDC, but according to graph deterior/misbehaves till 1.2 VDC (MCP6021 input bias curret 640pA @+125°C, max 5,000 pA
- ISL70444SEH VCC 2.7 V to 40 V, Offset Voltage typ 20 µV, max 500 µV
- RH1499M VCC 4.5 V to 36 V, Offset Voltage typ 200 µV, max 1100 µV
- LMP2012QML-SP Dual, VCC 2.7V to 5V, Offset Voltage typ 0.8V, max 60uV, CFP 10
- *OPA4H014-SEP offset 120 µV max, drift 1 µV/°C, input bias current 10 pA (–55°C to +125°C ±3 nA), equivalents OPA140AIDBVT and OPA140AIDBVR (found late)*

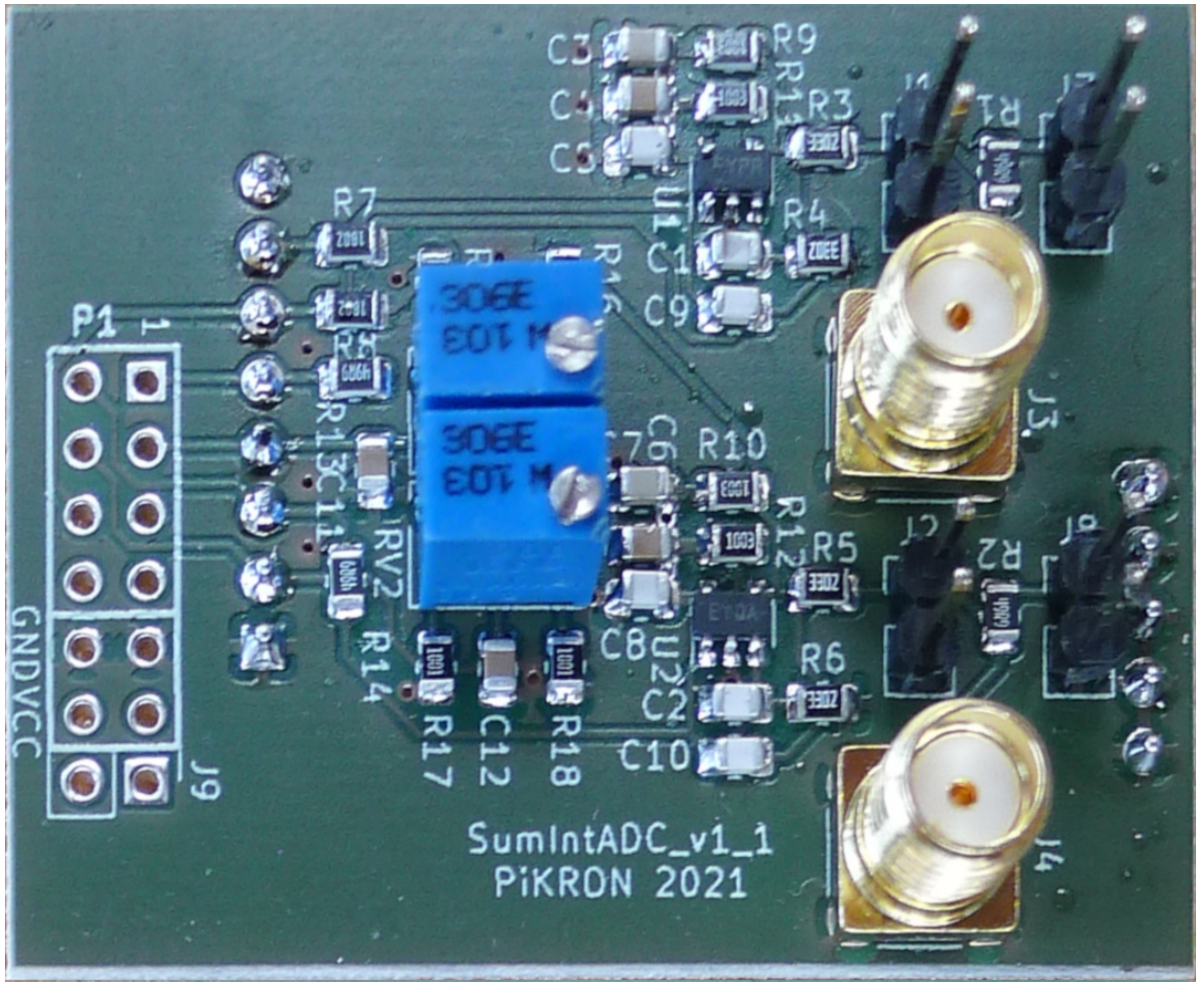
The Idea Based on LX_RoCoN



- The complete design schematics and fabrication data in the project repository: simple_adc_cmp_lvds/SumIntADC_v1_1

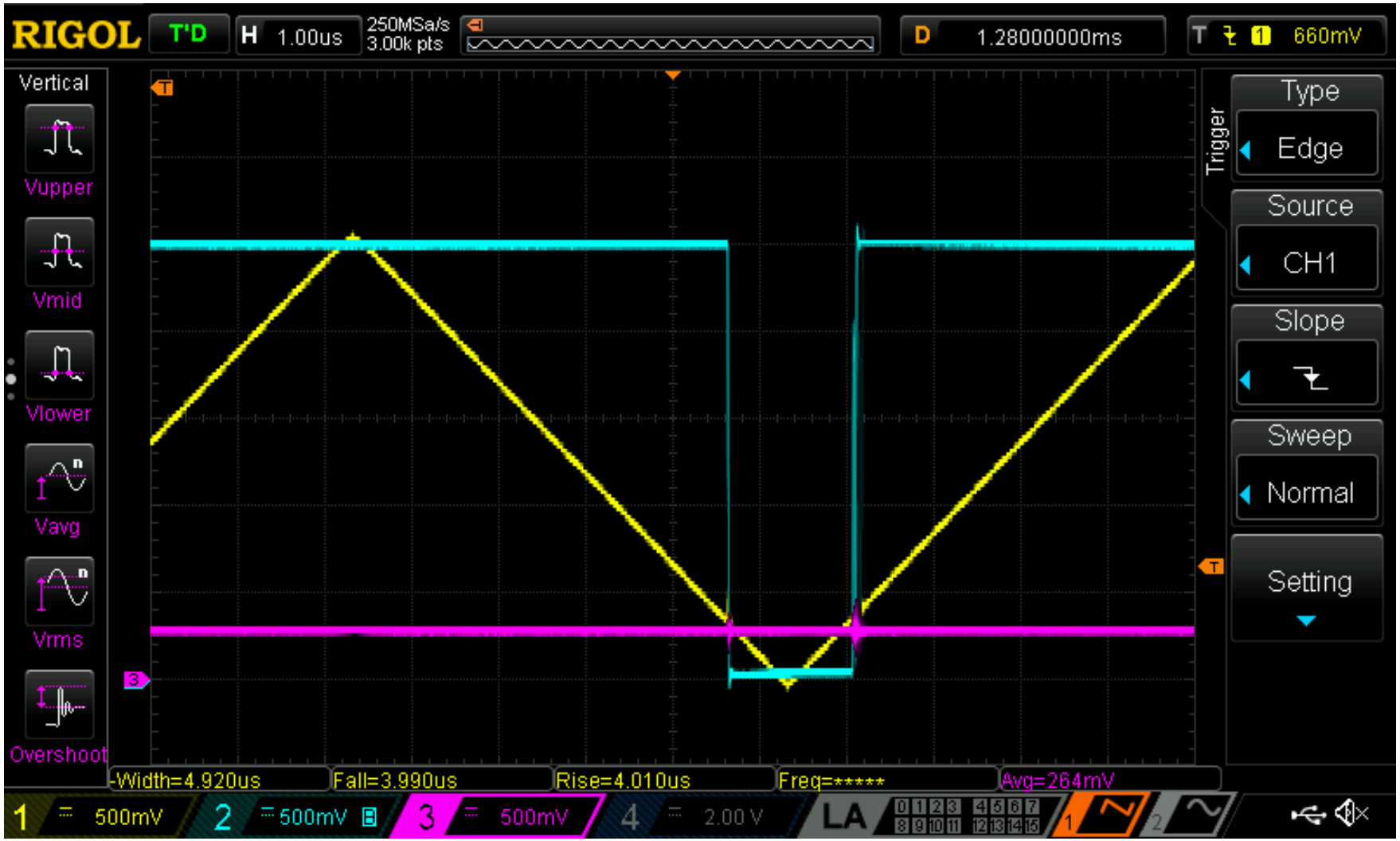
SumInt ADC Char. – Test Board 1 Realization





Reference directly by NX FPGA bank, integrator ADA4084 , comparator NX pins in LVDS mode

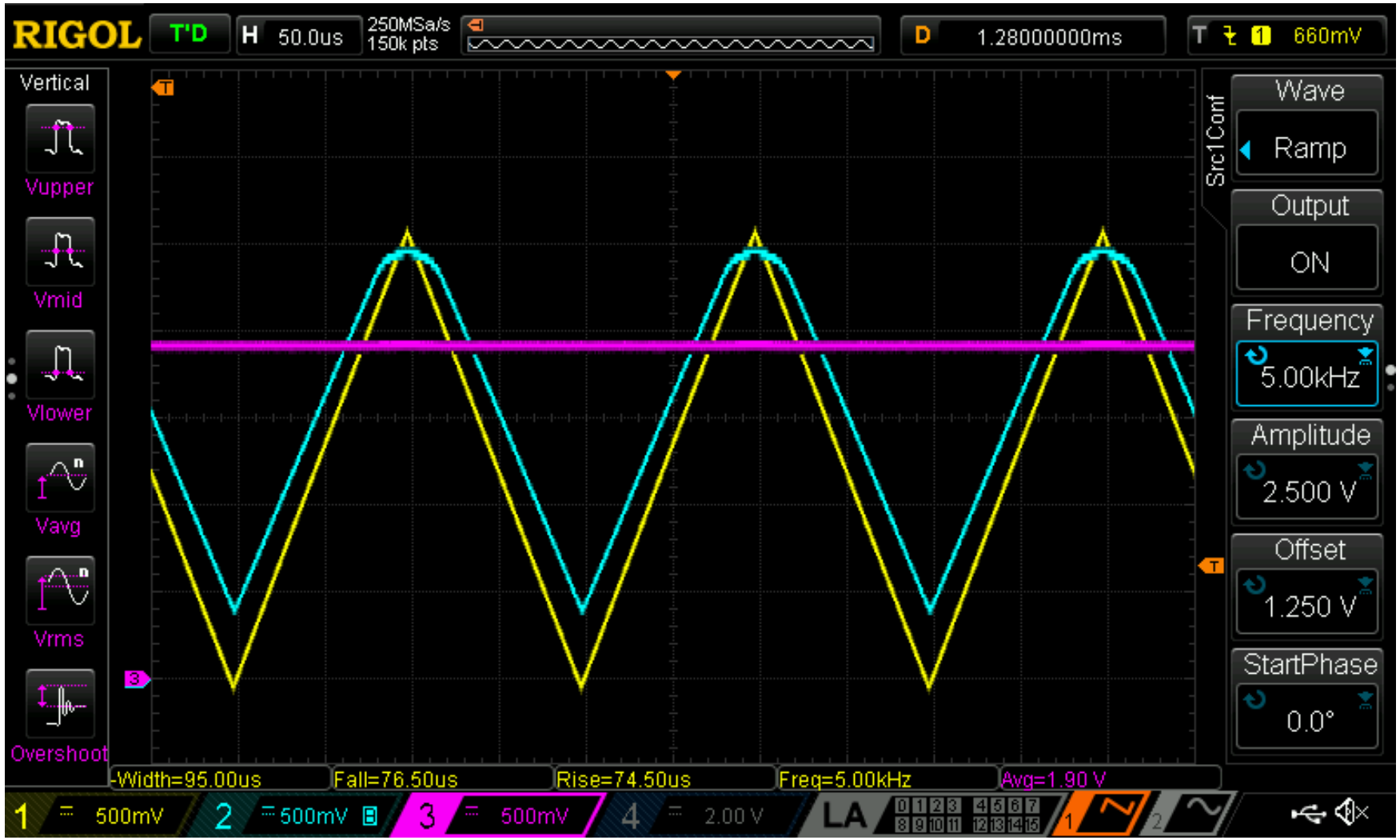
NanoXplore LVDS Pins Assessment



- Pos. triangle, 100 Ω / 10k Ω
- Neg. potentiometer
- LVDS termination is off, no influence to triangular signal
- 0.2 to 1.9 VDC, OK
- Safe: 0.5 to 1.5 VDC
- without flip flop, oscillation

100 Ω pos. source Y, neg. by potentiometer M, out C sumintadc-char/lvds-check

NanoXplore LVDS Pins Assessment



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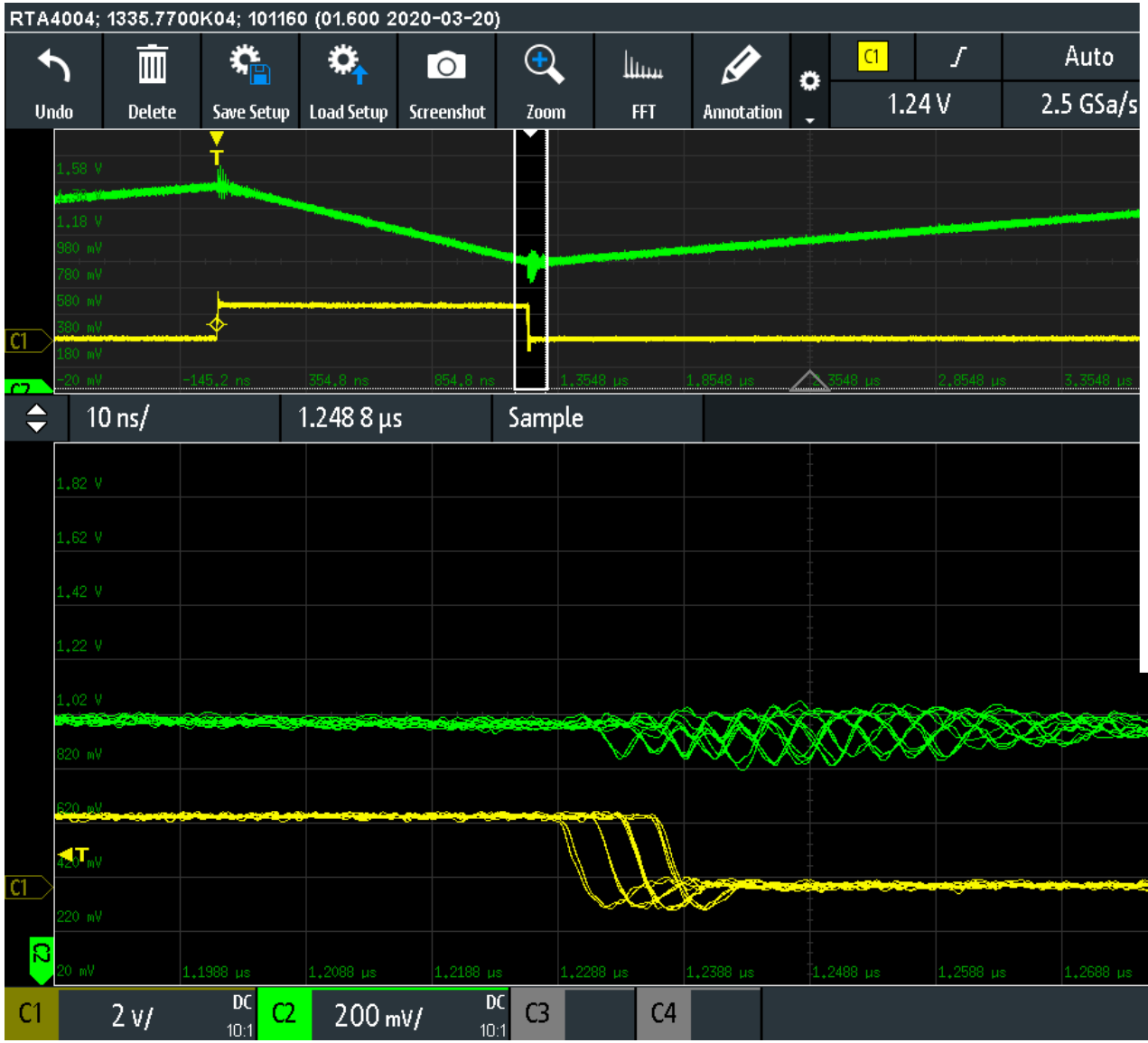
- 0.2 to 1.9 VDC, OK
- Safe: 0.5 to 1.5 VDC
- without flip flop, oscillation

Y before, C after 10 kΩ pos. source, neg. by pot. M sumintadc-char/lvds-check

The Test Board 1 Check

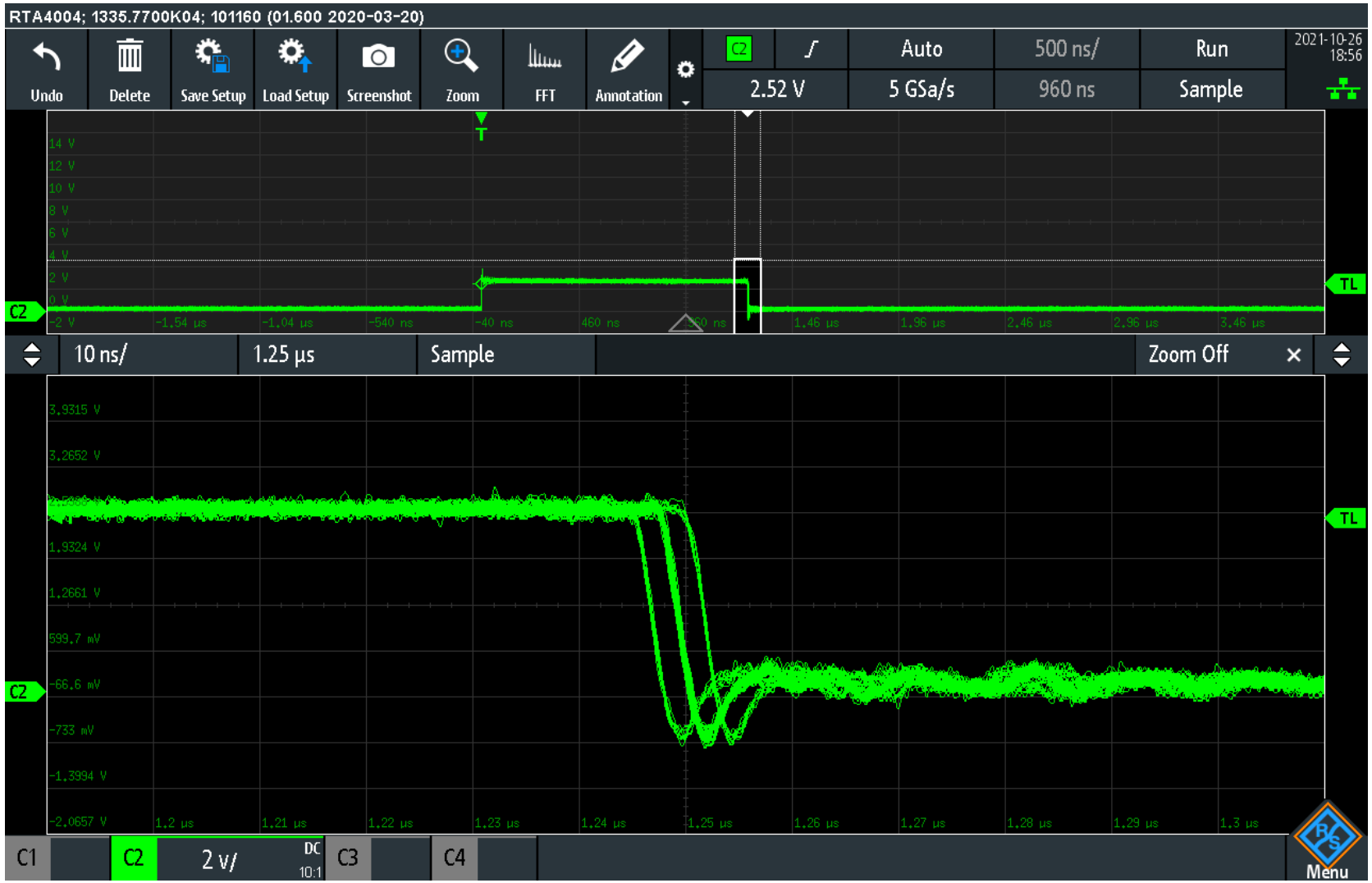


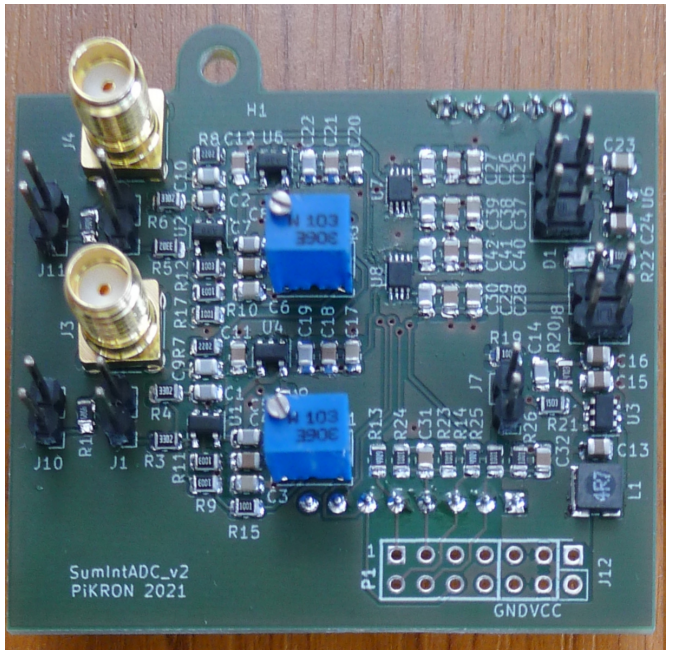
HDL Test Design

- sumint_nx_tp5
- Worked at 400 MHz modulator, 100 MHz logic
- The design taken from lxpwr-agl used on LX_RoCoN

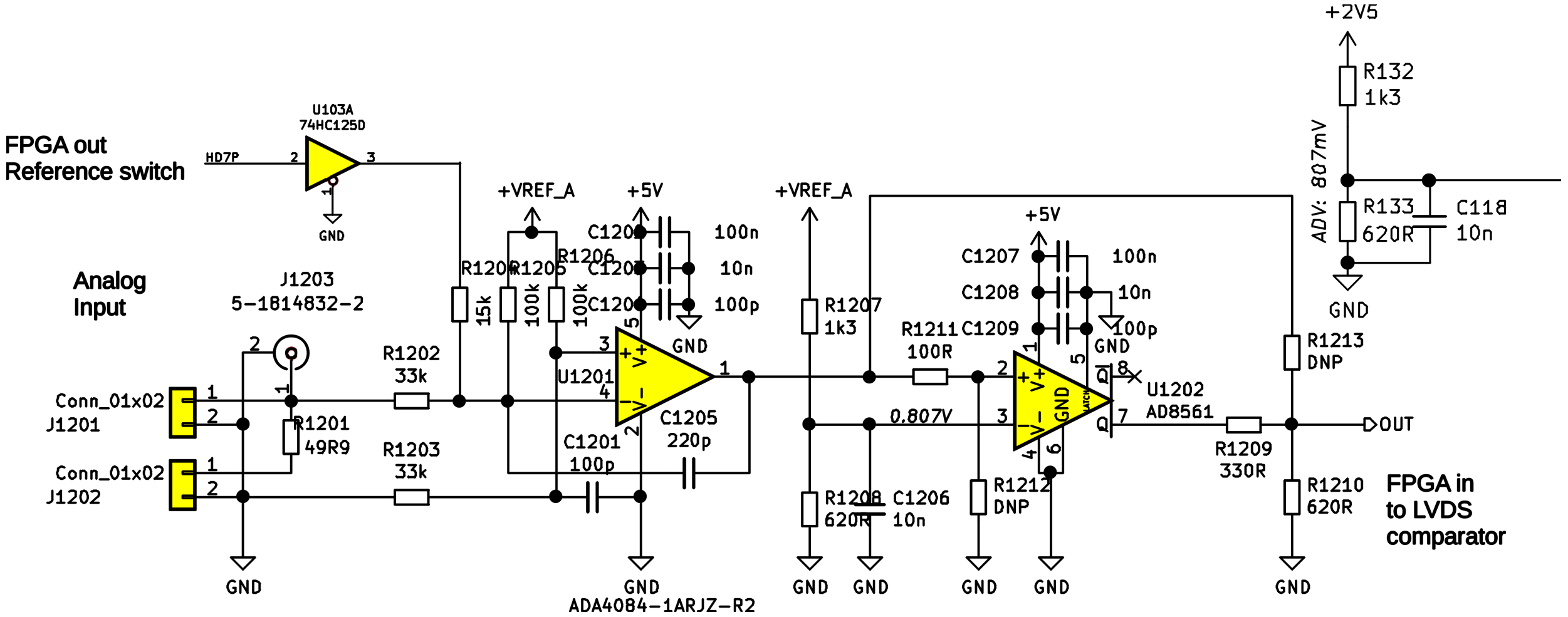
Componet	Lines	Description
pdchain.vhdl	49	pipelined synchronous pulse counter
pdivtwo.vhdl	41	the stage of the counter
siroladc.vhdl	86	sigma-integral rolling ADC digital part
sumint_nx_tp5.vhdl	176	top level test design

The Test Board 2 – REF43, ADA4084, 74HC125, comp



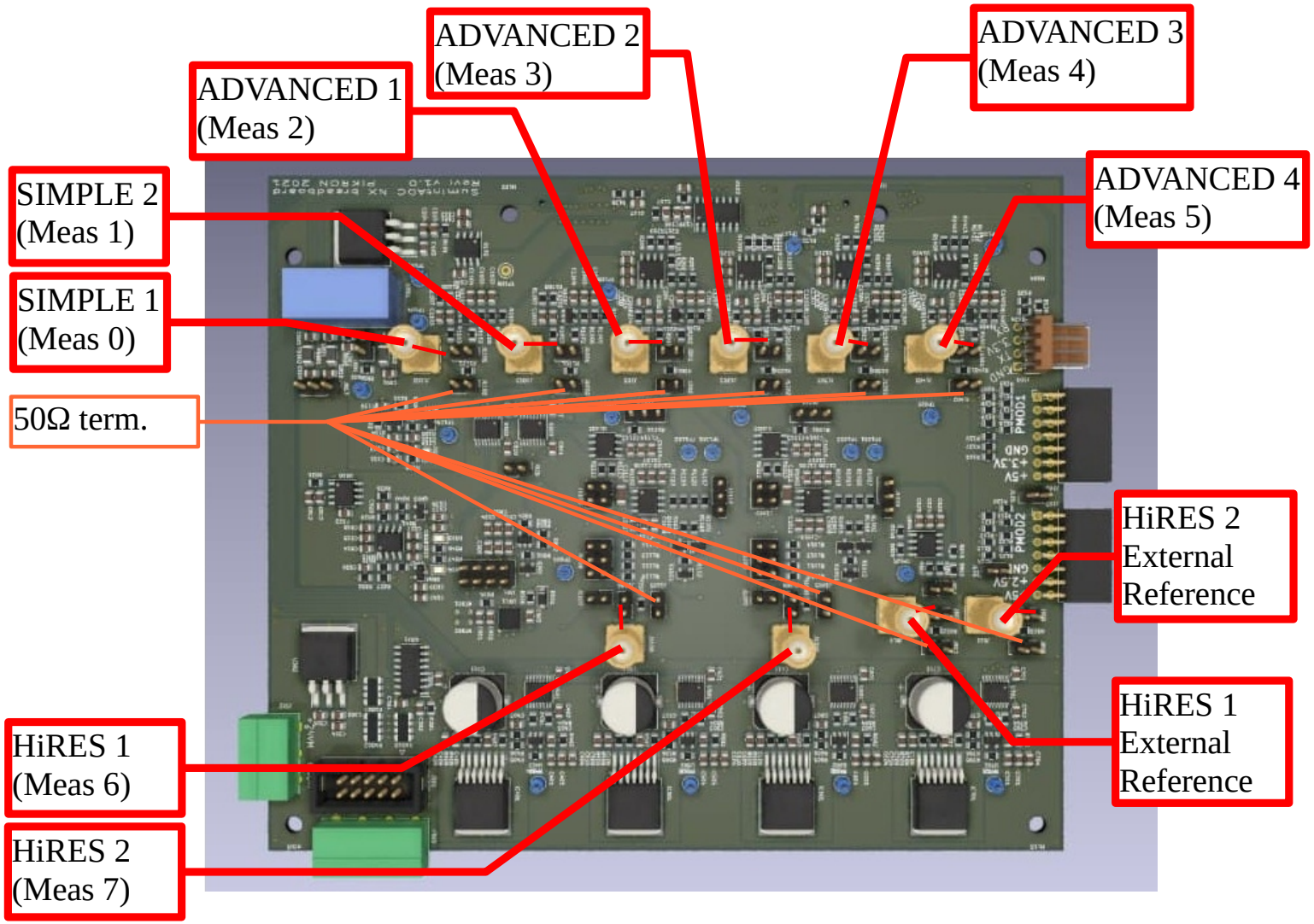


Final Advanced Channel Schematics

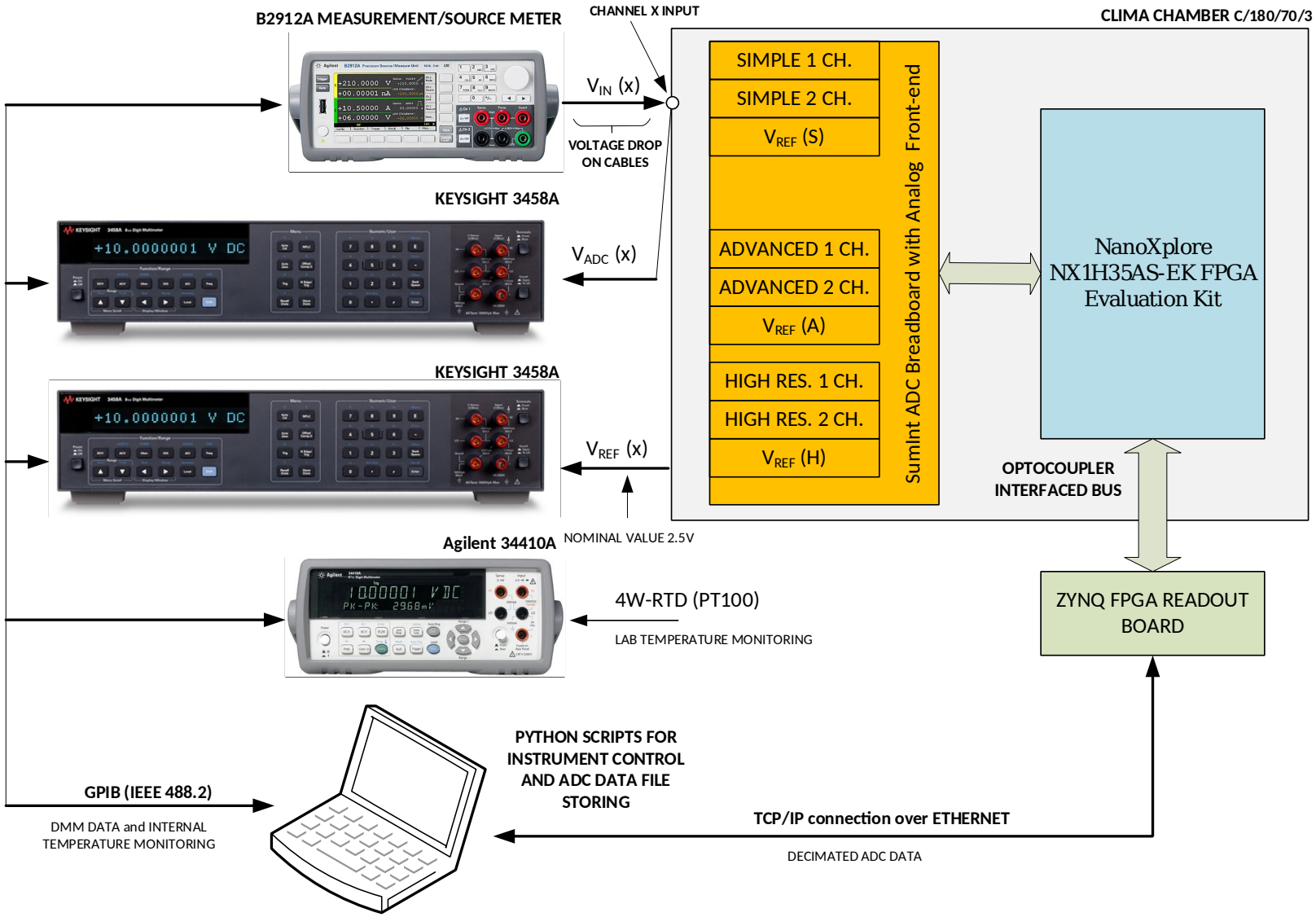


ADA4084-2S integrator , AD8561 comparator, 200 MHz internal nanoXplore PLL (f_{adcclk}), modulator frequency f_{adcmod} = 200 kHz, raw samples $f_{averaging}$ = 4 kHz resolution of ½ f_{adcclk} / $f_{averaging}$, 25000 levels, around 14 bits.

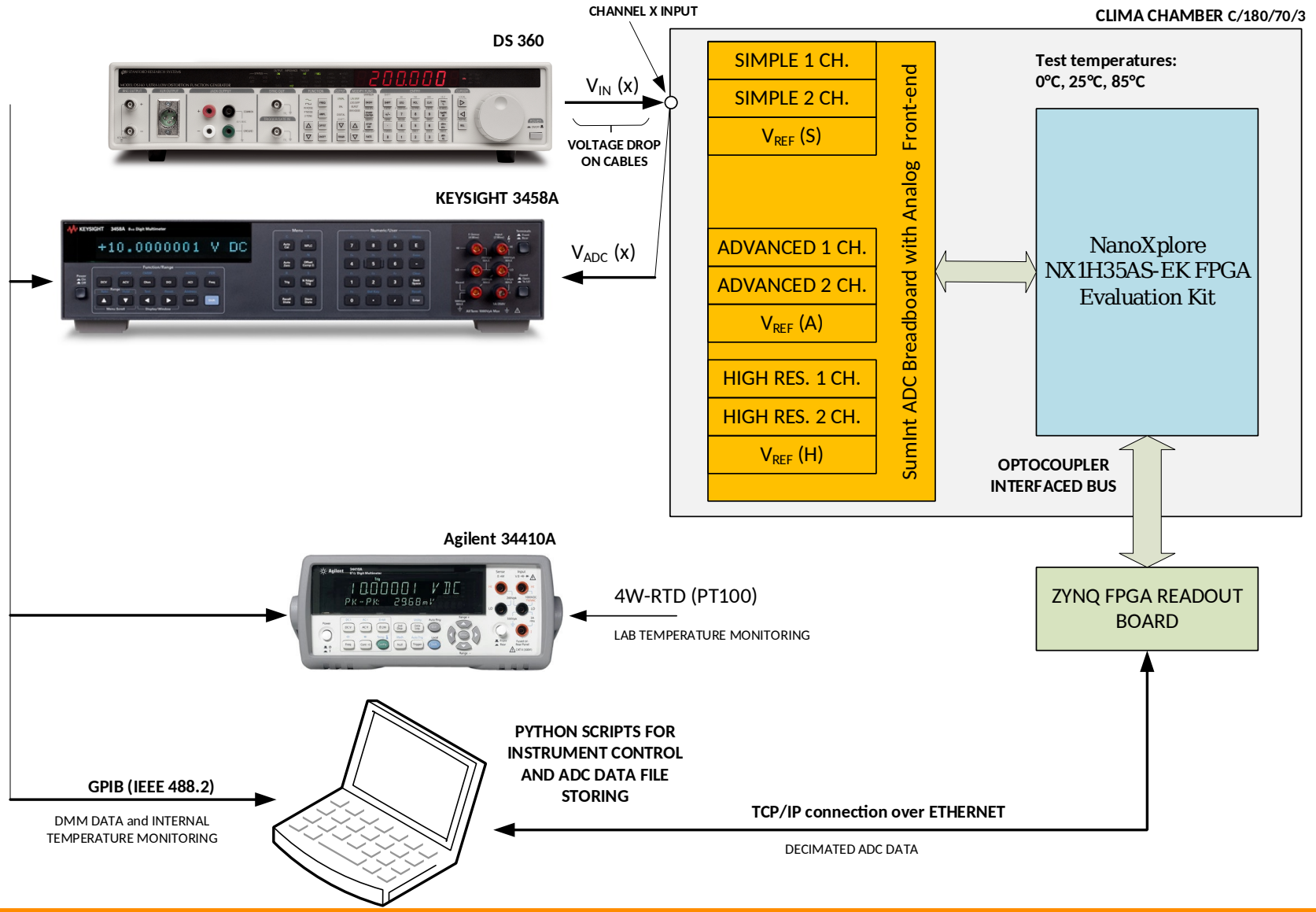
SumIntADC BreadBoard v3 Model



Static Characterization Setup

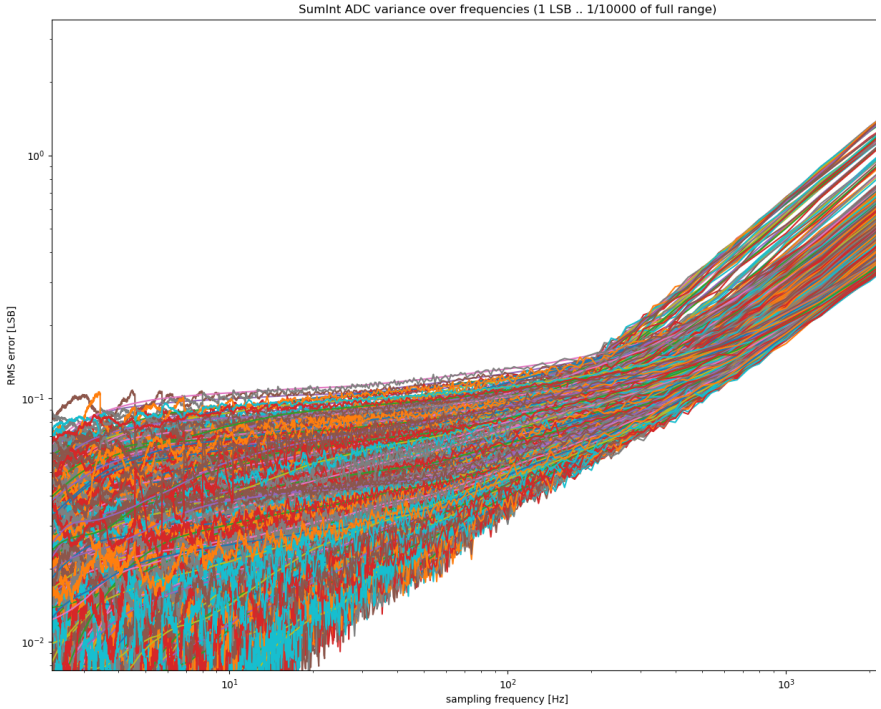


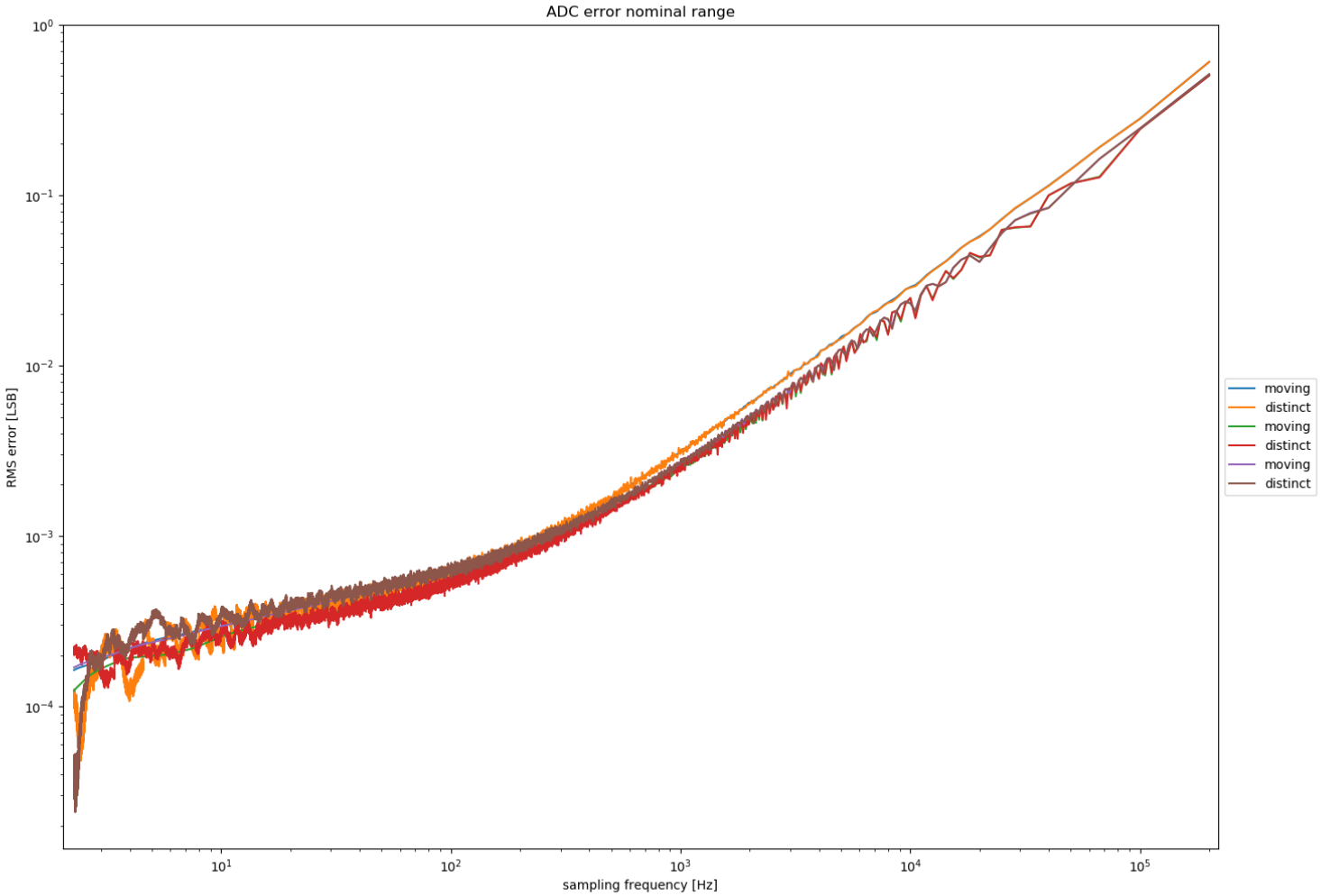
Dynamic Characterization Setup



- harmonic signal excitation
- perform "sinewave fit test"
- frequency: 10 Hz, 15 Hz, 22 Hz, 33 Hz, 47 Hz, 68 Hz, 100 Hz, 150 Hz, 220 Hz, 330 Hz, 470 Hz, 680 Hz, 1000 Hz, 1500 Hz, data for each frequency captured three times
- data processing – evaluation all key parameters (SINAD, ENOB)

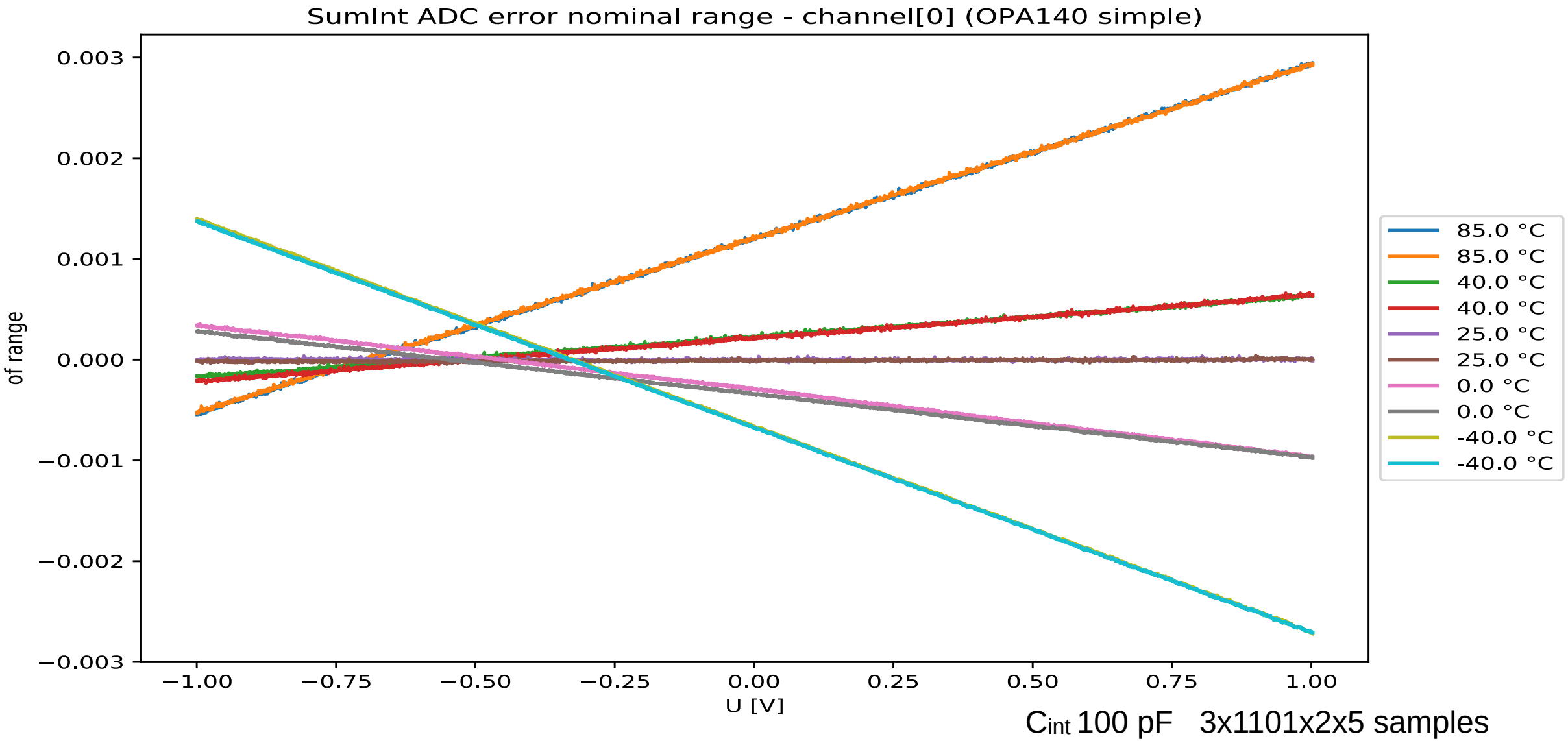
Growth of Resolution with Averaging





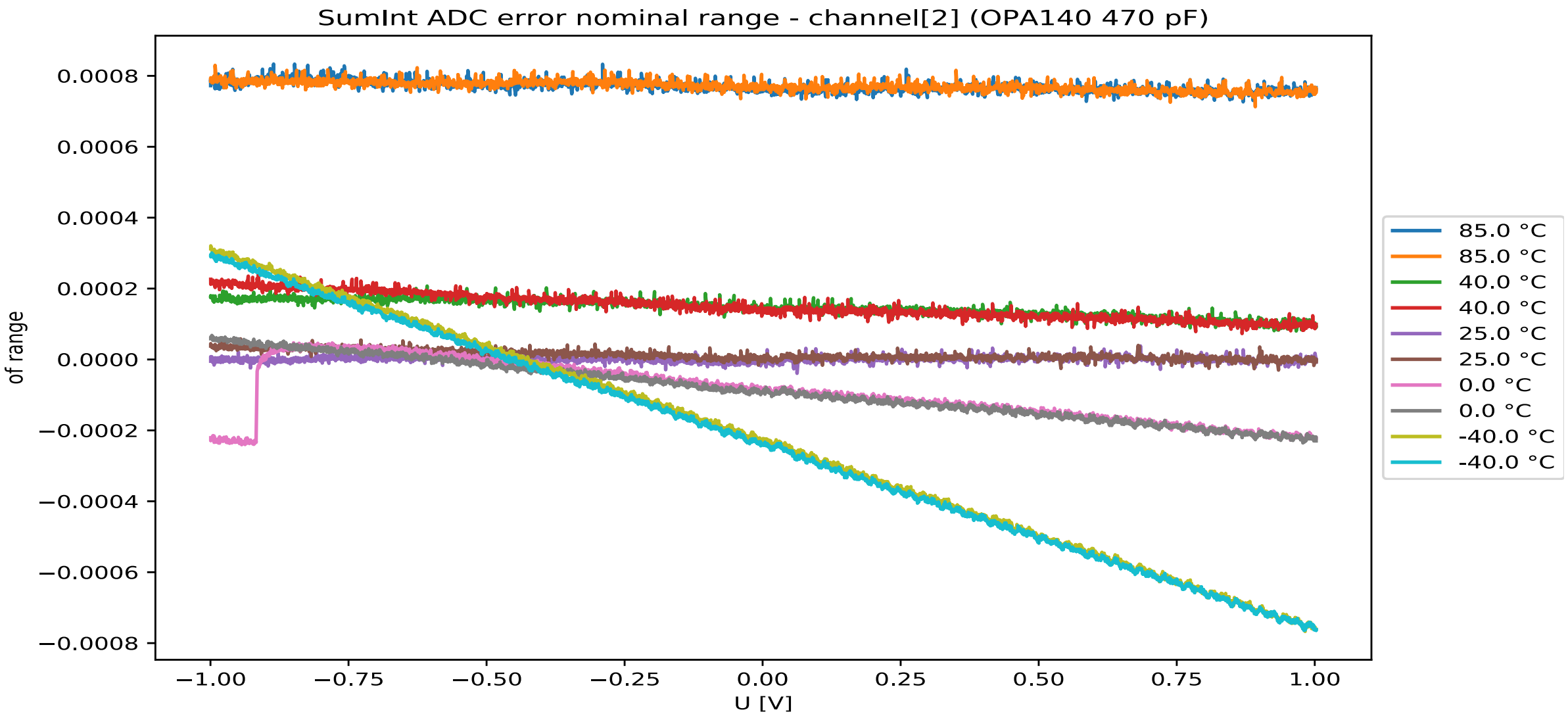
Demonstration of the linear growth of resolution from 200 kHz till 1 kHz

Short Test of OPA140 on Simple 1 (0)



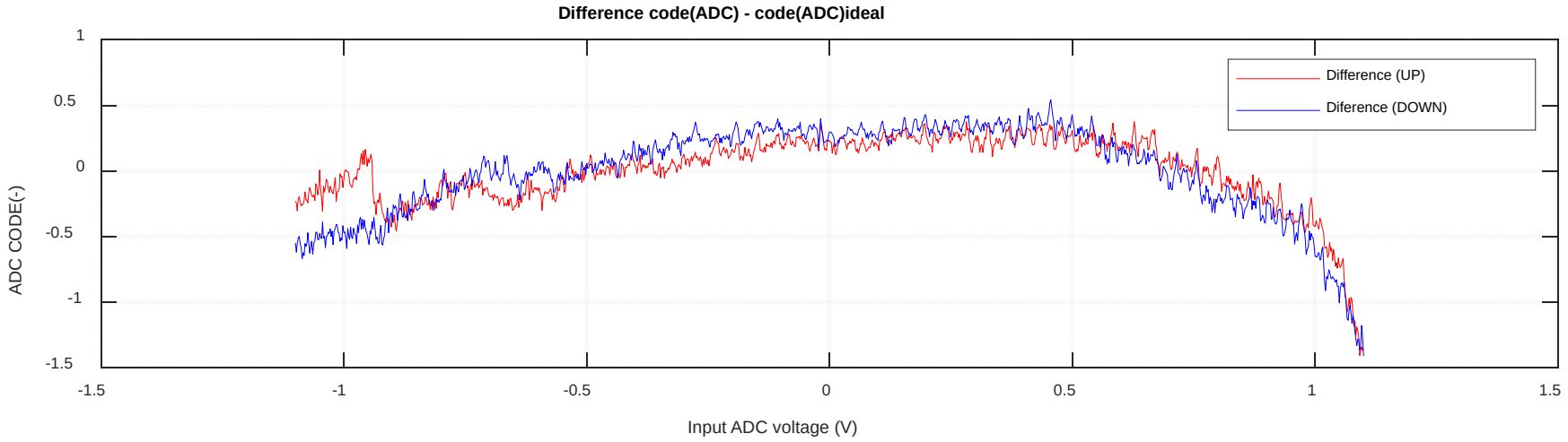
C_{int} 100 pF 3x1101x2x5 samples

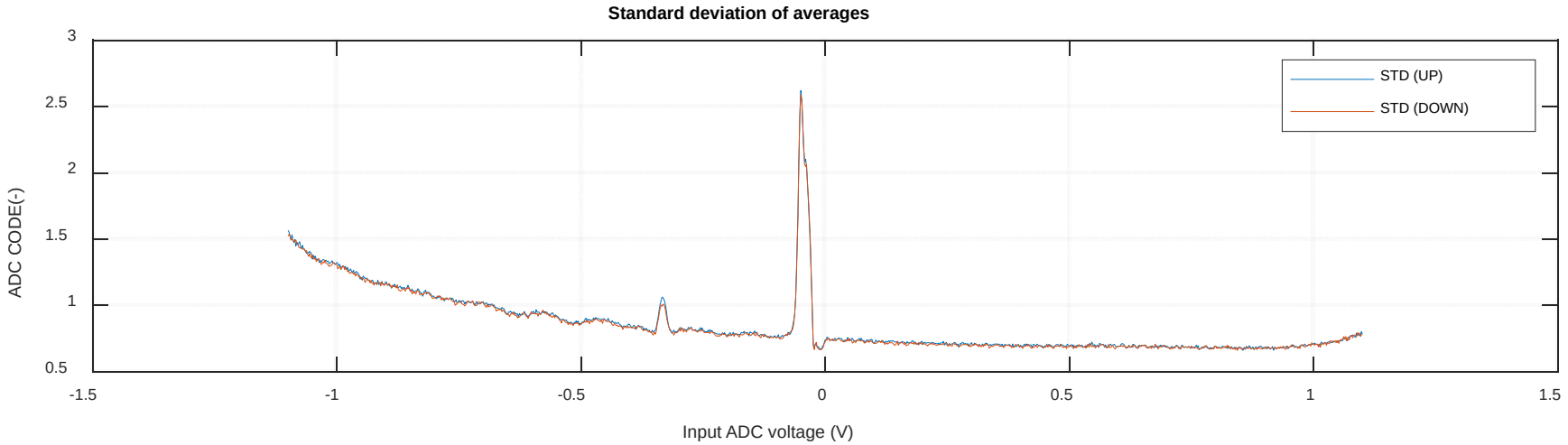
OPA140 Test on Advanced Channel 1



C_{int} 470 pF 3x1101x2x5 samples

Simple Channel Mutual Influence for Same Input Value – Aliasing of Switching Time





Noticed on measurement 1 when blind connected to 0V, can be on NanoXplore LVDS input comparators, outputs or FPGA bank power supply, advanced OK

Advanced Channels Static Characterization

OpAmp type	Linearity at single temp.		Single raw sample at temp		Single raw sample, all temp	
	aver err	raw std	min	max	min	max
1. OPA140 ch2 470 pF	2.51e-04	5.11e-04	-1.09e-03	9.88e-04	-1.24e-03	1.77e-03
1. OPA140 noisy 0 °C removed	5.72e-05	5.11e-04	-1.09e-03	9.88e-04	-1.24e-03	1.77E-03
2. OPA140 ch3 100 pF	5.49e-05	5.10e-04	-1.09e-03	9.68e-04	-3.00e-03	2.90e-03
2. OPA140 blind subs	5.45e-05	5.10e-04	-1.10e-03	9.56e-04	-1.46e-03	1.57e-03
ADA4084	4.62e-05	4.78e-05	-1.78e-04	2.09e-04	-3.60e-03	3.53e-03

ADA4084(-2S) / OPA4H014-SEP Integrator

AD8561 comparator

74HC125 ref. switch

200 MHz internal nanoXplore PLL (f_{adcclk}), modulator frequency

f_{adcmod} = 200 kHz

$f_{averaging}$ = 4 kHz

min and max computed from all 100 mil samples in test

The OPA140 setup 1. uses C_{int} 470 pF, setup 2. C_{int} 100 pF
Values in the table represent ADC error relative to the Full Scale

Simple Chan. – Static Characterization

OpAmp type	Linearity at single temp.		Single raw sample at temp		Single raw sample, all temp	
	aver err	raw std	min	max	min	max
OPA140	5.78e-05	5.17e-04	-1.19e-03	1.10e-03	-3.25e-03	3.84e-03
ADA4084	4.69e-05	1.44e-04	-4.27e-04	4.70e-04	-2.68e-03	6.45e-03

Values in the table represent ADC error relative to the Full Scale
min and max computed from all 100 mil samples in test

ADA4084(-2S) / OPA4H014-SEP Integrator

NanoXplore pins in LVDS mode as comparator

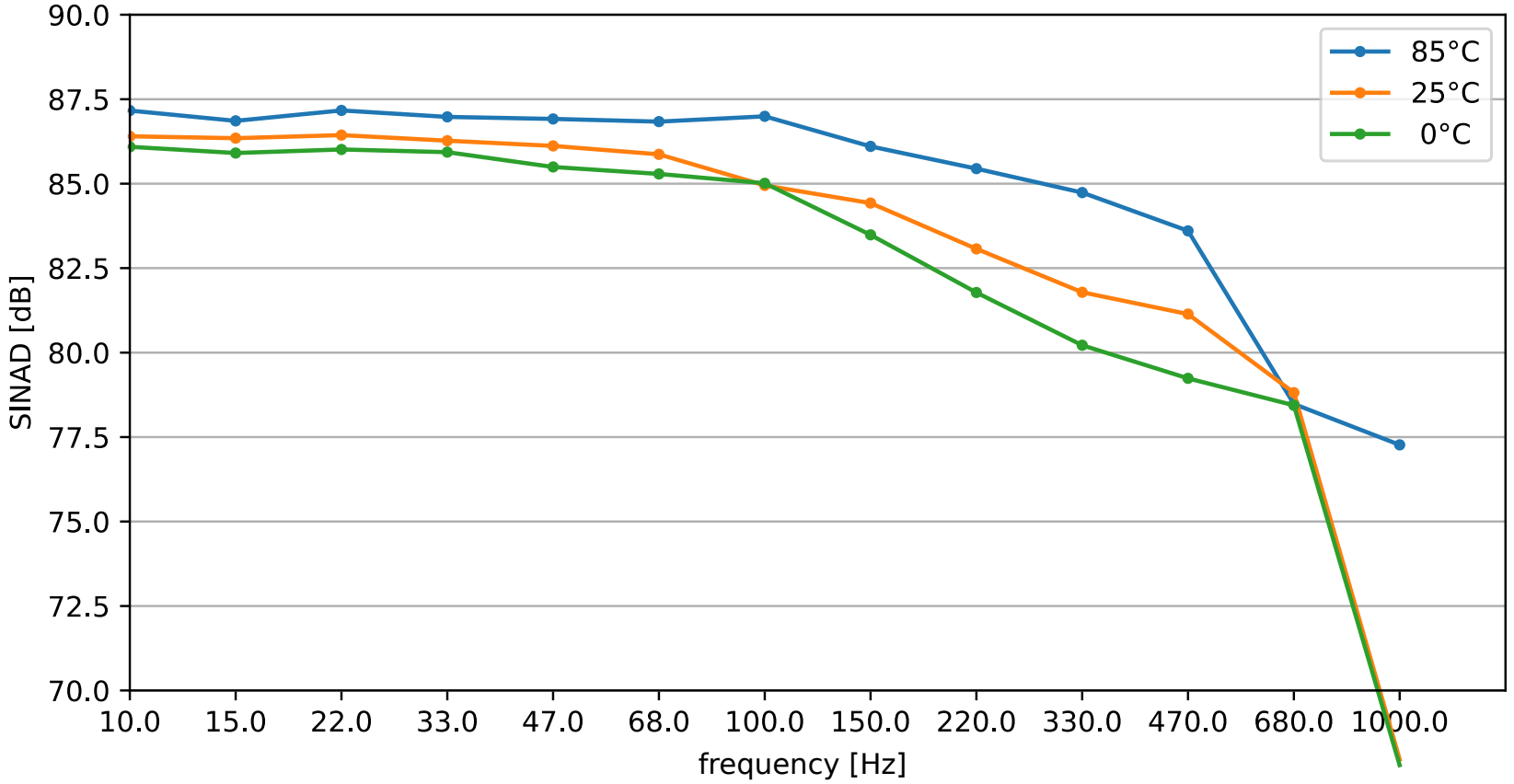
reference volatge from nanoXplore and single ended output

200 MHz internal nanoXplore PLL (f_{adcclk}), modulator frequency

f_{adcmod} = 200 kHz

$f_{averaging}$ = 4 kHz

Results of Dynamic Testing



- Advanced Channel, on ADA4084 only for now
- The sine fitting modified to take non-equidistant sampling
- Value computed by from ref+ divided by individual sampling intervals
  x_val = 2*Tclk*x_samp[2:end]./(Tsamp .+ Tclk*(x_subs[2:end] - x_subs[1:end-1]))

Dynamic Characterization Summary

- ADC input excitation – a harmonic signal, constant amplitude close to the full range
- frequencies 10, 15, 22, 33, 47, 68, 100, 150, 220, 330, 470, 680, 1000 Hz
- Raw data, no floating sampling interval accounted, resolution unusable.
- When SumInt principle accounted:
- SINAD for the advanced > 78 dB up to 680 Hz, SINAD > 85 Hz up to 100 Hz.
- simple (on FPGA pins) SINAD > 80 dB till 100 Hz, lower to 75 dB at 680 Hz
- actual integrating character is not modeled during fitting – for integration applications can provide even better results
- ENOB = (SINAD_dB – 1.76)/6.02
- resolution in range between 13 and 14 bits is confirmed.
- from previous quantization noise is suppressed by factor 1/n for given setup from modulator frequency down to the area about 1 kHz where curve switches to the standard $1/\sqrt{n}$ slope

References/Links

- PiKRON.com: Spectrophotometric detector LCD 5000 – User manual
  http://pikron.com/pages/products/hplc/lcd_5000.html
- P. Píša, P. Porazil, Σ-Integration analog to digital converter, Idea, implementation and results, IFAC Proceedings Volumes, 2005, 38.1: 85-90., 16th World Congress of the International Federation of Automatic Control
  https://www.sciencedirect.com/science/article/pii/S1474667016372056
- PiKRON LX_CPU board documentation and schematics
  https://www.pikron.com/pages/products/cpu_boards/lx_cpu.htm l
- PiKRON LX_RoCoN motion controller system documentation
  http://www.pikron.com/pages/products/motion_control/lx_rocon.html
- nanoXplore BRAVE NG-MEDIUM FPGA and NX1H35AS-EK evaluation kit
  https://www.nanoxplore.com/
- XilinX Zynq MZ_APO education kit
  https://cw.fel.cvut.cz/wiki/courses/b35apo/en/documentation/mz_apo/start
- PiKRON SumInt ADC GitLab project
  https://gitlab.com/pikron/projects/sumintadc