Implementation and Evaluation of Sum-Int ADC IP-core on NanoXplore FPGA

PISA, Pavel (PiKRON, s.r.o.); PORAZIL, Petr (PiKRON, s.r.o.); LADMAN, Jakub (PiKRON, s.r.o.); LEVACQ, David (ESTEC); PECA, Marek (ESTEC); SEDLACEK, Radek (Czech Technical University in Prague); SPACEK, Michal (Czech Technical University in Prague)

***Abstract*—The summing integration (SumInt) analog to digital conversion (ADC) technique combines and preserve many of excellent features of double integration and sigma-delta ADCs. It is well suited for application where integral of continuously sensed input signal carries information to acquire. It has been initially conceived at the PiKRON company for digitizing compounds responses measured by UV-VIS spectrophotometric detectors in high-performance liquid chromatography systems. The compound concentration in the sample is proportional to the integral/area under response peak. In a contrast to double integration ADC, the SumInt ADC integrates input signal continuously and does not require reset/idle interval control. In comparison to sigma-delta ADC, the frequency of reference switching is much lower (less charge leakage). The paid price is sampling interval floating in a range of up to one half of the fixed modulator interval. The actual ESA funded De-Risk project focuses on reuse of the technique for low analog components count conversion in radiation tolerant systems where FPGAs are already in use.**

I. Introduction

An original architecture of Analog-to-Digital Converter (ADC) has been conceived by the designers, which is suitable for low-frequency signal conversion. The design is mostly digital and well suited for FPGA implementation. The design is able to replace dedicated middle resolution and high-precision ADC component(s) with the FPGA IP core, having comparatively small and simple external circuitry (op-amps), simpler, cheaper and more mature than ADC ICs. The design is thus well suited for applications, where the FPGA is needed for other purposes – which are however becoming a majority in space equipment. Moreover, there are some unique distinguishing features of the ADC, yielding a remarkable performance, while maintaining implementation simplicity.

The conversion principle is used already for two decades in PiKRON company precise analytical HPLC instruments designs [1]. The precise analog front-end in combination with FPGA is used in these applications where resolution 19 bits at 25 Hz with no overlap between samples is used. Design allows to enhance resolution to 22 bits with simple moving average. The design analysis, usable input range, stability and properties of the converter are demonstrated in [2] by histograms from data acquired over 300 seconds.

The design has been later used for motion control applications where resolution of 12 bits at 20 kHz sampling frequency has been obtained. The unique achievement of this redesign has been direct use of FPGA (Microsemi AGL250 in particular) digital input and output pins to realize comparator and reference voltage sources in this case. This has been possible thanks to high tolerance of the design to comparator treshold uncertainty.

II. SumInt ADC Concept and Applications

A. Analog Front-End and Digital Modulator

The input signal is integrated by an operational amplifier and RC network in classical inverted integrator circuit. The value contributed by instantaneous input signal integration is balanced by addition of the signal provided by analog switch which switches between two levels of the reference signal. These levels are laeled for simplicity as positive and negative reference and are usually obtained from and single precise stable reference or for ratio conversions from filtered (quasistational) reference signal by its negation and attenuation. Integrator virtual ground reference point offset given only by resistor network is enough for simple use cases and then only single active analog component per channel (operational amplifier in integrator circuit) is required. For precise conversion as used in a LCD 5000 HPLC spectrophotometric detector, more components are used and whole analog front end is galvanically isolated from a digital logic by one Tx and one Rx fast digital optocoupler as shown in Fig. 1. The original design has been based on 8-bit 8051 based microcontroller (SAB-C509-LM) and Xilinx XC3064-PQ160 FPGA. The ADC time-quanta frequency was given by a crystal oscillator (f_{adcclk} = 32 MHz), modulator frequency f_{adcmod} = 5 kHz and measured/decimated raw samples $f_{averaging}$ = 25 Hz.

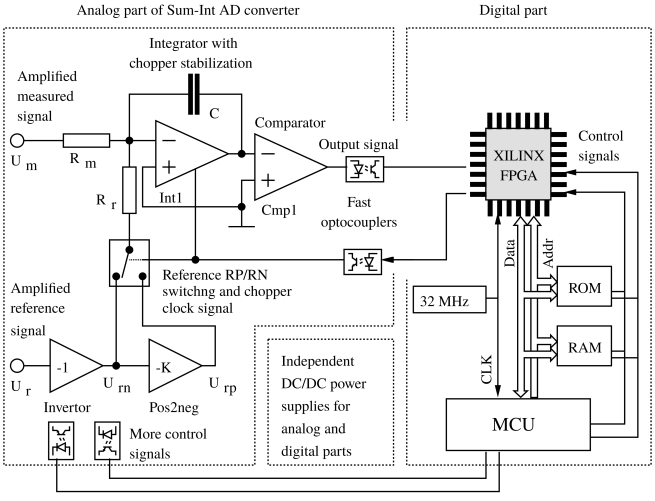

Fig. 1. Original SumInt ADC design for LCD 5000

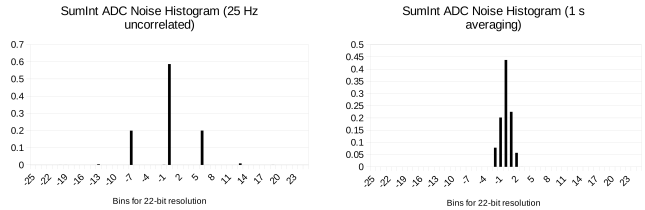

Fig. 2. LCD 5000 SumInt ADC quantization at artificial 22-bit resolution

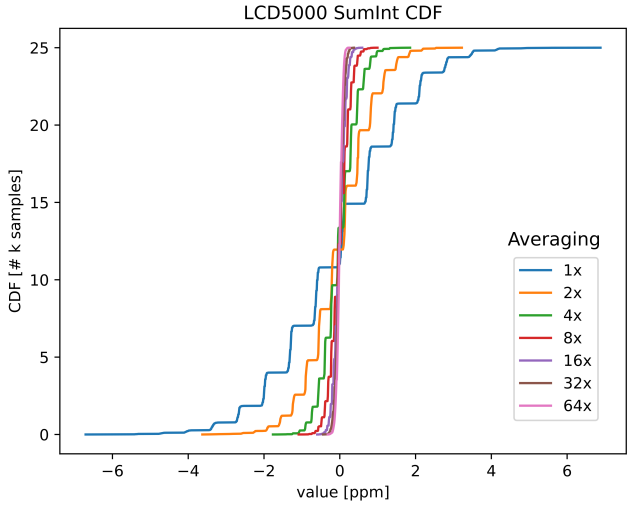

Fig. 3. Cumulative distribution function of null input on LCD 61 HW

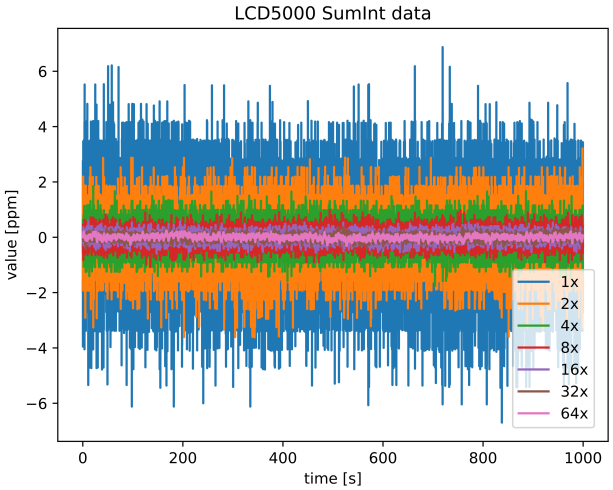

Fig. 4. Null input data used for CDF computation, 1000 s each

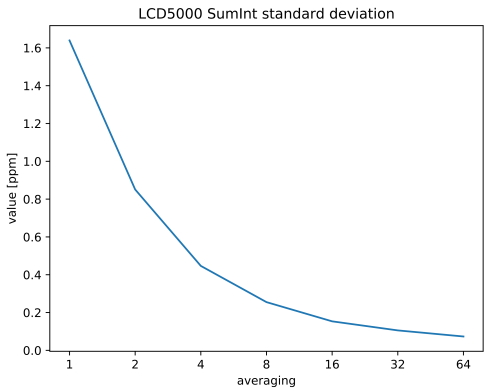

Fig. 5. Null input standard deviation from 0.04 to 2.54 s averaging 1 to 64

B. *Performance in HPLC Applications*

The original design performance is demonstrated in Fig. 2 by analysis of the null/zero inputs signal noise over 300 seconds. Raw data delivered at 25 Hz are quantized into bins equivalent to 22-bit ADC resolution. Count of time quanta ($1/f_{adcclk}$) when positive reference signal is applied are accumulated over averaging period ($1/f_{averaging}$). That gives 128 10^6 possible levels but as discussed in [2], only little less than half of that range corresponds to the modulator stable region. This roughly corresponds to 2^{19} levels into which uncorrelated raw samples are distributed. But mechanism to propagate remainder error into next conversion cycles allows to enhance resolution at the price of moving averaging with better noise suppression than $1/\sqrt{n}$ given for standard n independent samples with normal distribution of noise. In the fact, this continuous error summation and balancing allows to enhance resolution with 1/n noise quantitation suppression in large range till the point where clock jitter, reference noise and operation amplifiers input offsets, and input current levels and variations prevails.

The original high resolution implementation compensates for operational amplifier input offset influence by use of the chopper stabilized Texas Instruments TLC2652 precision operational amplifiers. The chopper signal is derived from the ADC modulator cycle signal to suppress possible effect of aliasing of independent chopper oscillator and period with the ADC conversion cycle.

The hardware of LCD 5000 detectors has been innovated. Analog front-end has been preserved but the rest of the electronic has been replaced (the setup code LCD 61). The electronics builds on LX_CPU board based on NXP LPC4088 [3]. The board carries even optional Xilinx XC6SLX9 FPGA but for the SumInt ADC application internal MCU timer with capture and compare units controlling single external J-K flip-flop are sufficient. The base clock has been increased, f_{adcclk} = 72 MHz, rest is modified, modulator frequency f_{adcmod} = 5 kHz and measured/decimated raw samples $f_{averaging}$ = 25 Hz. Sampling interval starts and ends float in range (0, ½ / f_{adcmod}) and actual resolution is given by chosen averaging. That is why concept of bins based on artificial resolution in bits has been replaced by ppm of the full range and acquired data noise is demonstrated in the form of a distribution function in integral/cumulative variant (CDF), Fig. 3, 4, 5.

C. *Analog Modulator Cycle*

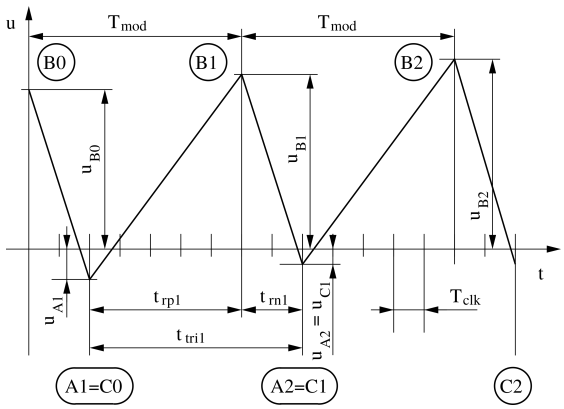

Fig. 6. SumInt ADC modulator cycle

Short list of highlights taken from [2] follows:

- input signal is integrated continuously
- integrator is never reset, no input contribution or short term quantization error is lost
- error/reference unbalanced charge/voltage remainder is preserved as start offset for the next cycle – limited integral error in theory and resolution limited only by number of cycles summed for averaging
- single switching signal between positive and negative reference
- for filtered or slowly changing reference true ratio conversions
- if reference switching latency and charge injection matches for both directions as well as delay in digital signal propagation, then it has no influence to conversion result
- if the reference is applied to the resistor matching by technology and ideally even value to the resistor used for measurement signal and both are located side by side then influence of their resistance change over temperature is suppressed, same for the variance of integrator capacitor parameters over temperature
- if the same analog multiplexer is used in measurements and reference channels than only dependence of it leaking current and resistance change in response to the carried signal value counts, temperature dependency is suppressed
- even slowly changing delay and or threshold value for comparator has no effect on the ADC results
- in a contrast to U → f converter, sampling rate is constant
- modulator frequency can be chosen as arbitrary multiple of time quanta and output averaging, sampling rate as arbitrary multiple of modulator period, this allows to tune parameters, integrator slope rates, level of interleaving for ration conversion etc..

On the other hand there are some critical parameters which contribute to the final resolution and absolute error which has to be analyzed for each applications

- the conversion starts and ends at next quantization clock (f_{adcclk}) period ($A_{i+1}=C_i$) which exact time t_{rmi} is function of input signal value and its change in previous cycles, shift is known, t_{tri} interval time can be computed and average signal level can be computed. But possible exact signal reconstruction has to take into account that only value of signal integral is known and only at points reported by ADC (not equidistant)
- the effect of input offset error, input currents of integrator operational amplifier and their change over temperature and time limits resolution and averaging over multiple modulator periods has no effect on this limit of relative resolution and bias errors
- the reference switching timing jitter and mainly its systematic aliasing with some other signal consonant with modulator frequency degrade resolution, when resolution is enhanced by averaging over n modulator periods, then switching time uncertainty has to be ideally n times smaller than fast quantization clock (f_{adcclk})

III. Low Components Count Implementations

A. *PMSM Winding Currents Sensing with Single Operational Amplifier per Channel*

Many motion control subsystems for laboratory and medical instruments as well as more robotic contd units has been designed at PiKRON. The idea of SumInt ADC has been considered when need for 16 winding current channel control emerged during LX_RoCoN [4] system design. The reverence voltage switching has been realized by dedicated Microsemi IGL00 AGL125 FPGA bank pins. Complete analog front-end consist from single MCP6021T-E/OT operational amplifier per channel, current sensing resistor (20 mΩ), integrator and filtering capacitors and four more resistors. The solution proved stable and is used in production from 2016 year.

B. *Idea to Test Solution on Radiation-Tolerant FPGA*

Because analog components selection for space applications is very restricted and today space applications application usually demand complex digital control often realized by FPGA, idea to reuse some pins of FPGA for auxiliary analog channels realizations s well as use of FPGA together with more complex analog front-end for galvanically isolated high resolution conversion has been considered as good match to previous successful applications of SumInt ADC principle.

The European nanoXplore BRAVE NG-MEDIUM FPGA and NX1H35AS-EK [5] evaluation kit has been selected as target of the experiment. FPGA design is attractive for its simplicity and actual modulator stream has been routed to Xilinx Zynq based MZ_APO education kit [6] for logging and further experimental processing in software.

The components selections and hardware design has been hit by world wide chip crisis which made selection of the components from narrow list of qualified ones even more difficult.

The Analog Devices ADA4084-2S operational amplifier was suggested as possible solution for simple SumInt ADC solution Parameters: VCC 3V to 36V, Offset Voltage typ 20µV, max 100µV, but up to 400 nA input bias at +125°C, declared as rail to rail, fast recovery and comparator, but it clamps inputs over diodes together, declares CMRR @3VDC single supply from 0 to 3 VDC, but according to graph deterior/misbehaves till 1.2 VDC (compare to MCP6021 input bias curret 640pA @+125°C, max 5,000 pA).

The final evaluation breadboard design has been adapted according to the measurement and adjustment on initial experimental partial prototype PCBs. The simple version uses directly FPGA bank pins as the source of switched reference signal and input comparator is realized on pair of FPGA pins configured for LVDS input mode.

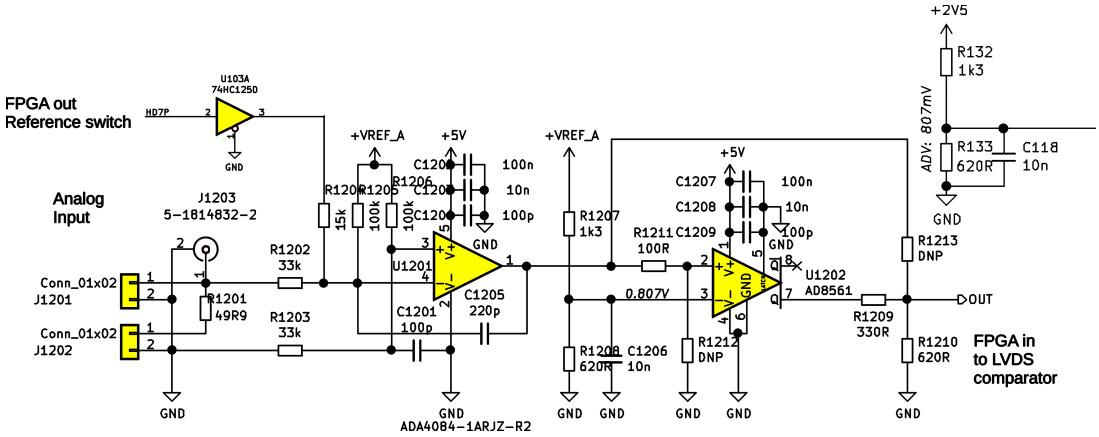

Fig. 7. Advanced SumInt ADC channel analog front-end for NX1H35AS

Advanced version of the solution without galvanic isolation has been realized again by commercial chip equivalent of ADA4084-2S. As reaction to found misbehave of ADA4084 in comparator function, the AD8561 has been used as comparator as shown on Fig. 7.

200 MHz internal nanoXplore PLL has been used as source of logic and time-quanta clock (f_{adcclk}), modulator frequency f_{adcmod} = 200 kHz and measured/decimated raw samples $f_{averaging}$ = 4 kHz. Raw samples resolution of ½ f_{adcclk} / $f_{averaging}$ has been expected, 25000 levels, around 14 bits.

The high resolution version with Texas Instruments TI LMP2012MA (equivalent of a qualified LMP2012QML-SP) operational amplifiers used for integrator and Analog Devices AD8561(S) comparators with ISOS141-SEP digital insulators has been added to the design for proof of concept experiment. Because no suitable space qualified analog multiplexers has not been found, analog reference (another LMP2012MA conditioned REF43/REF43S) switch has been designed from discrete N and P type MOSFETs.

IV. Evaluation and Characterization Results

Laboratory of Precise Electrical Measurement of Czech Technical University has been contracted to process characterization on a professional equipment.

A. *Static Characterization of Simple and Advanced Channels*

Used method: direct comparison of the tested A/D converter with the reference voltmeter Keysight 3458A. Another one used for SumInt ADC board reference voltage monitoring. The measurement/source unit Keysight B2912A provided source of testing DC voltage. Climate chamber, type ClimaEvent C/180/70/3, provided temperature controller for SumInt ADC breadboard mounted on NanoXplore FPGA kit. The data stream has been delivered to the MZ_APO education kit over digital insulators.

The nominal input rage -1.0 to +1.0 VDC has been divided to 1001 points and range has been extended to -1.1 to +1.1 VDC to check safe/monotonic behavior of the converter for signals over nominal range. The measurement has been taken for 5 temperatures: -40 °C, 0 °C, 25 °C, 40 °C and 85 °C. For temperature, 1101 points voltage sweep up and down was processed and for each point three samples taken.

The each sweep data has been processed individually and error against calibration obtained by linear regression has been obtained for average from captured SumInt ADC 4 kHz data-stream consisting of 3495 raw samples (length limited by DMA setup on XlinX Zynq capturing 200 kHz data-steam for 6 channels in parallel). Then absolute maximal error of all 100 millions of raw 4 kHz data was computed against calibration of the given channel at 25°C. Parameters from the one of the two sweeps at 25°C with lower error has been used. The whole instruments setup has been orchestrated by Python program running on PC communication with instruments over GPIB and obtaining SumInt ADC preprocessed data from the MZ_APO over TCP.

The visualizations and analysis proved that the ADA4084 operational amplifier input current dependency on temperature is the main contribution to observed static errors over temperature. This was know to be problematic parameter from the design time. But the new promising operational amplifier from the Texas Instruments with space qualification has been introduces by start of 2022 year – OPA4H014-SEP input offset 120 µV max, drift 1 µV/°C, input bias current 10 pA (–55°C to +125°C ±3 nA).

Texas Instruments provided confirmation that OPA140AIDBVT and OPA140AIDBVR are commercial equivalents of the chip. But due to chip crisis it took longer time to obtain limited number of samples in the package suitable for the bread board design.

TABLE I. Advanced SumInt ADC Characterization Results

OpAmp type	Linearity at single temp.		Single raw sample at temp		Single raw sample, all temp	
	aver err	raw std	min	max	min	max
1. OPA140	2.51e-04	5.11e-04	-1.09e-03	9.88e-04	-1.24e-03	1.77e-03
2. OPA140	5.49e-05	5.10e-04	-1.09e-03	9.68e-04	-3.00e-03	2.90e-03
ADA4084	4.62e-05	4.78e-05	-1.78e-04	2.09e-04	-3.60e-03	3.53e-03

Values in the table represent ADC error relative to the Full Scale"

The table represents results of many days of preparation and test runs and around one day for each final run. The linearity error is the first computed from averaged samples data against their linear approximation. When error value is converted from the nominal scale fraction to logarithmic scale then it is equivalent to 14 bit resolution for the run test 2 of OPA140 and ADA4084. Unfortunately, there occurred

some offset in one of the sweeps at 0 °C for the first OPA140 run. The raw standard deviation column reports maximum in standard deviation of the raw 4 kHz samples again mean of each 3495 raw samples in one go. Then maximal and minimal error of raw samples to the computed linear approximation at given temperature and sweep is provided. The last one is complete error all raw samples (over 100 millions for each test) against conversion calibration at 25 °C. There the test 1 of the OPA140 with 470 pF integration capacitor shows its quality. The test 2 of OPA140 was the experiment with 100 pF integration capacitor and resistors network tuned appropriately but even for OPA140 then prevails some problems with circuit variance over temperature. Table 2 provides result for the simple variant where comparator is realized on FPGA input pins and FPGA IO bank output digital signal is taken as the conversion reference.

TABLE II. SIMPLE SUMINT ADC CHARACTERIZATION RESULTS

OpAmp type	Linearity at single temp.		Single raw sample at temp		Single raw sample, all temp	
	aver err	raw std	min	max	min	max
OPA140	5.78e-05	5.17e-04	-1.19e-03	1.10e-03	-3.25e-03	3.84e-03
ADA4084	4.69e-05	1.44e-04	-4.27e-04	4.70e-04	-2.68e-03	6.45e-03

Values in the table represent ADC error relative to the Full Scale

In this case much higher noise level and variance over raw 4 kHz raw samples is observed but even this solution can be used for low resolution and less demanding application.

B. *Dynamic Characterization of Simple and Advanced Channels*

Excitation of the ADC input by a harmonic signal at a given frequency and with a constant amplitude close to the full range was performed as “sinewave fit test” - interpolation of the measured values by an ideal sine wave – reference voltmeter Keysight 3458A used digitizer (set on DC sampling mode). The test has been run at next frequencies 10, 15, 22, 33, 47, 68, 100, 150, 220, 330, 470, 680, 1000 Hz. When data are used directly and floating sampling interval is not considered in the sine wave fitting then obtained resolution is unusable.

When properties of the SumInt ADC are accounted then stable results for all frequencies and tree tested temperatures are obtained (0 °C, 25 °C, 85 °C).

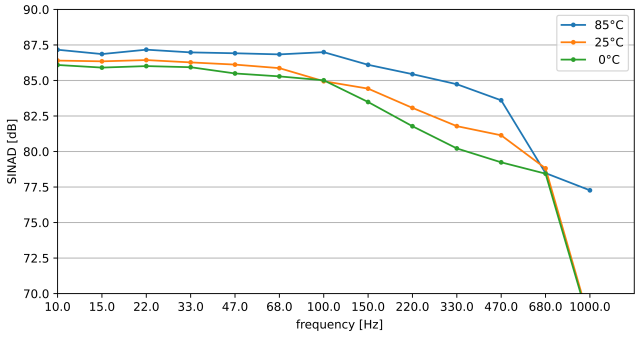

Fig. 8. Advanced channel SINAD as a function of excitation signal frequency

Fig. 8 confirms SINAD for the advanced channel better than 78 dB up to 680 Hz. SINAD is even better than 85 Hz up to 100 Hz. The simple implementation on FPGA pins keeps SINAD over 80 dB till 100 Hz and falls down to 75 dB at 680 Hz. Floating sampling point and changing interval length is accounted in this evaluation but actual integrating character is not modeled during fitting. If that is taken into account then even better results will be probably obtained.

When standard formula for the bit resolution is applied

ENOB = (SINAD_dB – 1.76)/6.02

then resolution in range between 13 and 14 bits is confirmed. The detailed graphs and evaluation then shows that property to suppress quantization noise by factor 1/n is valid for given setup from modulator frequency down to the area about 1 kHz where curve switches to the standard $1/\sqrt{n}$ slope.

V. CONCLUSION

The SumInt ADC technique has been ported to nanoXplore FPGA, actual core HDL code size is about 160 VHDL lines the rest 200 lines are for raw data delivery to the system for evaluation. When compensation for non/equidistant sampling is required then computation with reciprocal approximation would make design more complex but that part can be easily converted into supporting software operating at low frequency after averaging. The short term resolution about 13 bits has been confirmed by dynamics tests. The use of wide operating temperature range is limited by the components stability. The committing criteria defined in the project proposal

- abs. accuracy 5.00e-03 @ 4000 samples/s
- short-term noise 2.00e-03 @ 4000 samples/s

has been fulfilled by OPA140 based design but further analysis of the impact of the temperature to the design is necessary to achieve expected final goal results.

The whole project has been developed in public GitLab repository including HDL, SW and data processing and evaluation solutions [7].

REFERENCES

[1] PiKRON.com: Spectrophotometric detector LCD 5000 – User manual http://pikron.com/pages/products/hplc/lcd_5000.html

[2] P. Píša, P. Porazil, Σ-Integration analog to digital converter, Idea, implementation and results, IFAC Proceedings Volumes, 2005, 38.1: 85-90., 16th World Congress of the International Federation of Automatic Control https://www.sciencedirect.com/science/article/pii/S1474667016372056

[3] PiKRON LX_CPU board documentation and schematics https://www.pikron.com/pages/products/cpu_boards/lx_cpu.html

[4] PiKRON LX_RoCoN motion controller system documentation http://www.pikron.com/pages/products/motion_control/lx_rocon.html

[5] nanoXplore BRAVE NG-MEDIUM FPGA and NX1H35AS-EK evaluation kit https://www.nanoxplore.com/

[6] XilinX Zynq MZ_APO education kit https://cw.fel.cvut.cz/wiki/courses/b35apo/en/documentation/mz_apo/start

[7] PiKRON SumInt ADC GitLab project https://gitlab.com/pikron/projects/sumintadc

Project funding: ESA De-Risk 4000134870/21/NL/GLC/rk