ESD reliability design flow elements for space application mixed signal applications

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founder & CEO

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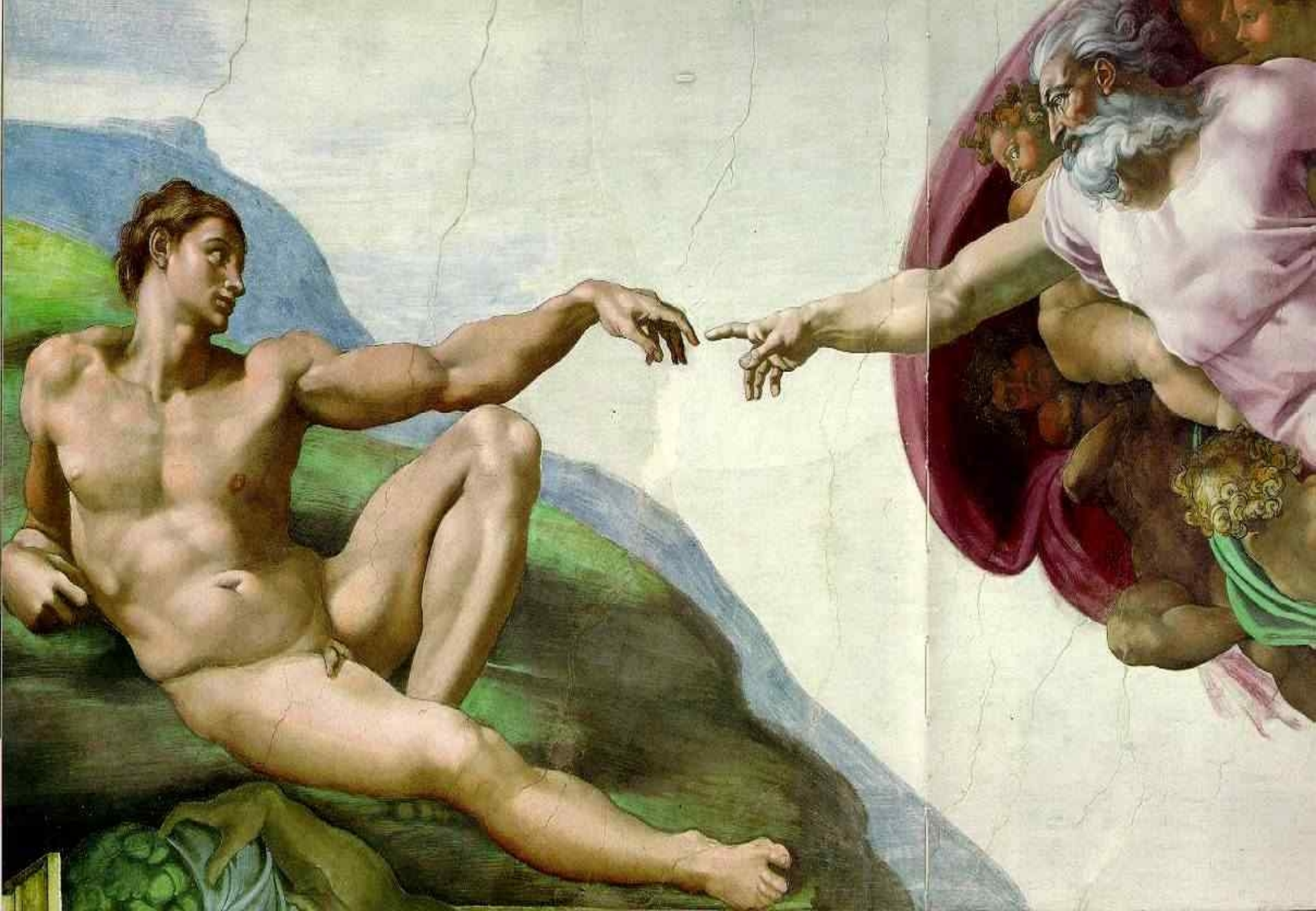
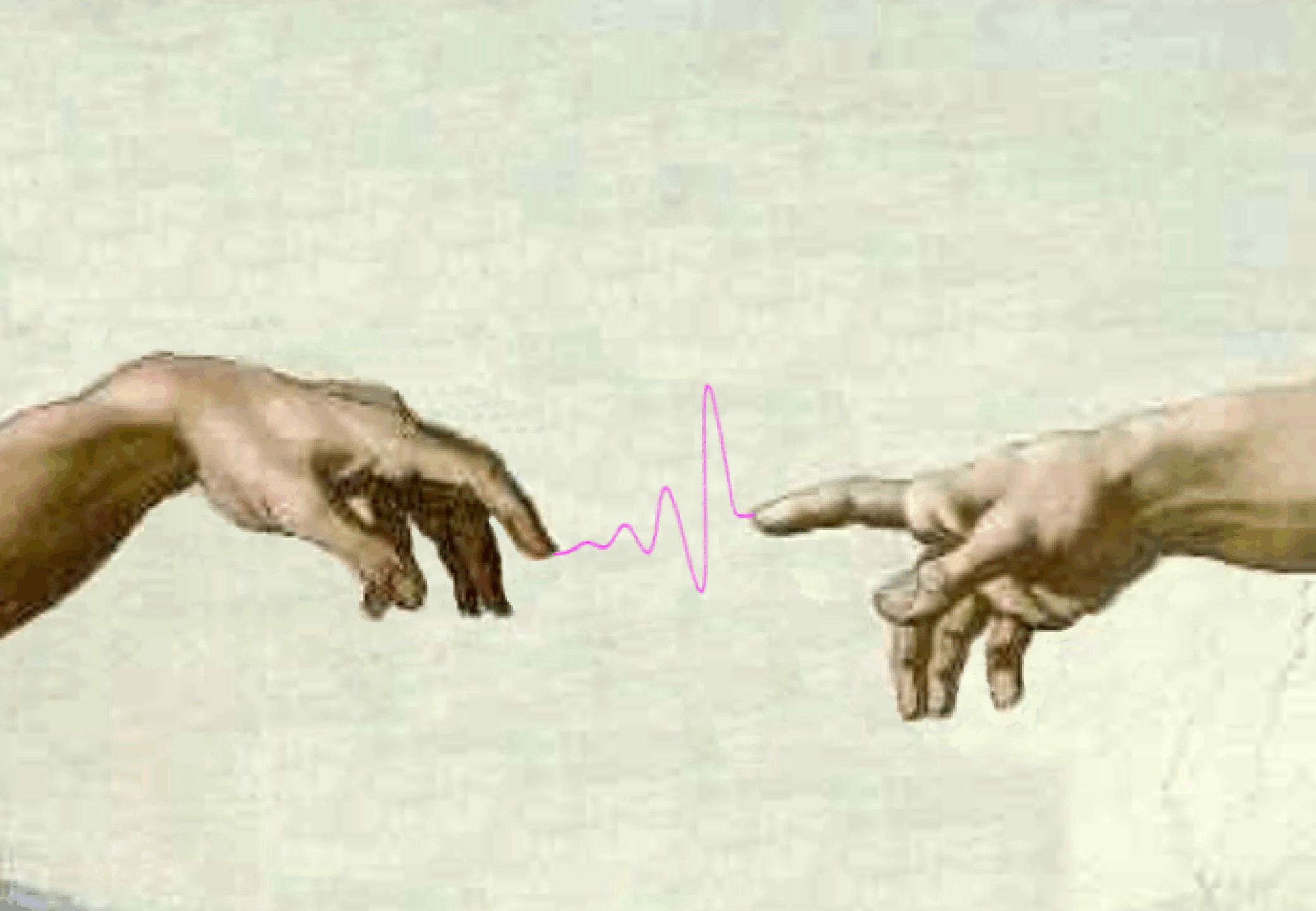




The speaker today ..

Vess Vassilev, Ph.D. EE, M.Sc. Applied Physics

- Over 22 years industry experience in on-chip ESD protection development, ESD IP and circuit design, ESD product qualification
- Special interest in developing ESD EDA tools - circuit simulation solutions & design verification AND space
- Experience with both Industry and Academia, held positions in companies as IMEC (Belgium), National Semiconductor (USA), Texas Instruments (USA).., developing ESD solutions for mixed signal, analog RF/high speed in various technologies;
- General Chair and past Technical Program Committee Chair of the EOS/ESD Symposium -THE ESD MAJOR INDUSTRIAL FORUM
- Author and co-author of more than 40 ESD related papers and 4 patents
- Past ESD topic Editor for the Journal of Microelectronics Reliability
- BoD member of the European SME4Space Association

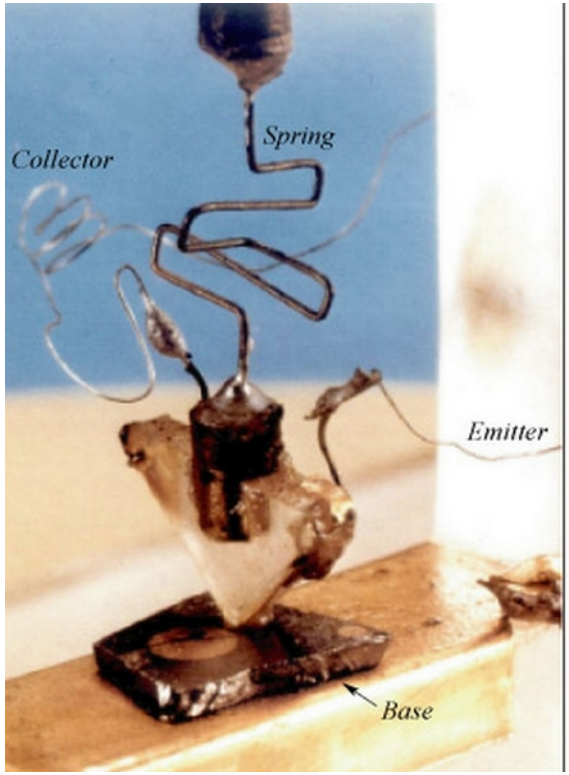
Content

1. Introduction- ESD reliability
2. ESD stress modes and failure mechanisms
3. ESD device physics
4. ESD design – ESD components & ESD Cells
5. ESD design - integrated circuit module and full chip level design
6. ESD circuit moddelling approach
7. Some ESD design cases
8. Space environment ESD
9. Conclussions

WHY ESD *Reliability* ?

Reliability* is to provide *quality* over *time

The first point contact transistor
William Shockley, John Bardeen, and Walter Brattain
Bell Laboratories, Murray Hill, New Jersey (1947)



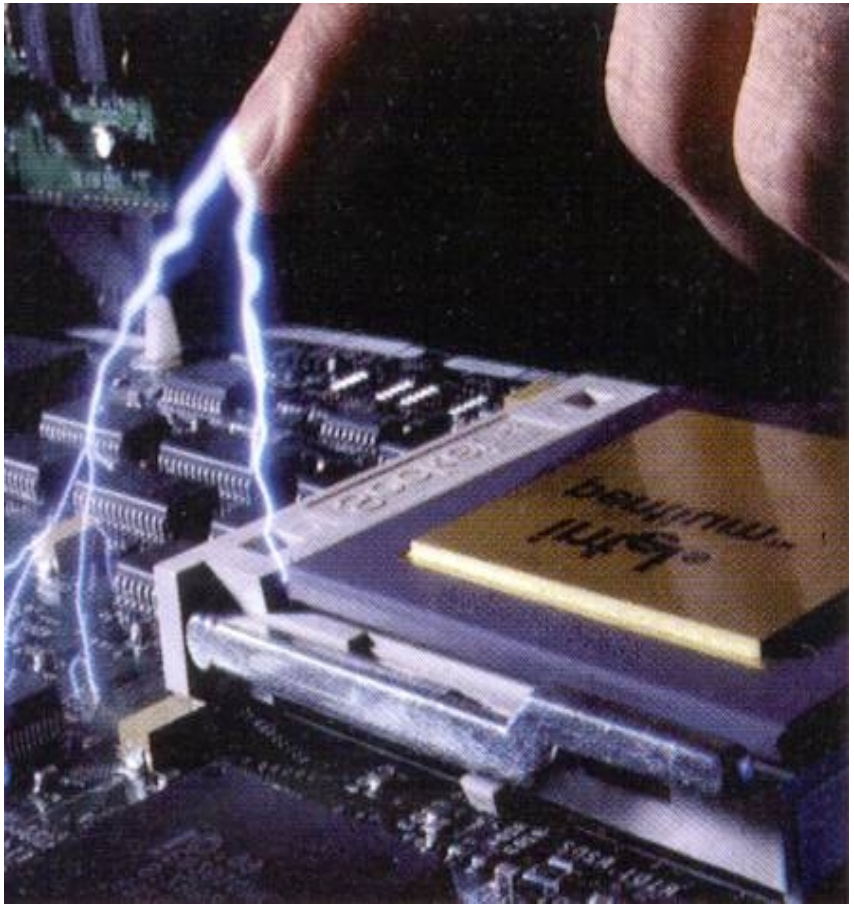
Failure Mechanisms → **ElectroStatic Discharge in Integrated Circuits**

Failure Rates

- **responsible for ~ 45% average product failures**

Design for ESD reliability is a major requirement to ensure high yield and high profit production

ElectroStatic Discharge is everywhere…



Duration: ~ 0.1 s
Current: ~ 10 000 A
Voltage: ~ 100 million V

Duration: ~ 100 nano s
Current: ~ 10 A
Voltage: ~ 10 000 V

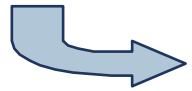
RELIABILITY FOR IC TECHNOLOGIES

Electrostatic Discharge

- High current (1.6 Amps) for 1-100 ns
- Human and machine handling damage
- Immediate and visible, as well as latent, failures
- Destructive IC chip design function
- Can be overcome with protection clamps

Electrical Overstress

- Voltage overshoot resulting in high currents for 1 us - 1 ms
- Overvoltage during applications
- Very destructive and cannot be recovered



Can be reduced with proper ESD/Latchup design

Latchup

- Interaction between PMOS and NMOS devices
- High power supply current until power disconnected
- Destructive damage to the IC chip
- Can be prevented with design and process

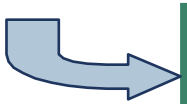
Has a more direct trade-off with ESD

Duvvury at EOS/ESD

RELIABILITY FOR IC TECHNOLOGIES

Electromigration

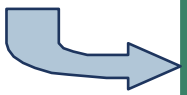
- Result of metal transport under high current density through metal leads
- Can lead to nonfunction of the chip
- Can be overcome with good design rules and understanding of the metal process



Can degrade with latent effects from ESD

Hot Carriers

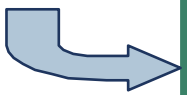
- Degradation of transistors during long-term operation (5-10 years)
- Understanding of the phenomena during technology development is important
- Circuit simulations can be used to predict failures



Direct trade-off with ESD in most cases

Oxide

- Wearout mechanism over long time period
- Can be reduced with technology development
- Defect reduction during process



Vulnerable to ESD damage or latent effects

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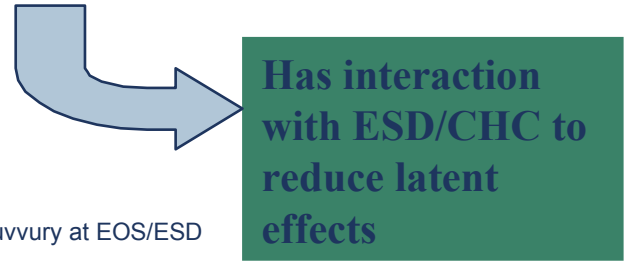
RELIABILITY FOR IC TECHNOLOGIES

Antenna Effects

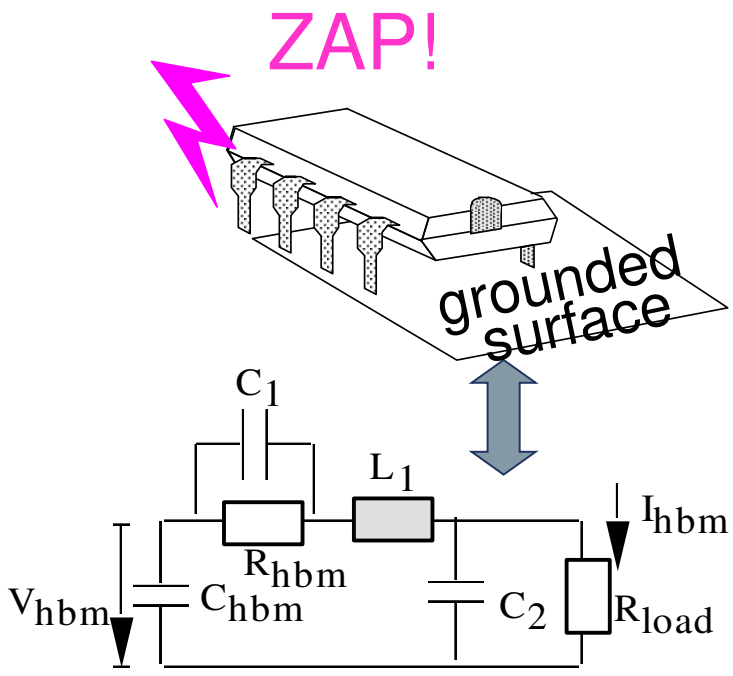
- Occur due to plasma charging during process steps and the charge buildup can blow gate oxides
- Can be reduced with proper process monitor
- Antenna effects can be reduced with proper protection clamps and by following the design rules



ESD modes - HBM, MM

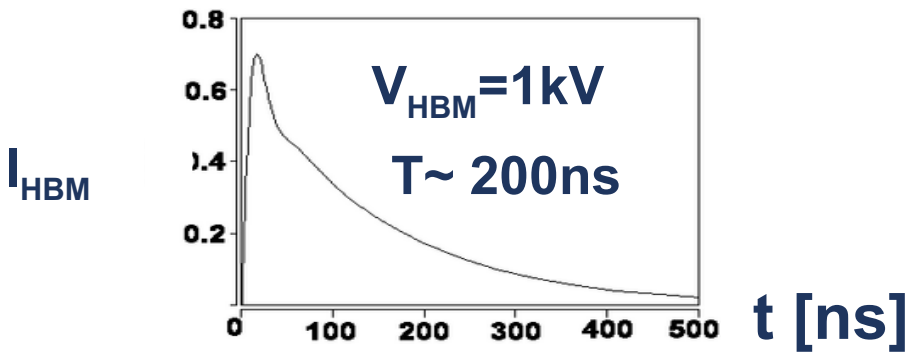
Human Body Model (HBM)

- **charged person discharges trough the component**
- **C_{HBM}=100pF, R_{HBM}=1.5kΩ, □ =150ns, I_{max}~0.67A per 1kV**



Machine Model (MM)

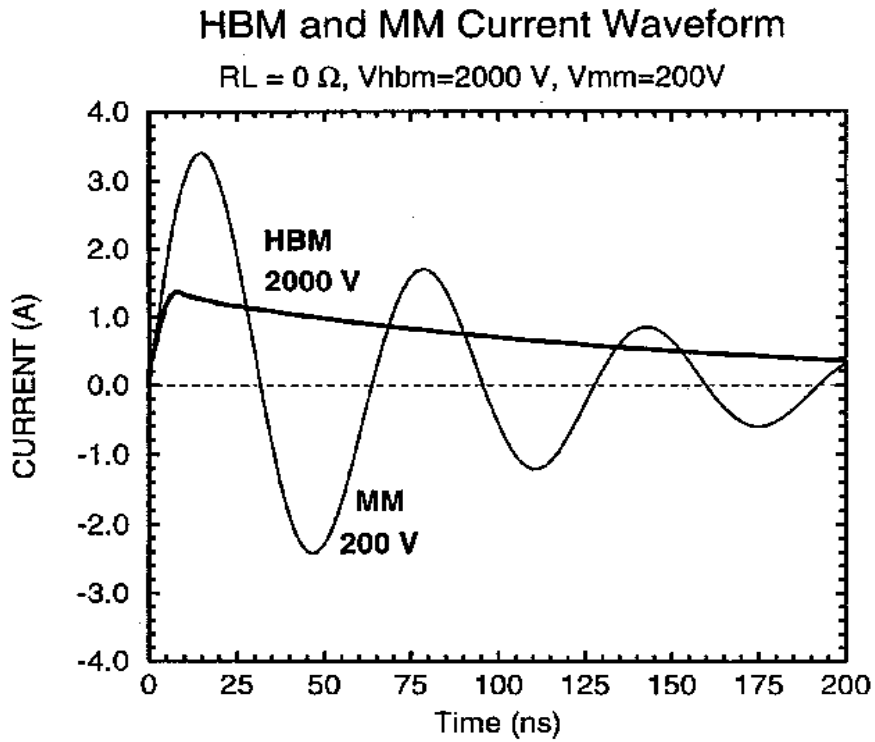
- **charged machine discharges trough the component**
- **C_{MM}=200pF, R_{MM}0 Ω, ²T=40ns, I_{max}~17.5A per 1kV**



HBM/MM events are equivalent to current injection

HBM vs. MM

- **Comparison of 2000 V HBM vs. 200 V MM**



- **According to ESD S5.1-1993 (HBM)**
  ESD DS5.2-1996 (MM).

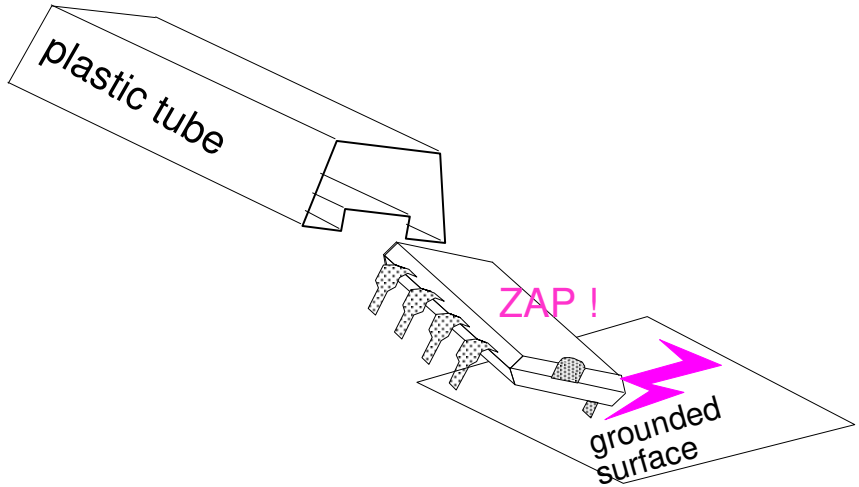
AJITH AMERASEKERA 1999

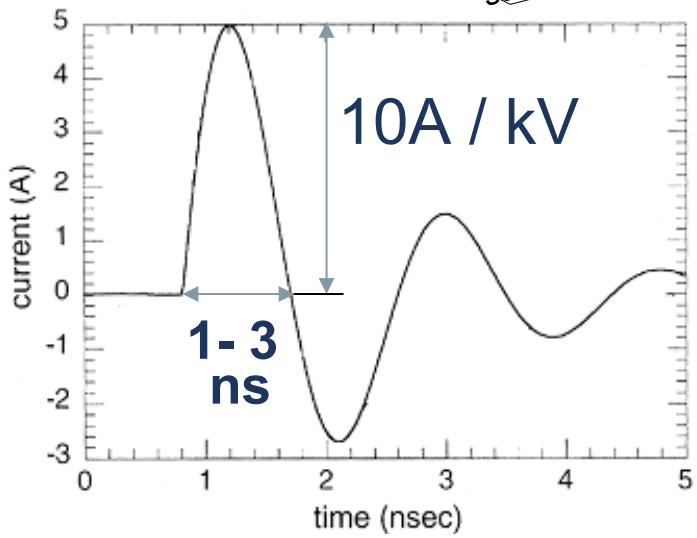
ESD modes - CDM

Charged Device Model (CDM)

charged **component**
discharges via grounded pin(s)

- $C_{component}$
- □ =1-3ns
- I_{max}10A per 1kV
- **any part** in an IC can be affected !

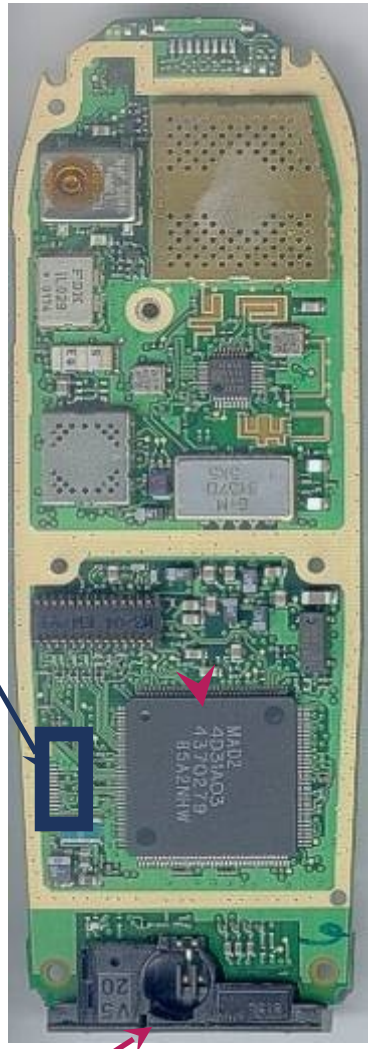


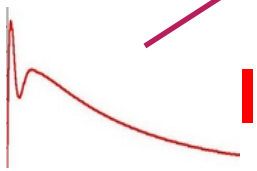


CDM stress is a voltage stress and depends on Z!

The system level ESD – THE real issue

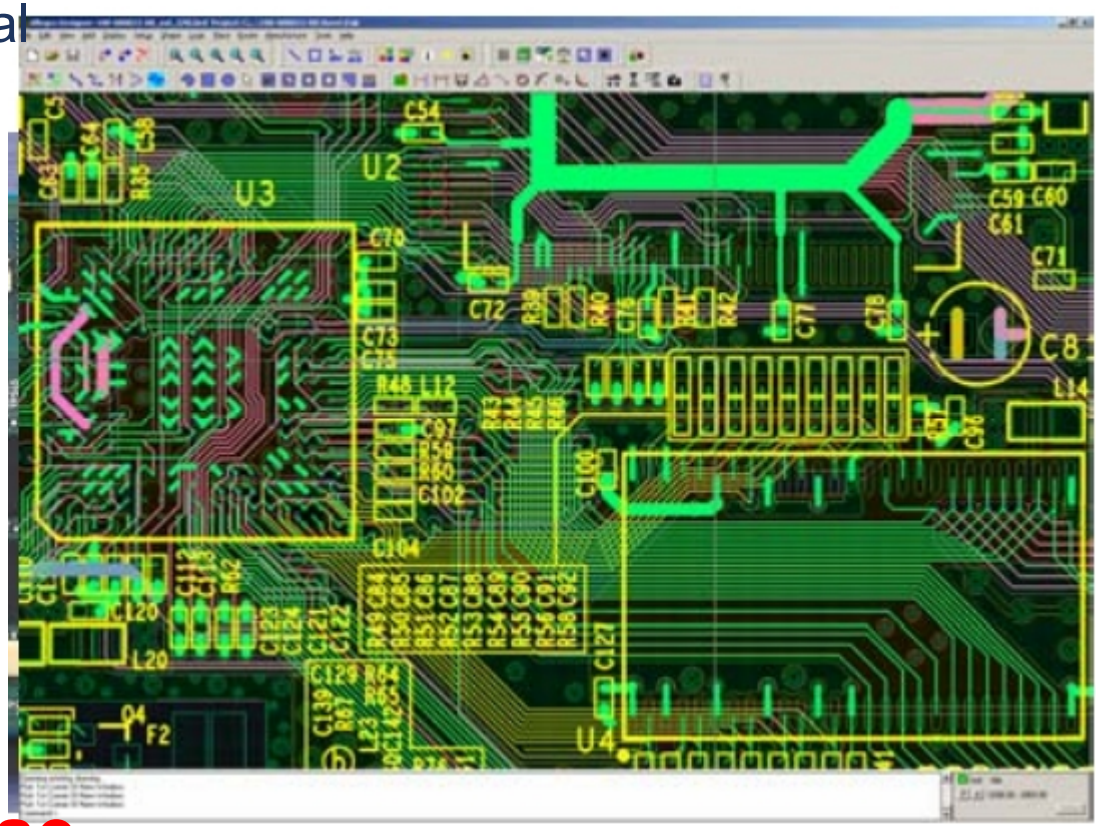
The PCB board and discrete components act as filters which change in “unknown’ way the input waveform



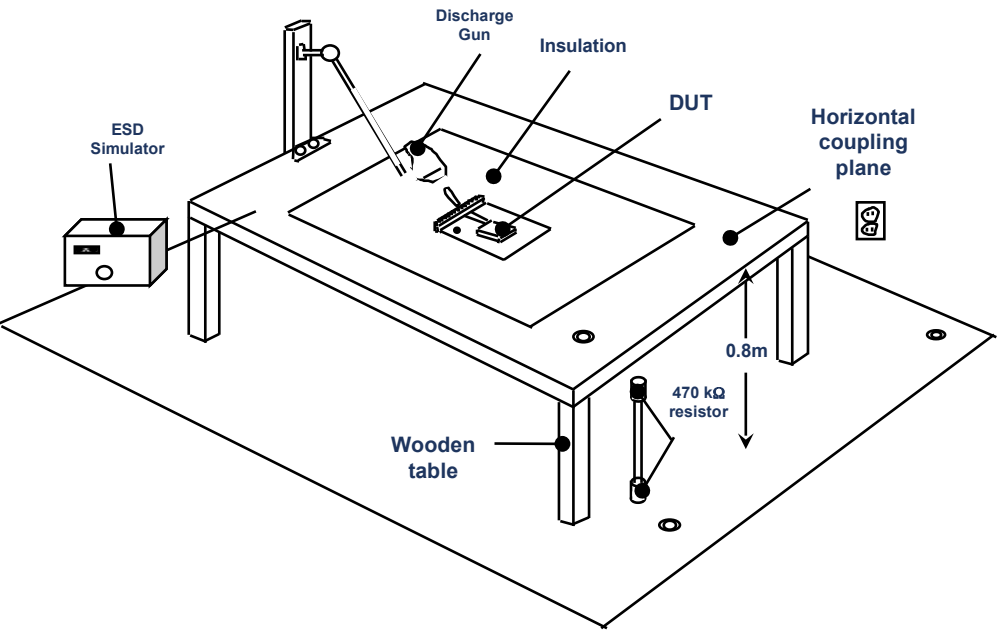


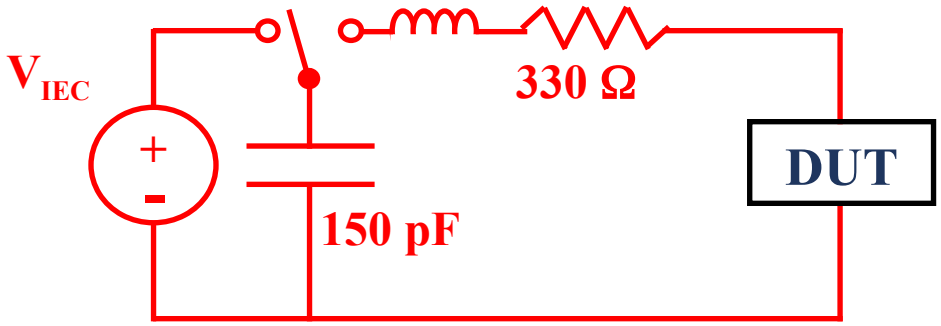
IEC ESD pulse

- Large Voltage transients can occur inside the PCB board
- ESD IEC waveform on IC - **Not** defined !
- Use discrete components to filter input IEC signal

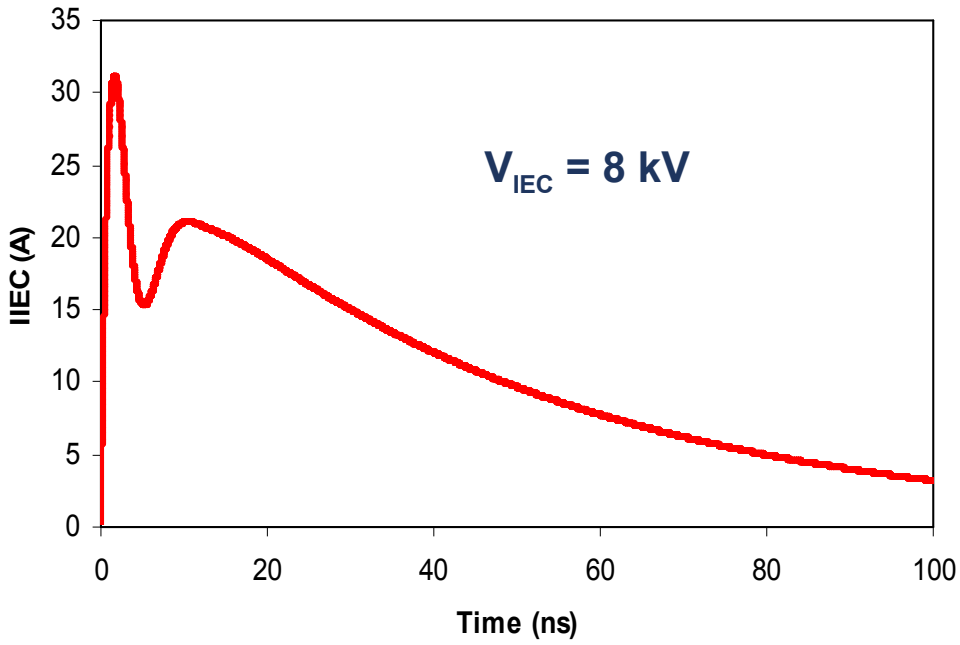


System Level ESD Testing Models - IEC



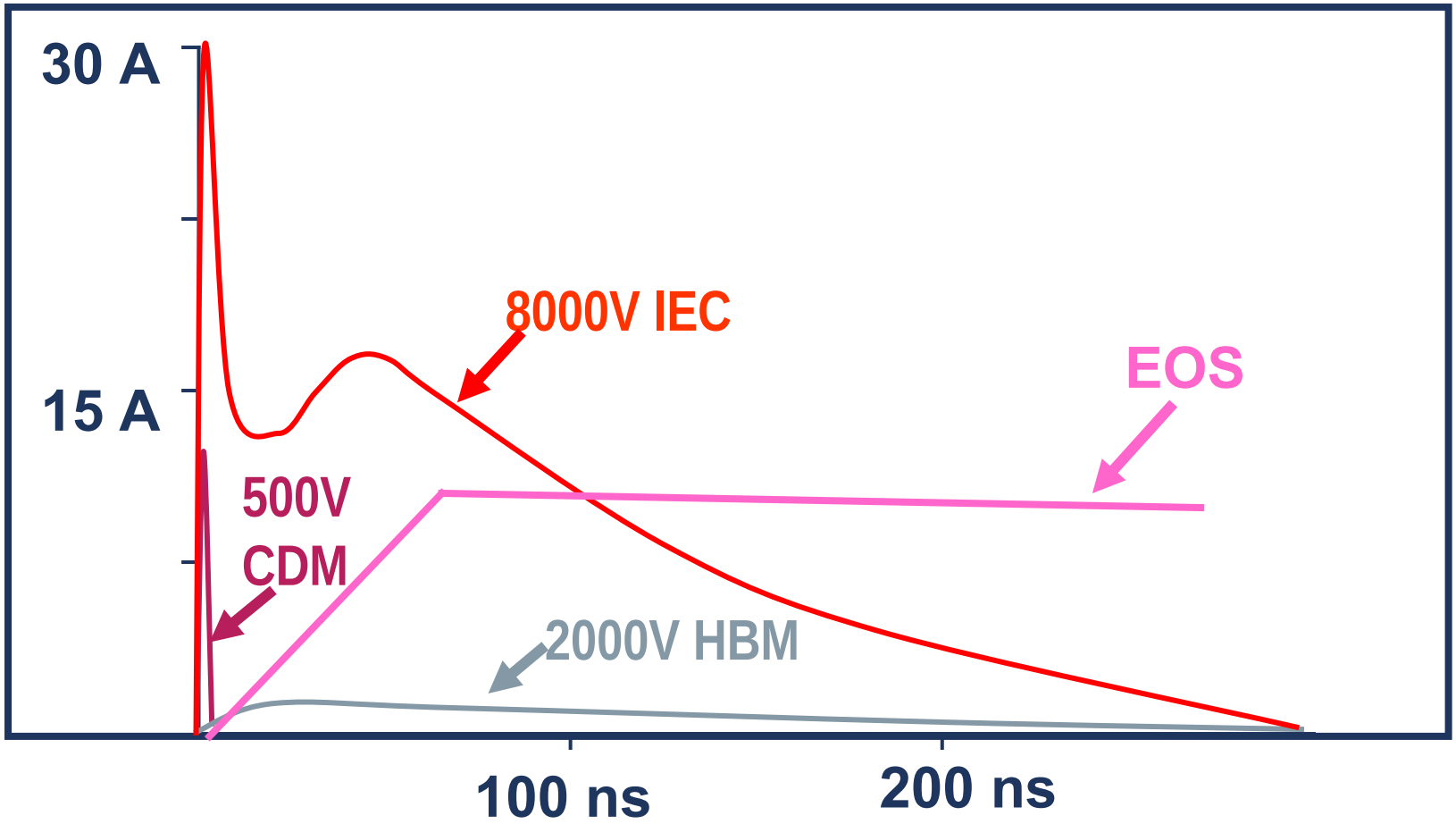


Equivalent Circuit



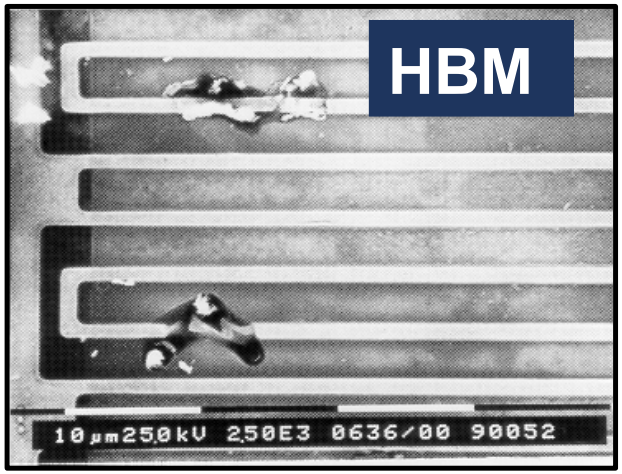
See the "IEC 61000-4-2" standard for detailed specifications

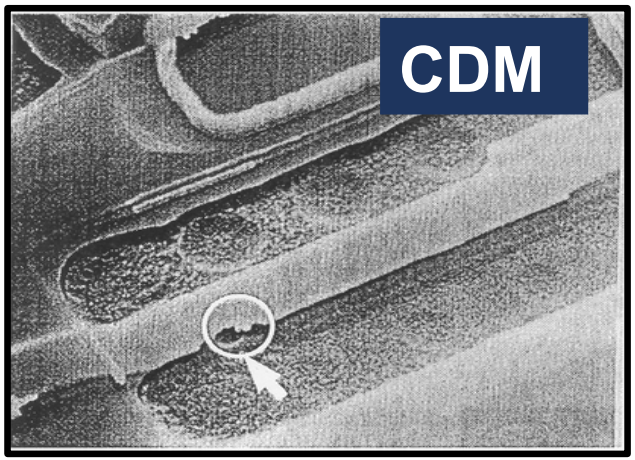
Transient Stress Modes

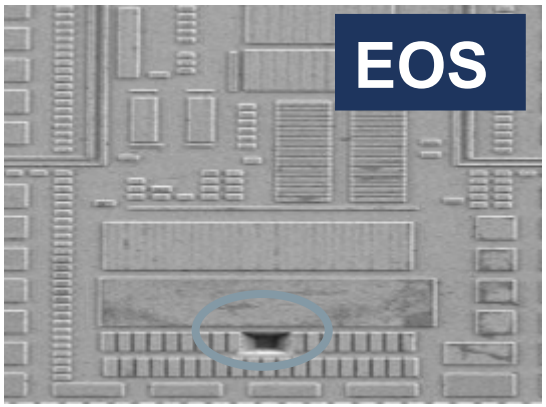


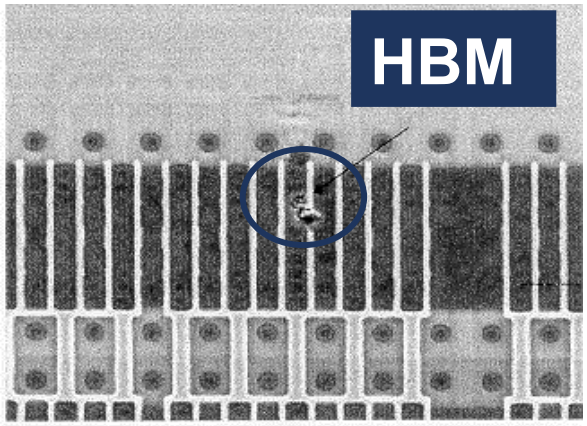
- ESD: HBM and CDM require on-chip protection
- IEC: requires off-chip and on-chip protection
- EOS: requires care during customer applications

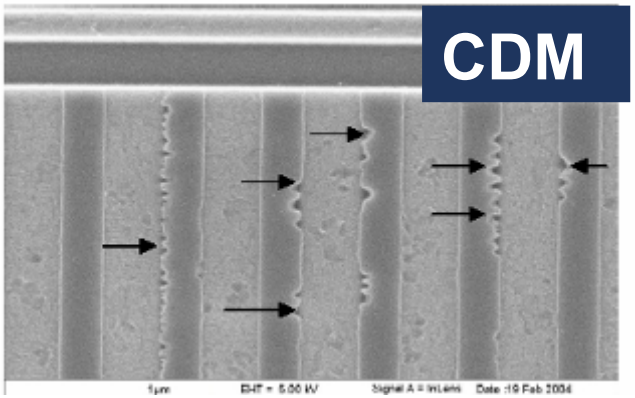
Typical ESD Damages

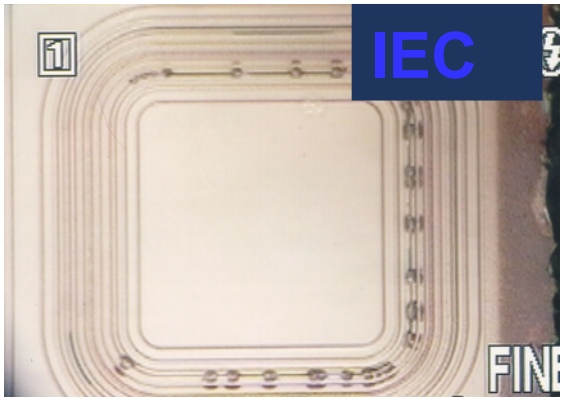












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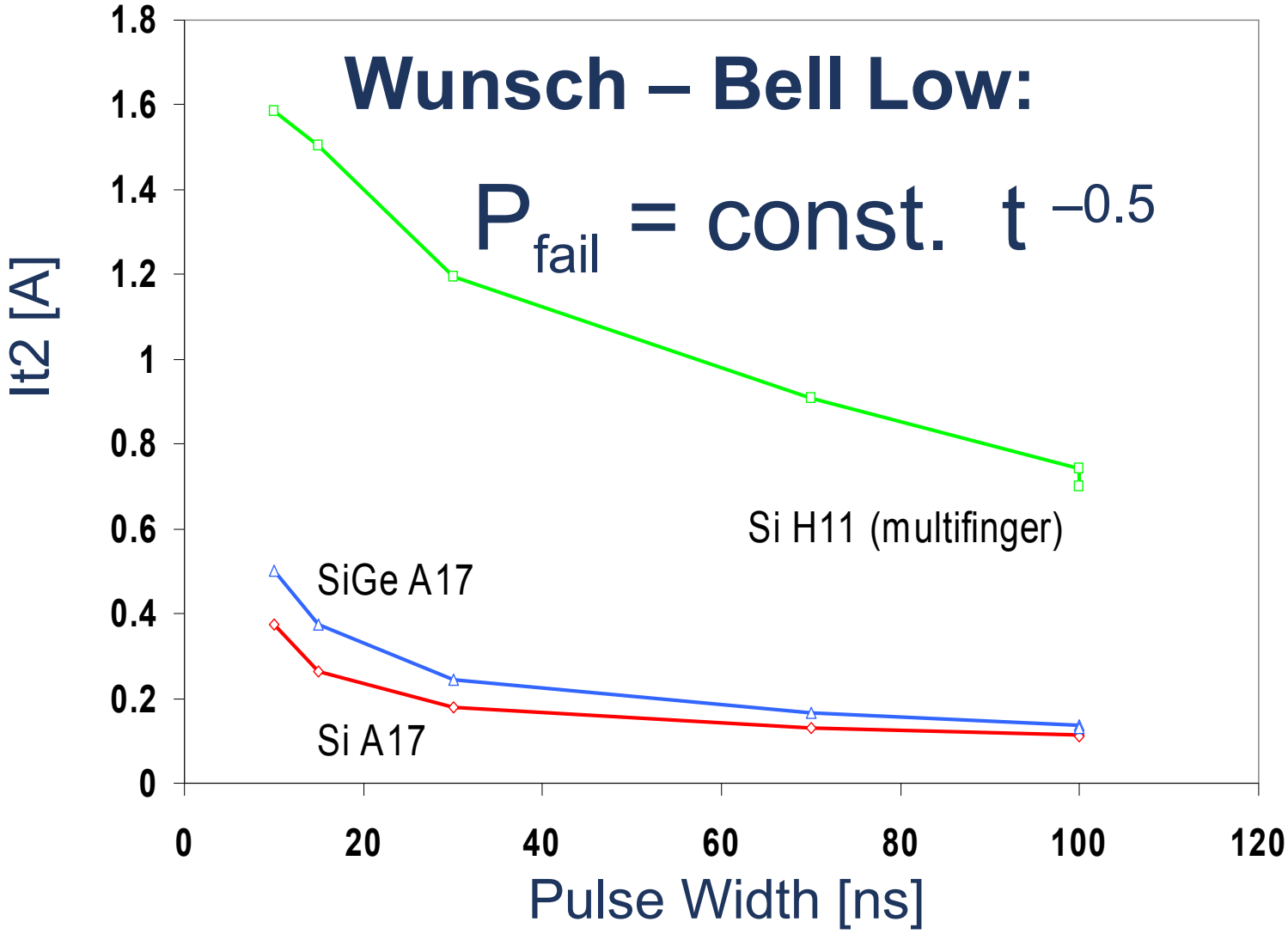
Subtle damage for HBM/CDM is becoming a major issue with technology scaling & complex IC pin circuit layouts

ESD Modes Comparison

Model	HBM	MM	CDM
Test Levels (Volts)	500, 1000, 1500 2000, 2500	100, 150, 200	250, 500, 750, 1000
Pulse Width (ns)	~150	~80	~1
Rise Time	2-10 ns	n/a	<400 ps
Typical ESD Failures	• Junction Damage • Metal Penetration • Metal Melt • Contact Spiking • Gate Oxide Damage		• Gate Oxide Damage • Charge Trapping • Junction Damage

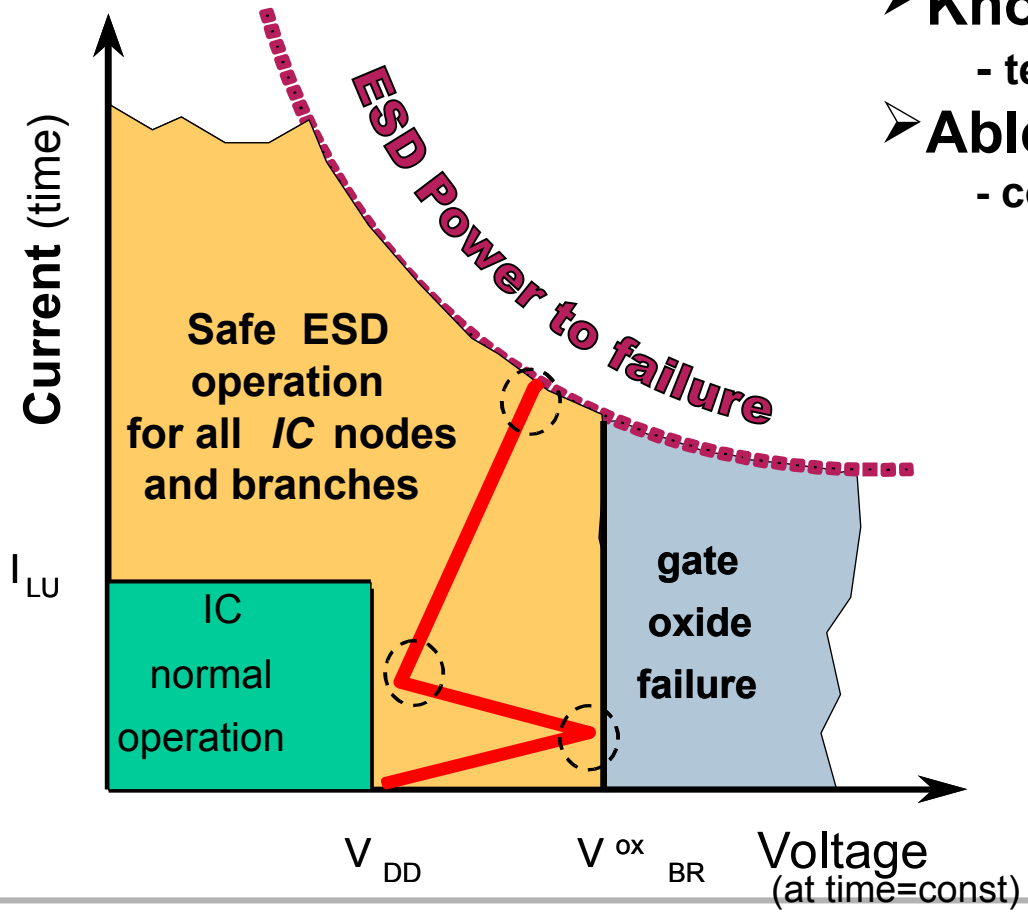
Duvvury at EOS/ESD

Silicon melting failure level (It2) in ESD current injection



Any ESD design ultimate goal

Ensure the ESD domain responses (red curve) is within the Safe Area of Operation (orange area) for ALL circuit components



ENABLERS to perform ESD optimisation

- **Know ESD SOA**
  - technology characterization
- **Able to compute ESD domain IV**
  - component, IP module and full IC ESD simulation

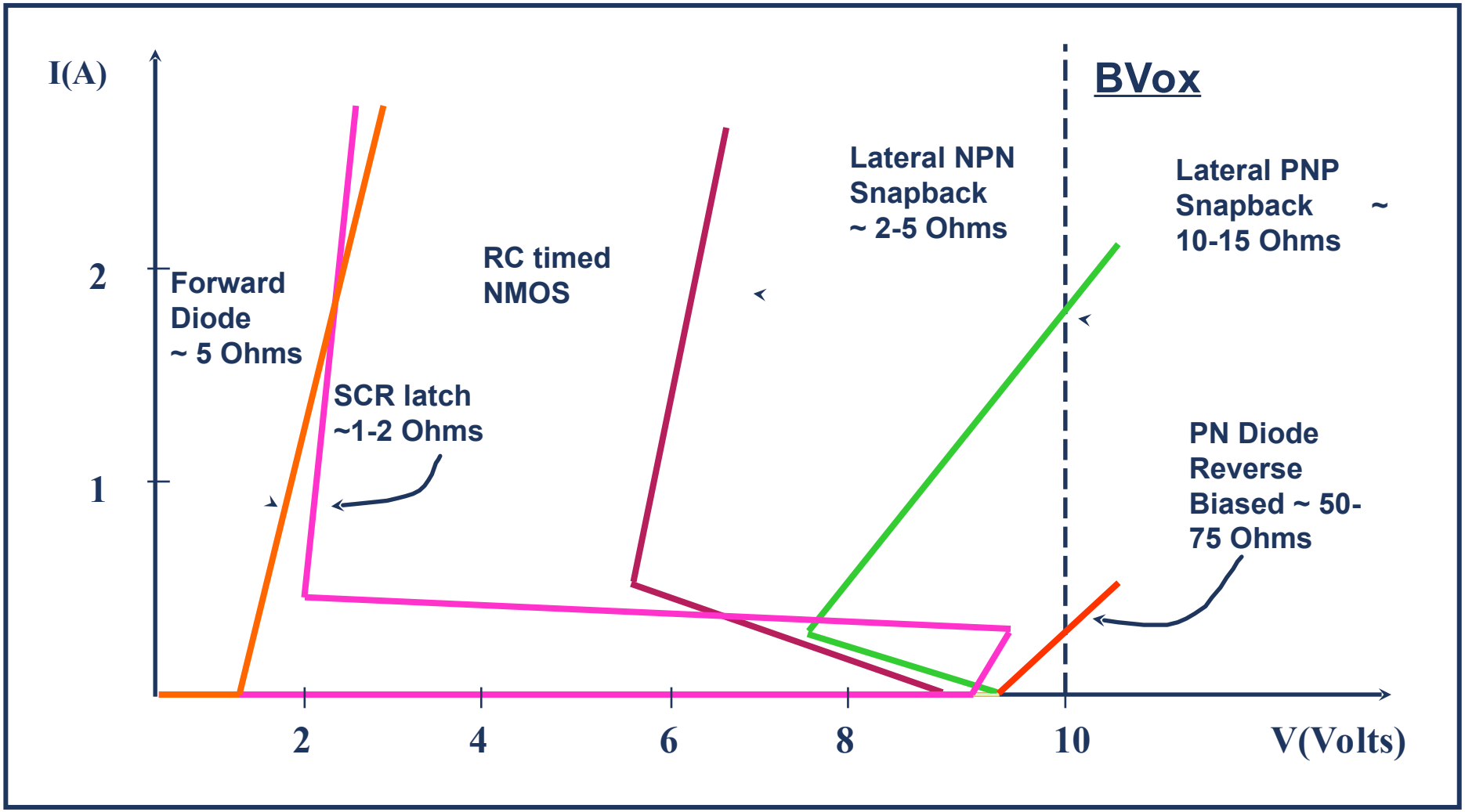
Power levels

circuit operation ~ 100mW
ESD stress pulse ~ 10W

Δ~ 100÷1000 times!

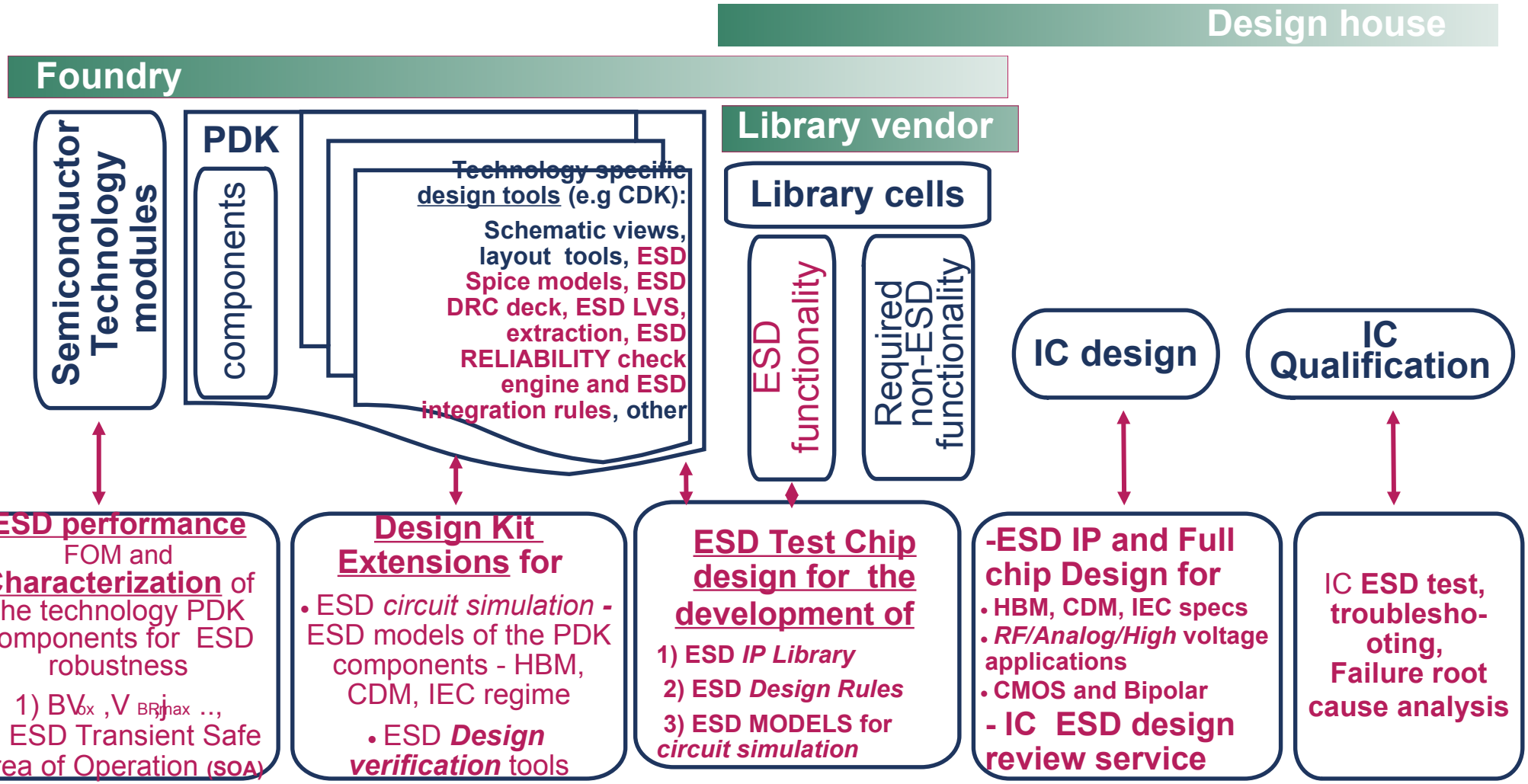
There is a need for specialized ESD domain simulation tools to handle such high power levels and provide valid simulation results

ESD PROTECTION CIRCUIT ELEMENTS



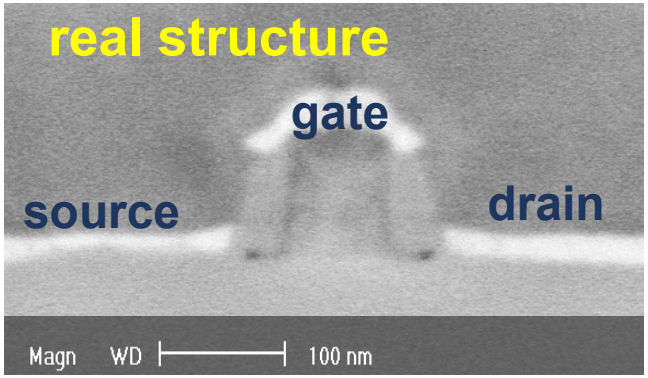
Any type of ESD clamp must protect the gate oxide with a breakdown of Bvox.

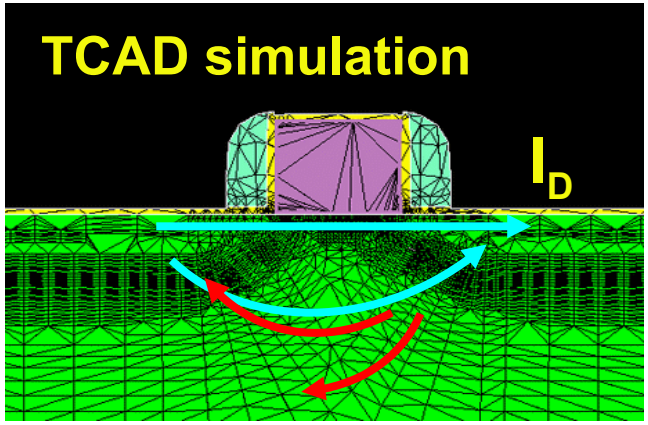
ESD needs through the technology lifetime

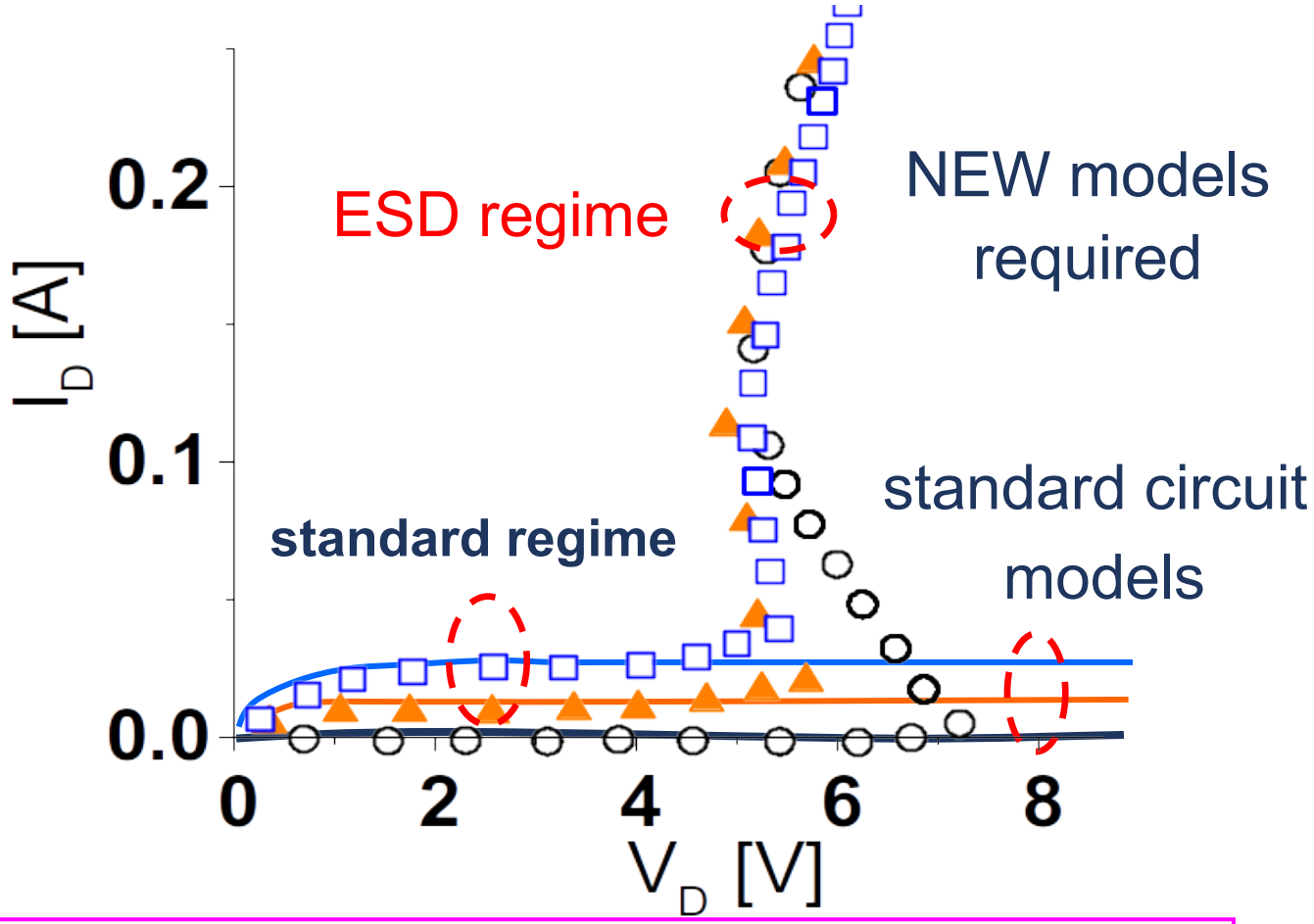


Example: PDK implementation of an ESD snapback MOSFET for ESD protection design ...

Basic ESD clamp behaviour – gg NMOS



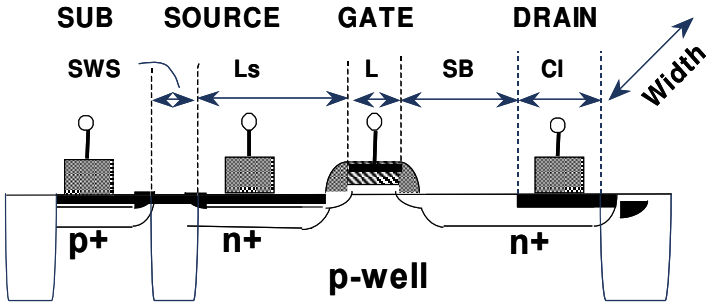




NEW circuit models are required to describe the ESD domain of MOS transistor operation

Main requirements for a MOSFET ESD model

- Description of the MOSFET snapback operation – I(t), V(t)
  (accuracy ΔV/V ~ 10-30%, ΔI/I<10%, determined by the ESD design space)
- Scalability with the major ESD design parameters- W,L,SWS,SB
- Applicability for I/O pad cell level simulations (efficiency,convergence)



Physical effects to be considered:

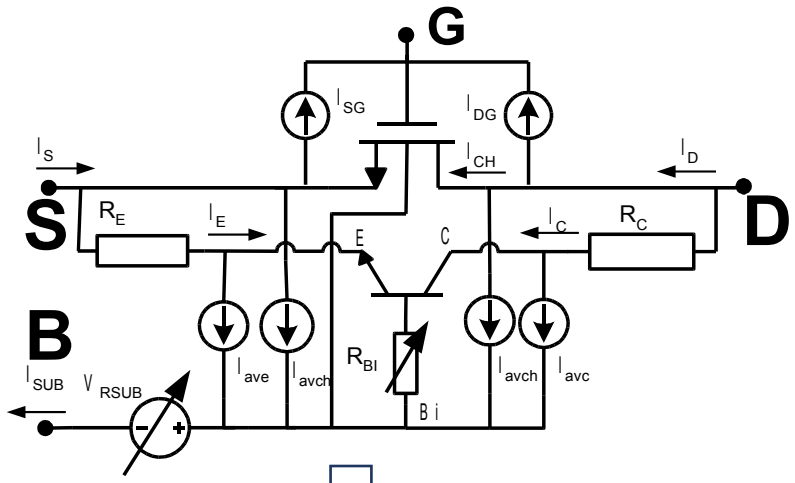
- MOSFET breakdown
- Bipolar triggering
- Bipolar operation
- High-current conduction

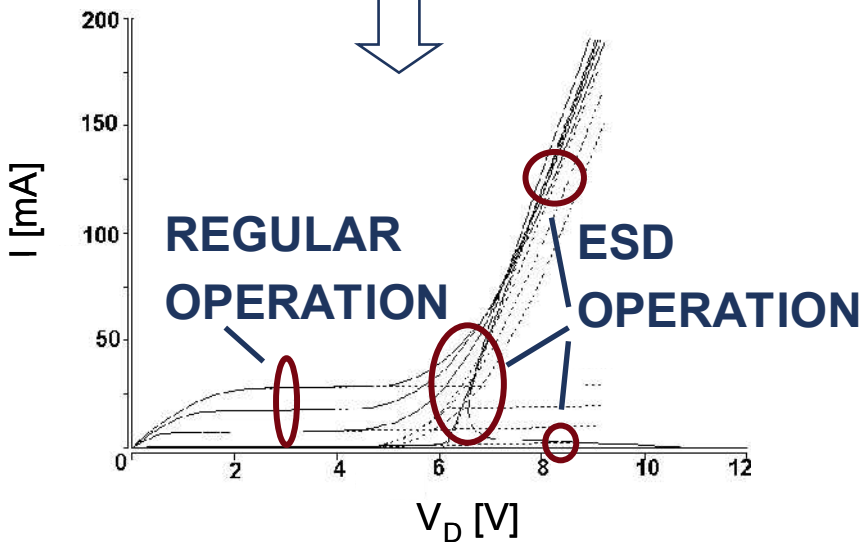
Not significant from ESD circuit operation design view

- self-heating and elevated T^0 operation
- failure level modelling

Simulation models for ESD circuit operation

Example: MOSFET model for ESD domain simulation





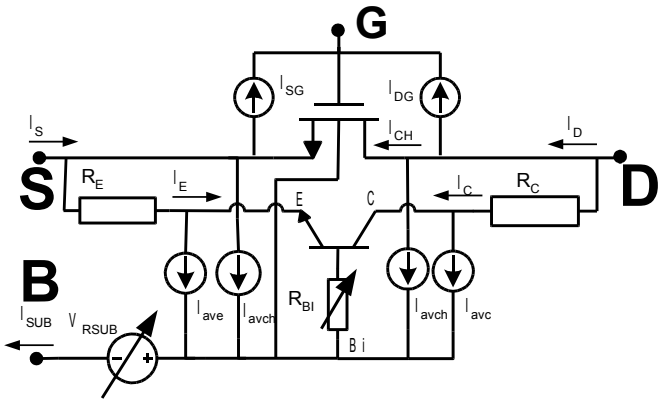
- ✓Equivalent circuit model (to ease the practical implementation)
- ✓VERILOG A implementation of the equation defined current/potential generation sources
- ✓Symmetrical topology for D/S (Important for variable polarity ESD stress e.g. CDM)
- ✓Capacitance model-the same as for the the intrinsic MOSFET

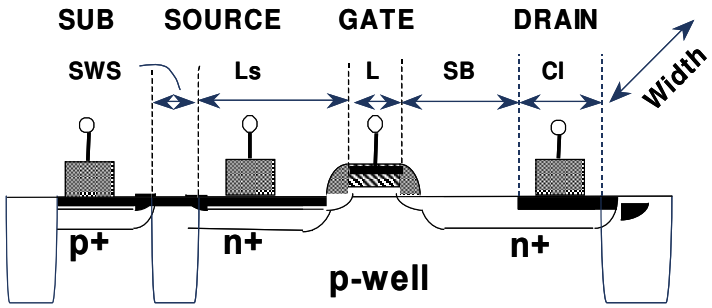
NOVORELL's compact modeling approach allows extension of the regular component models into the ESD regime

Simulation models for ESD circuit operation

Example: MOSFET model for ESD domain simulation

Parameter Extraction



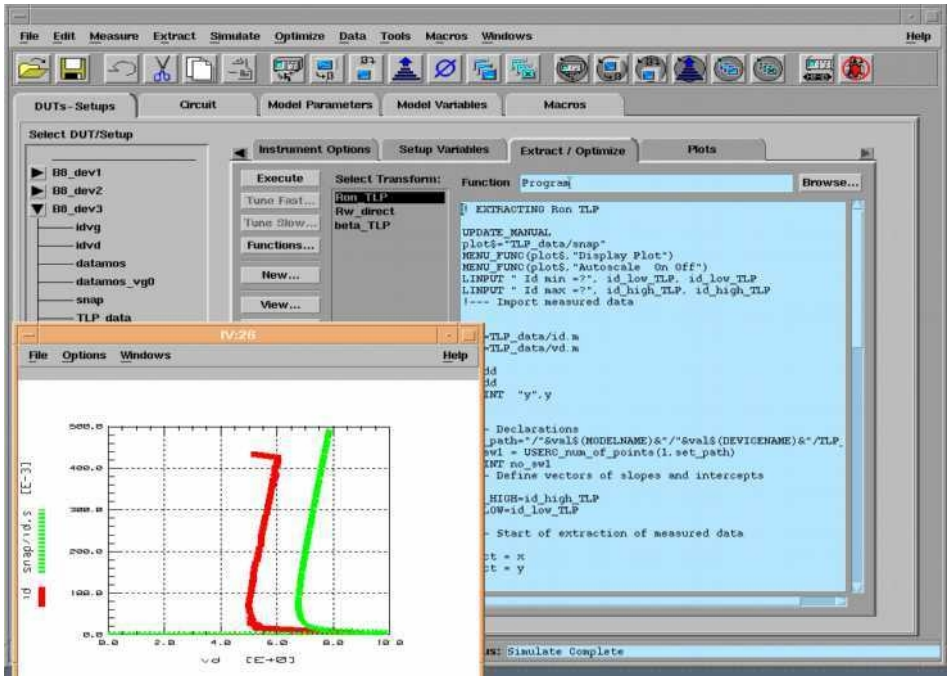


- The intrinsic MOSFET – a library model
- Extraction of the bipolar parameters as function of the ESD layout variables
  - -multiplication factors M_b,M_{ch}
  - -substrate potential and tunneling sources
  - -current gain β
  - -high current 'on' resistance
  - -base transit time
- Scaling of the parameters - based on physically based semi-empirical expressions

The ESD model parameters are extracted from an array of structures using reverse solutions of the model equations (whenever possible) and applied to representative parts of the experimental characteristics.

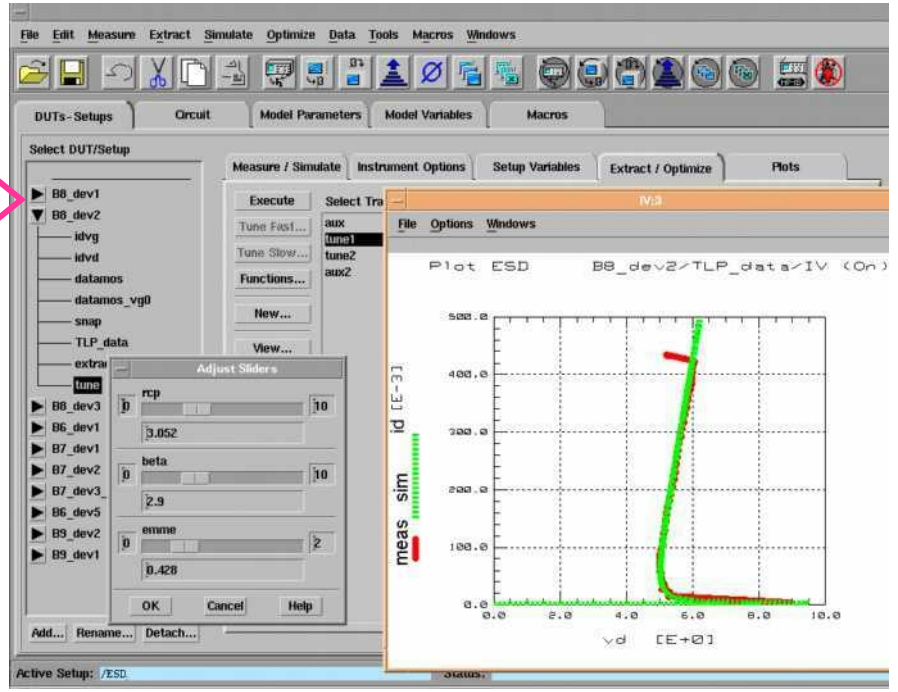
ESD Model Calibration tool for your SPICE modeling team

Before model extraction: need to fit the measured (red) and simulated (green) ESD IV's



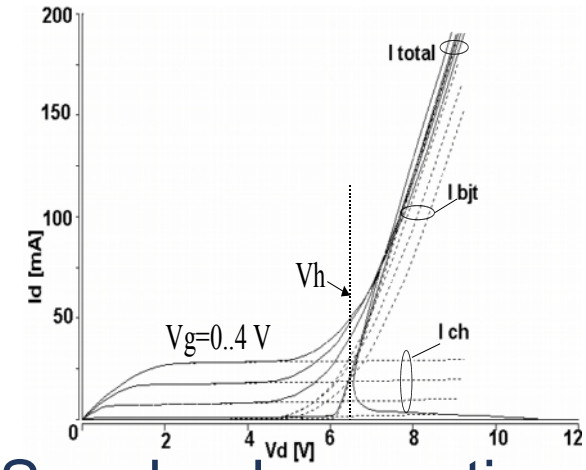
NOVORELL's ESD modeling expertise allows to achieve excellent accuracy between ESD simulation ESD and measurement

After model extraction: the measured (red) and simulated (green) ESD IV's match



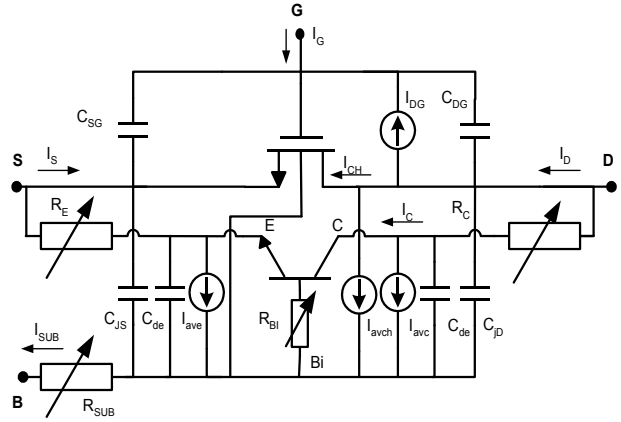
- IC-CAP from Agilent is a standard tool in the industry used for model calibration
- Both the static and transient ESD behaviour of the device can be represented in IC-CAP
- Fully compatible with the standard MOSFET extraction implementation

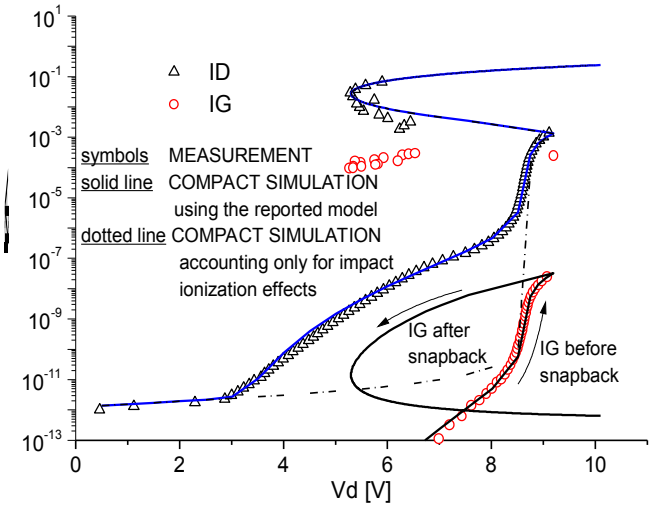
Simulation models for ESD circuit design



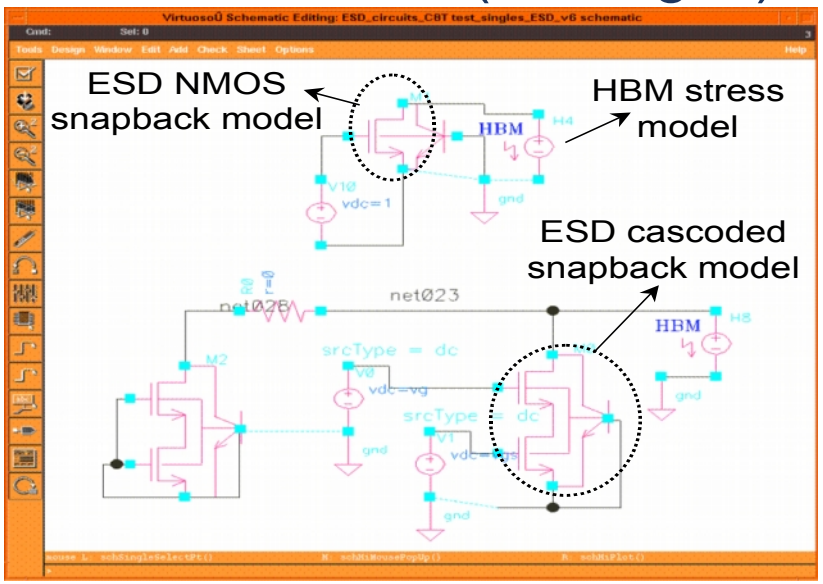
Snapback operation- Si-data

The compact modeling approach allows extension of the regular SPICE models into the ESD regime





Snapback operation- calibration to Si-data

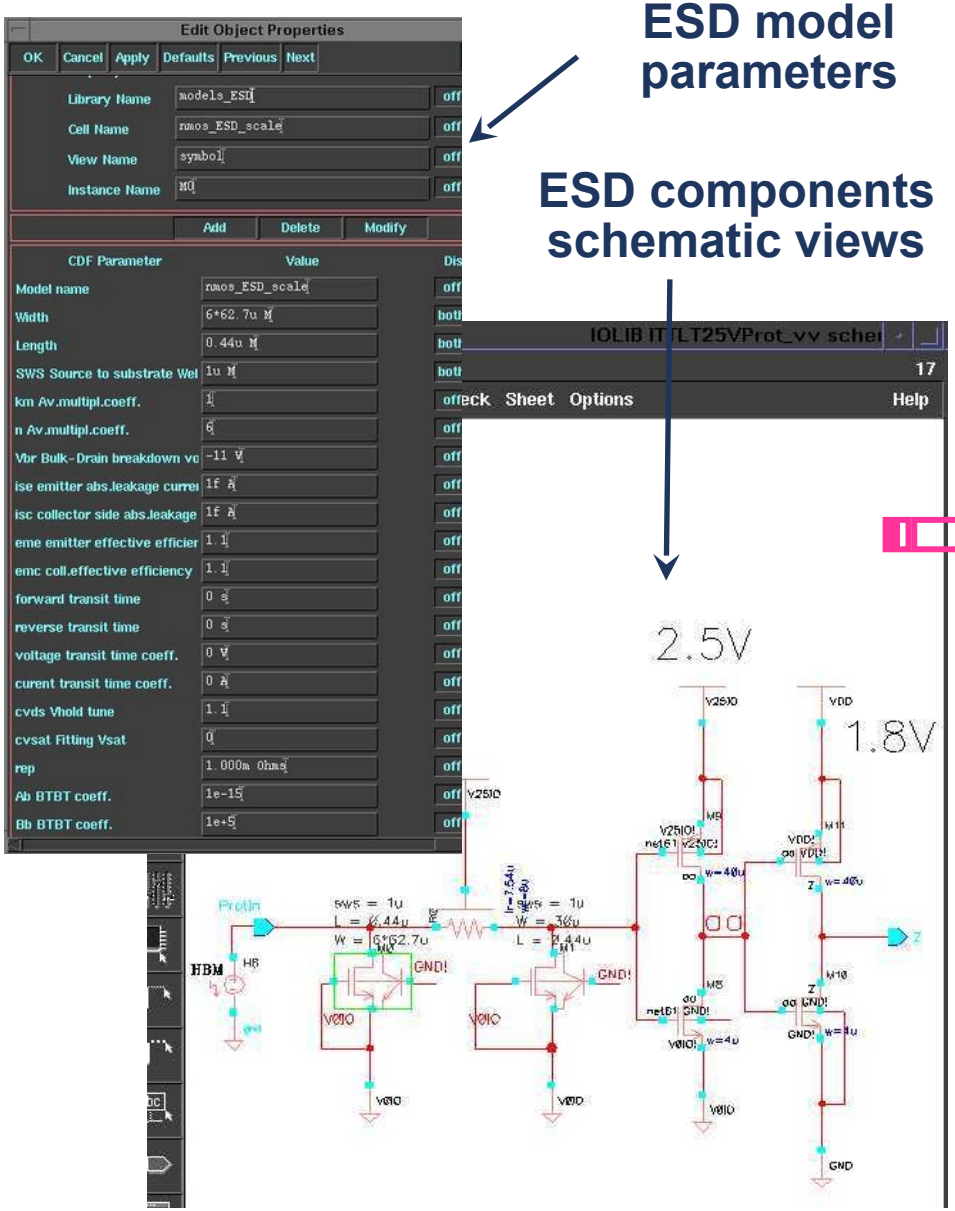


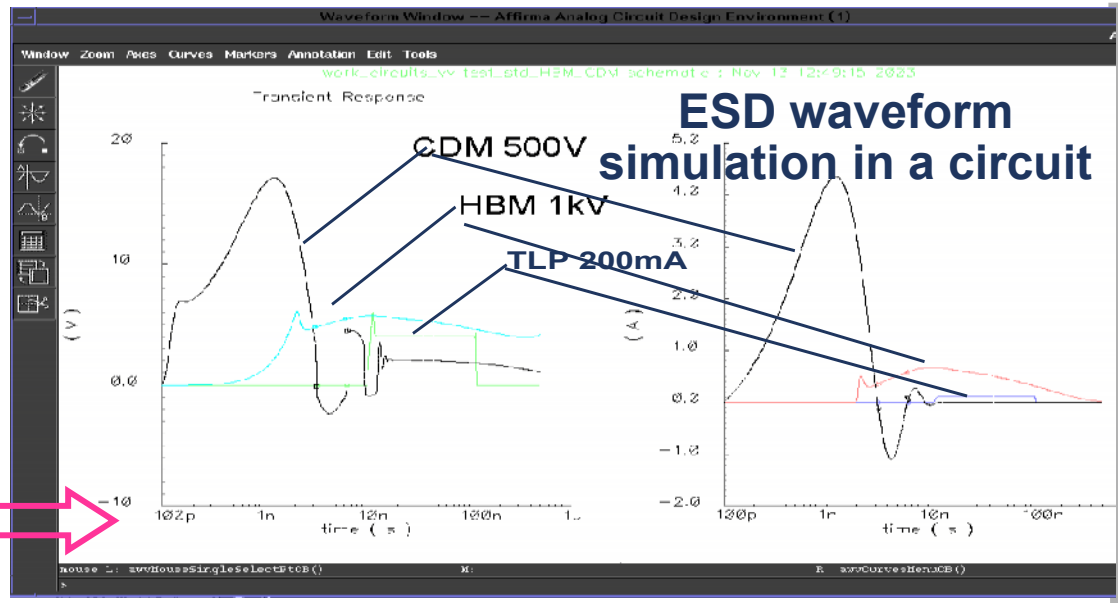
Cadence Design Kit integration

ESD design kit Implementation in Analog Artist/CADENCE

ESD model parameters

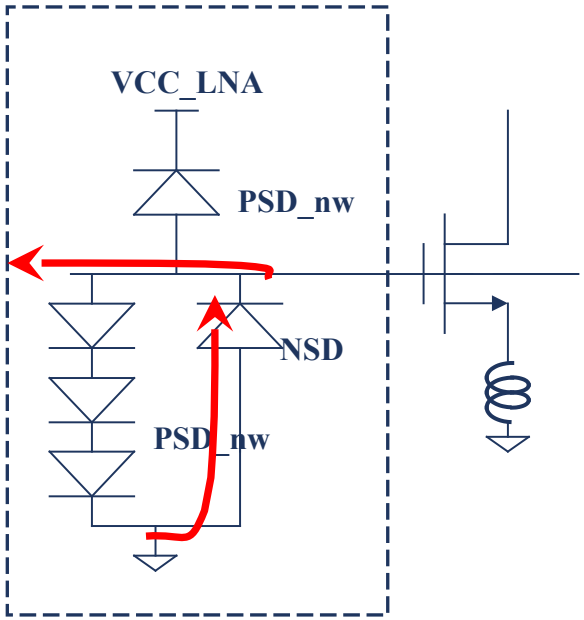
ESD components schematic views

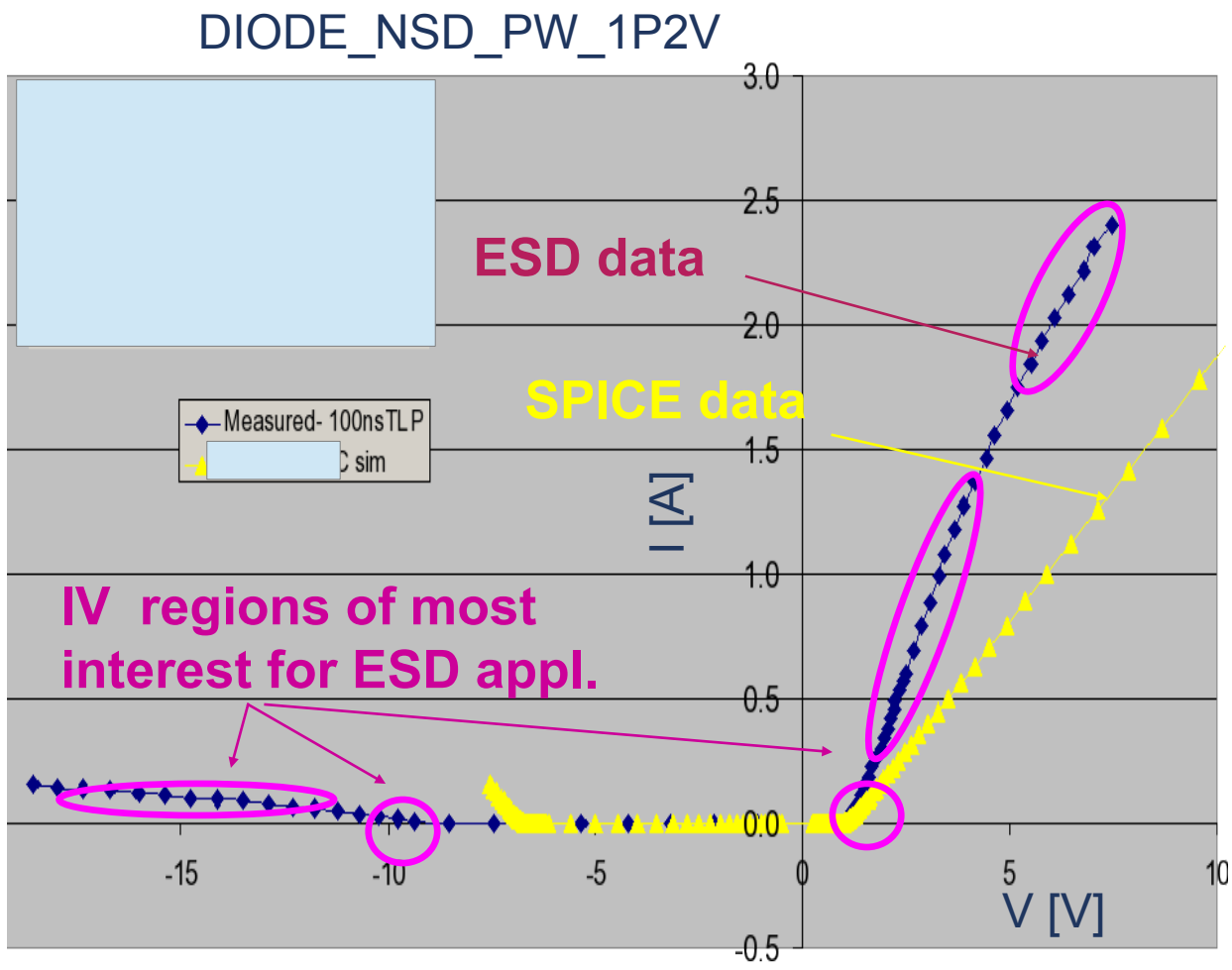




- implementation in the standard CADENCE PDK environment
- SPECTRE&HSPICE simulation

Pwell diode : important ESD clamping device

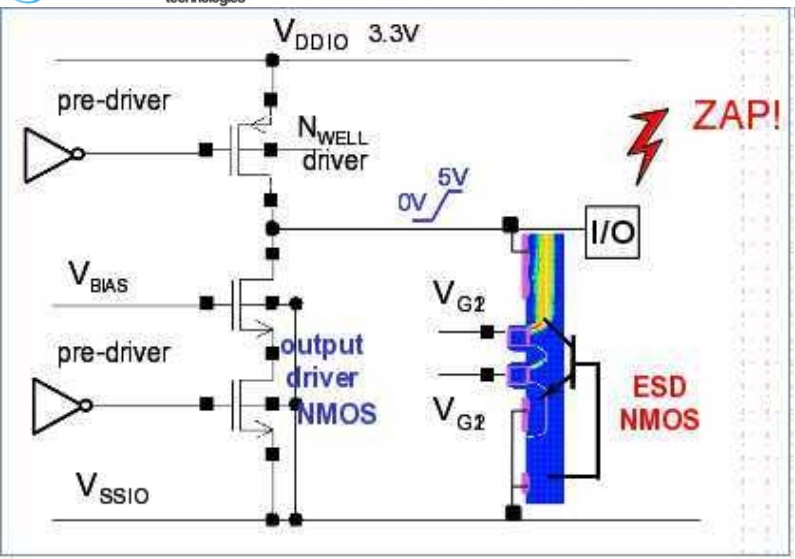




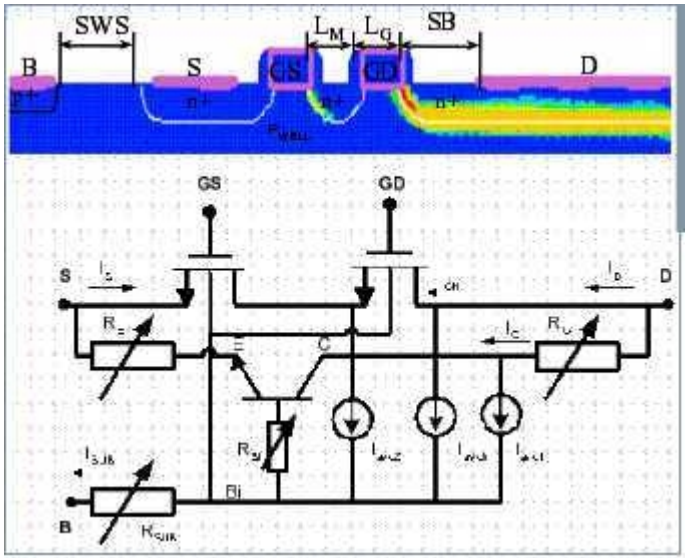
Spice and ESD data show significant mismatch in 4 out of 5 IV regions important for ESD diode application

ESD protection for High-Voltage and mixed signal

ESD protection for mixed signal

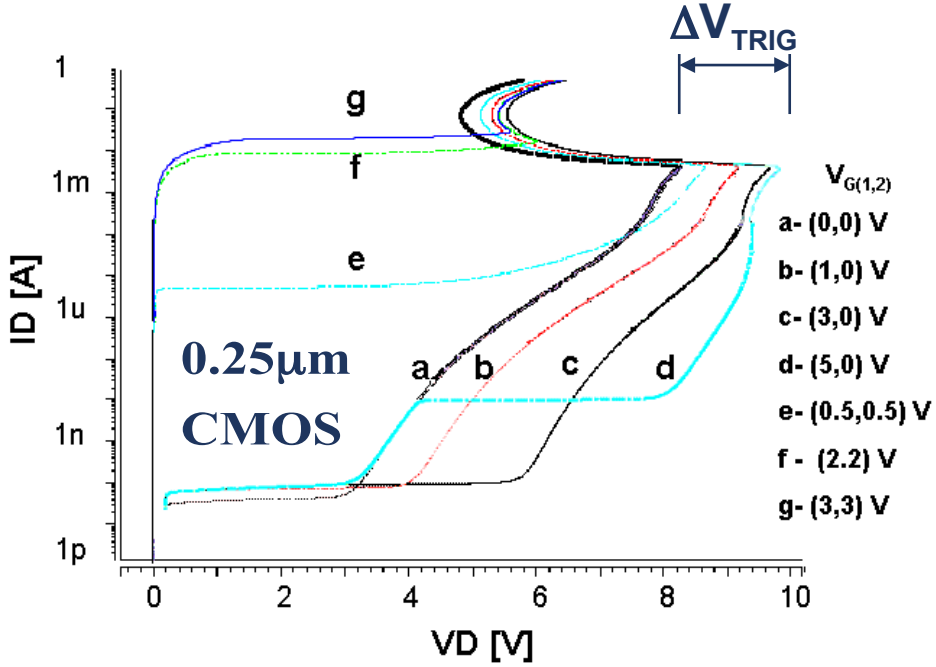


IO buffer



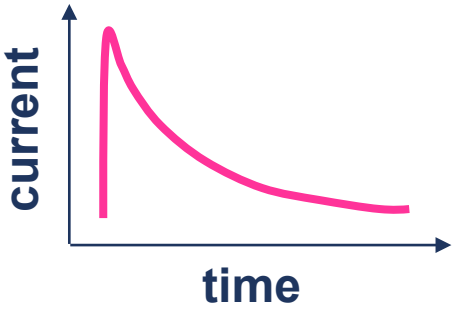
Cascoded ESD NMOS cell

Example: SPICE level model for cascoded NMOS devices used in 5V tolerant IO buffer in a 3.3V CMOS technology

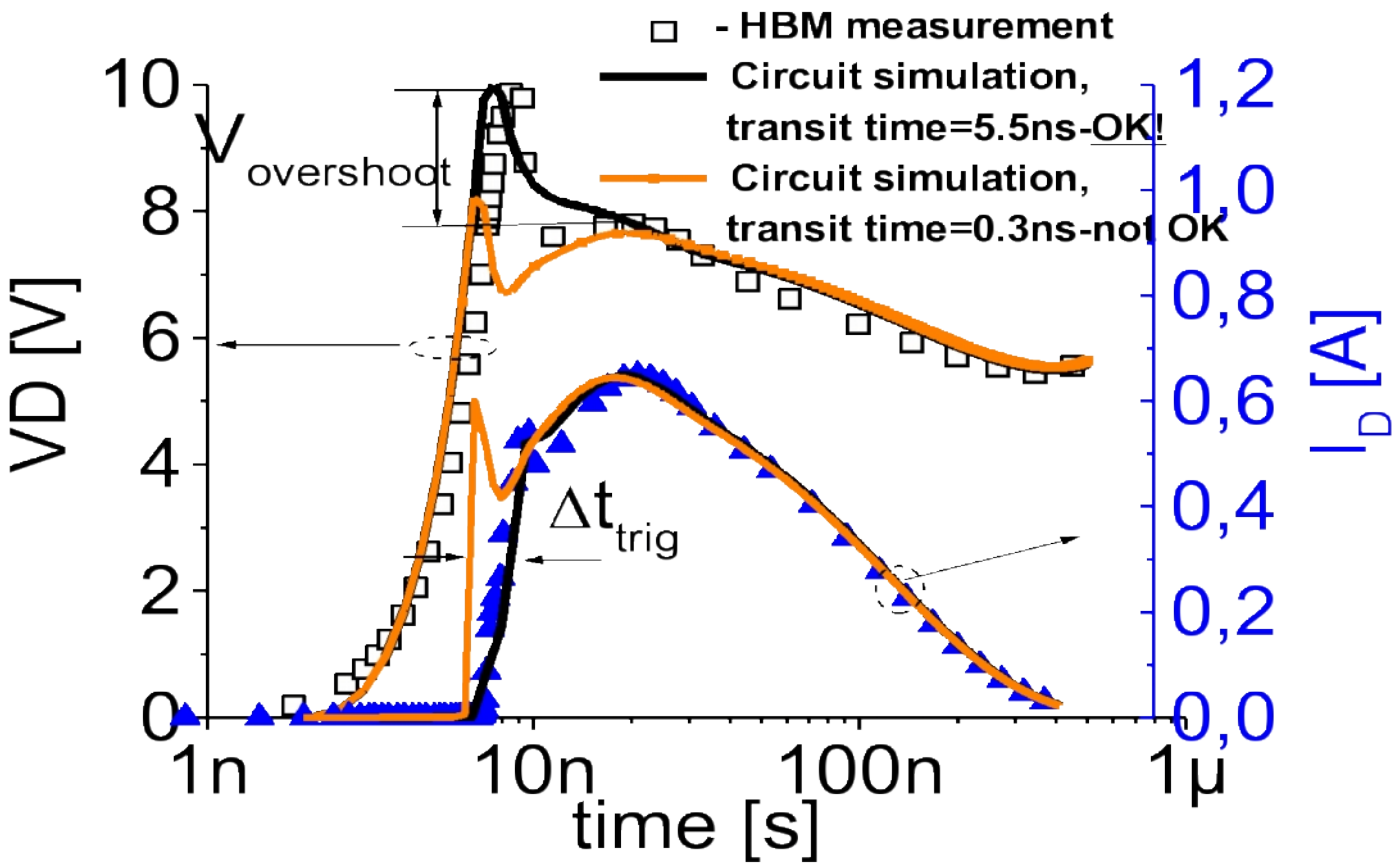


ESD cascoded NMOS model : the gate bias on each of the two gates affects the ESD performance and needs optimization in real stress conditions

1kV ESD HBM stress IO PAD vs. ground

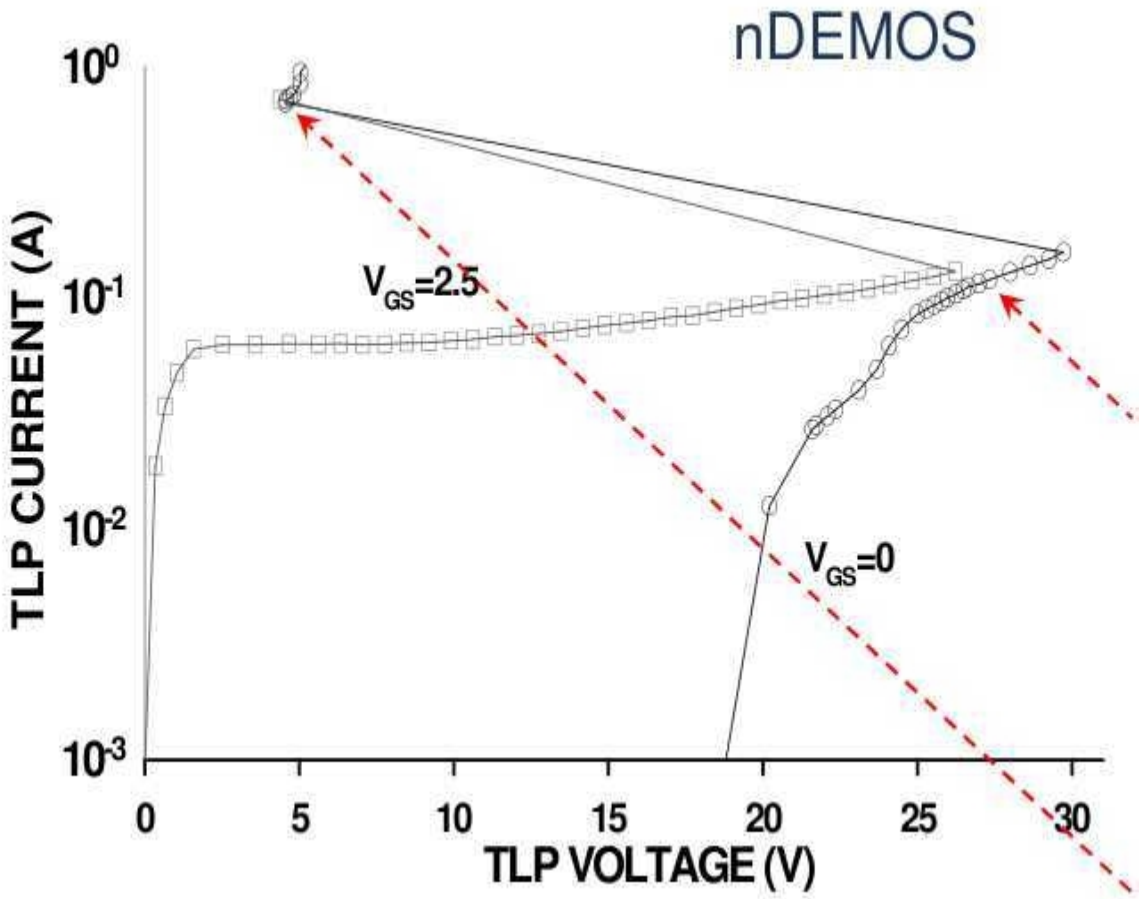


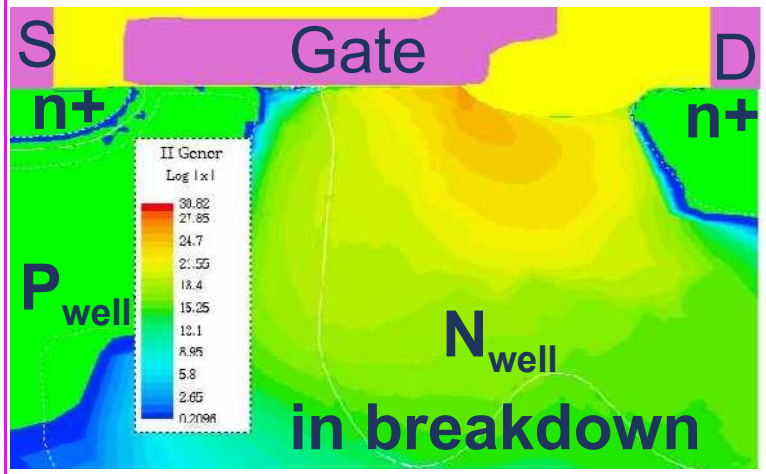
ESD HBM stress waveform



Using calibrated ESD circuit models, it is possible to precisely simulate the transient voltage overshoot *Vovershoot* and the trigger delay time Δt_{trig} of the ESD protection cell. This is very important for the <u>circuit level optimization</u> of the ESD operation speed in any design

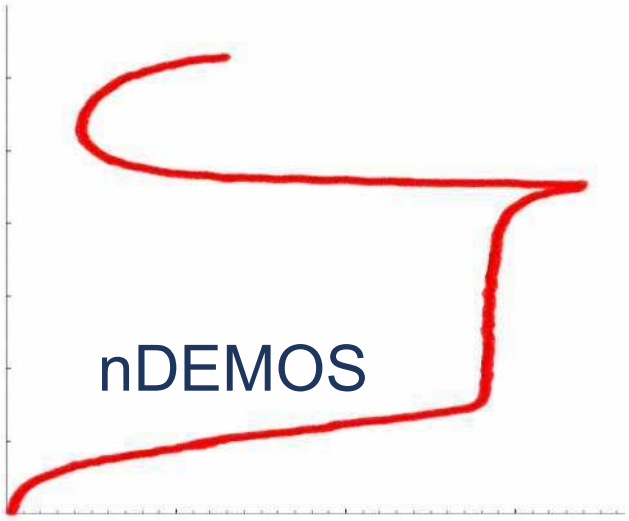
The development of new ESD circuit models for the nDEMOS and nDEMOS-SCR cells

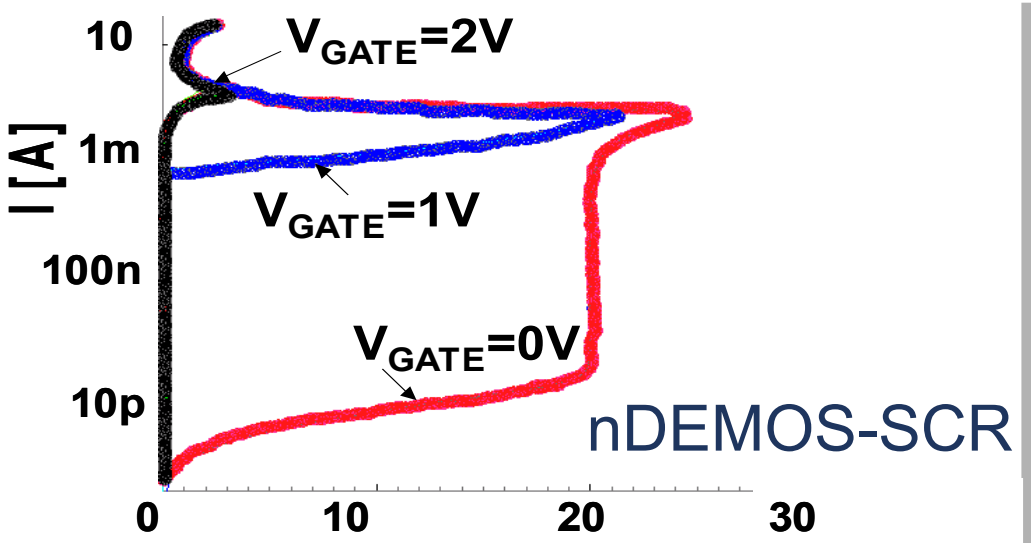


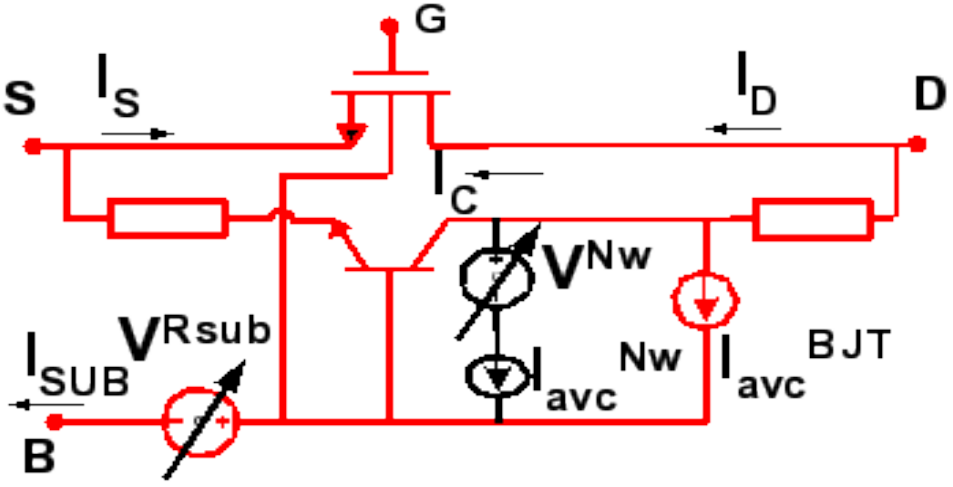


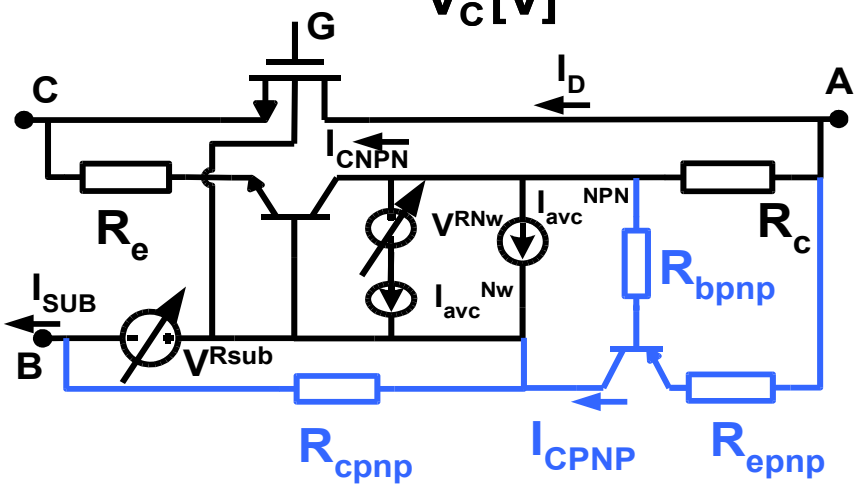
Parasitic bipolar operation, conductivity modulation and base push-out are the main effects to model

The ESD circuit models for nDEMOS and nDEMOS-SCR



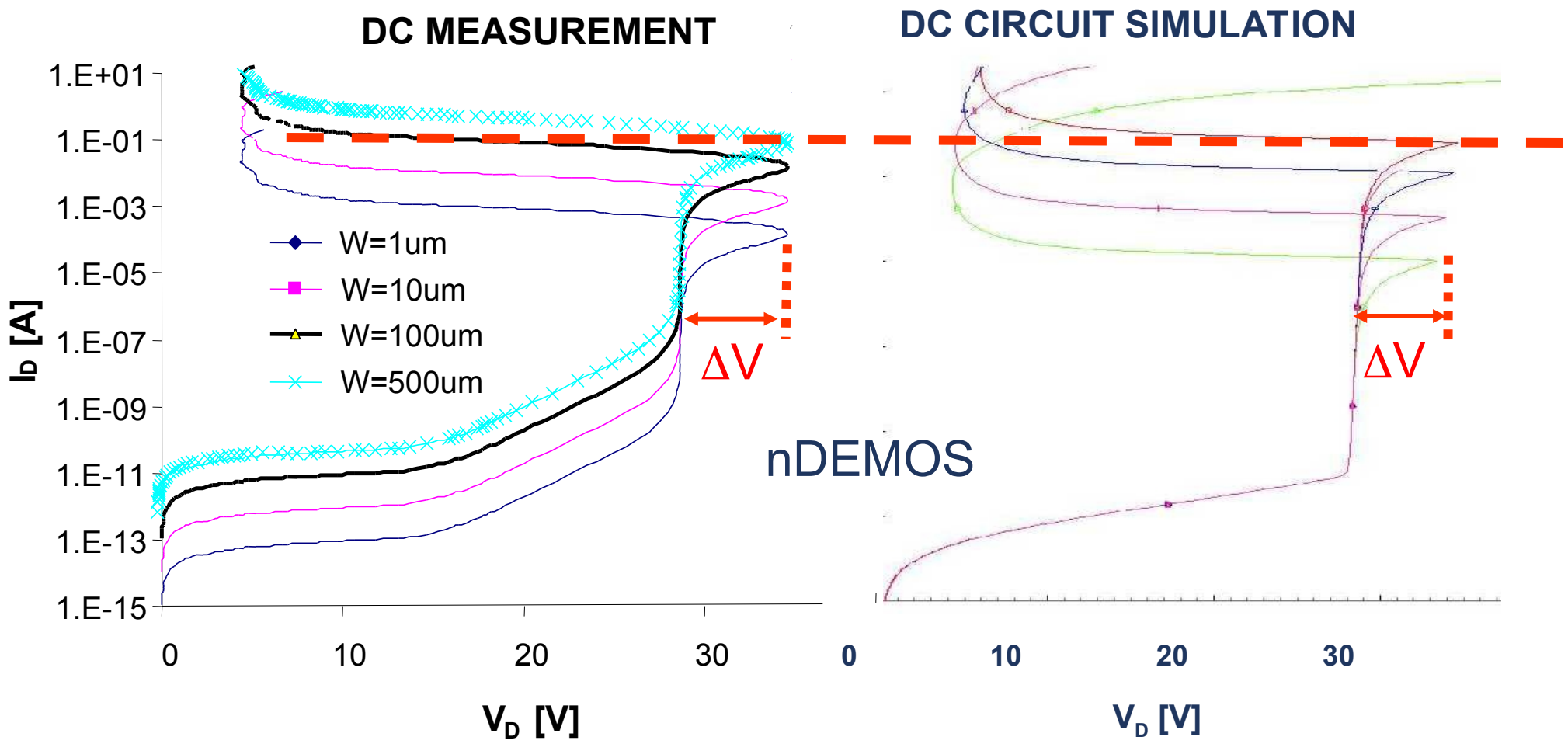






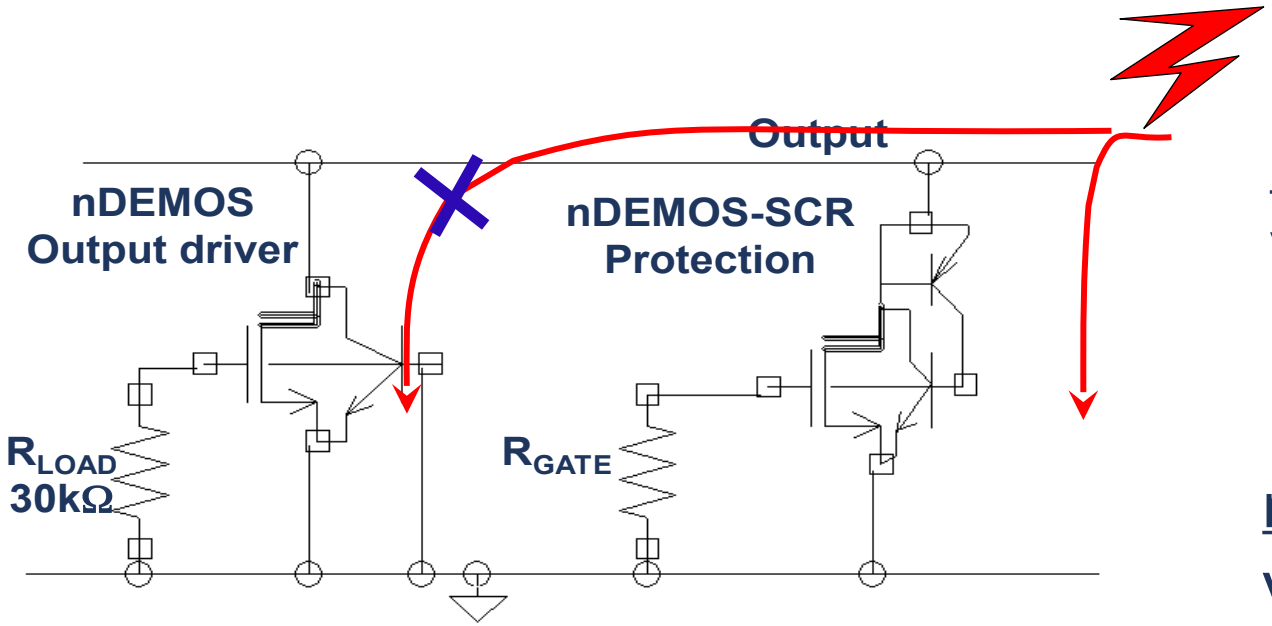
The equivalent circuit modelling approach allows to easily represent all the necessary physics and model behaviour

The ESD circuit models for nDEMOS and nDEMOS-SCR – model validation against Experimental data



The complex snapback behaviour of the devices is well represented with the circuit models. For example, the high shown ΔV ~ 10V can not be obtained with previous ESD models

Application Example – Power Output cell protection



nDEMOS

Vt1 ~ 30V

It2 ~ 0

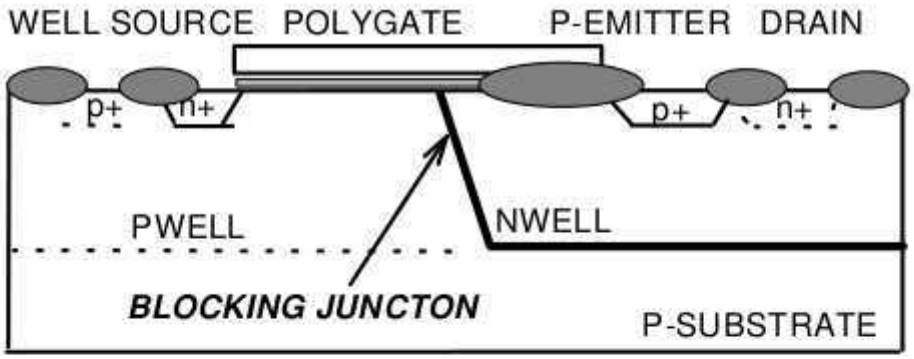
nDEMOS-SCR

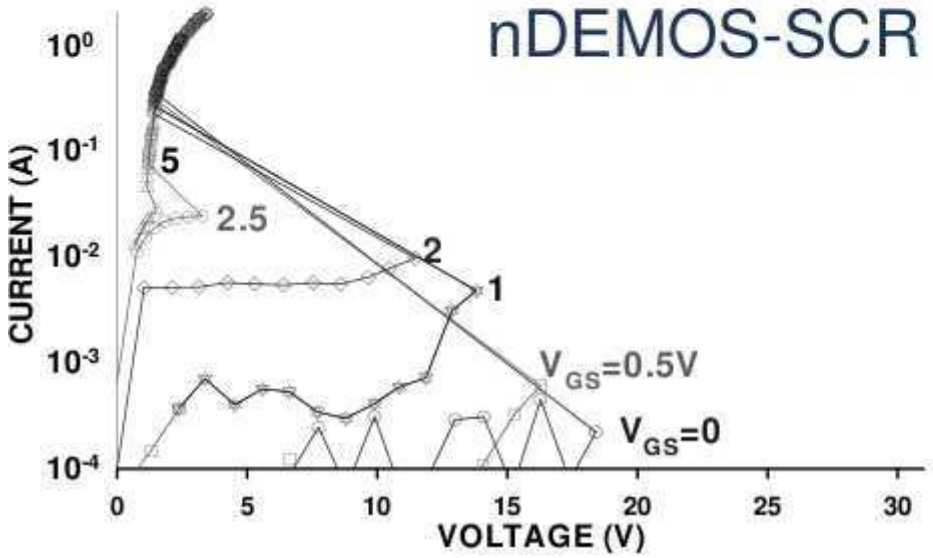
Vt1 ~ 25V @ Vg=0V

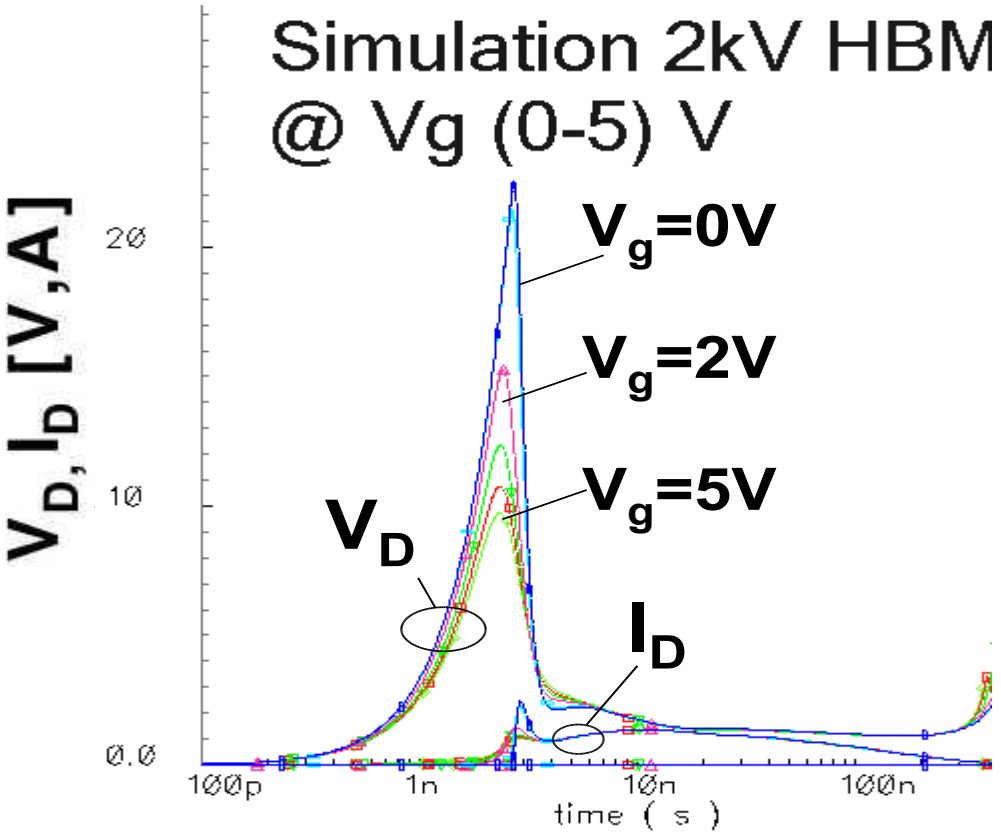
Vt1 ~ 5V @ Vg=2.5V

The ESD protection of open drain high-voltage drivers is challenging due to the small ESD design window. No ESD stress current is allowed to enter the nDEMOS output driver, which conditions needs to be optimized with the ESD protection

Application Example – Power Output cell protection





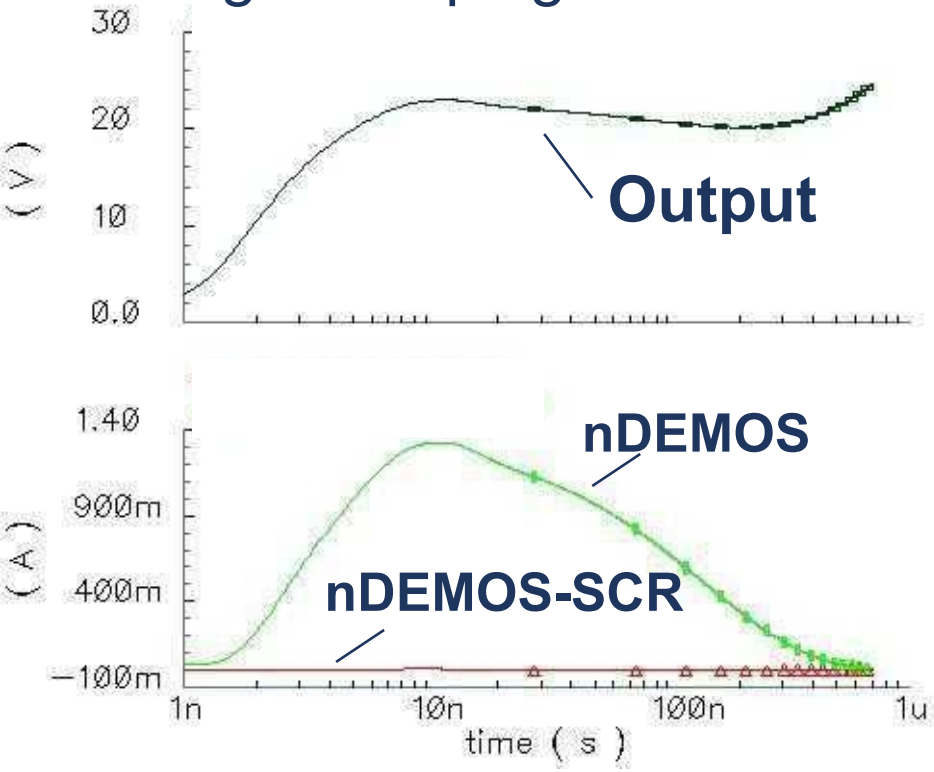


Introducing gate bias coupling during the ESD event improves the HV SCR trigger speed and voltage overshoot Vg. To optimizie the circuit, the new HV ESD compact models are needed

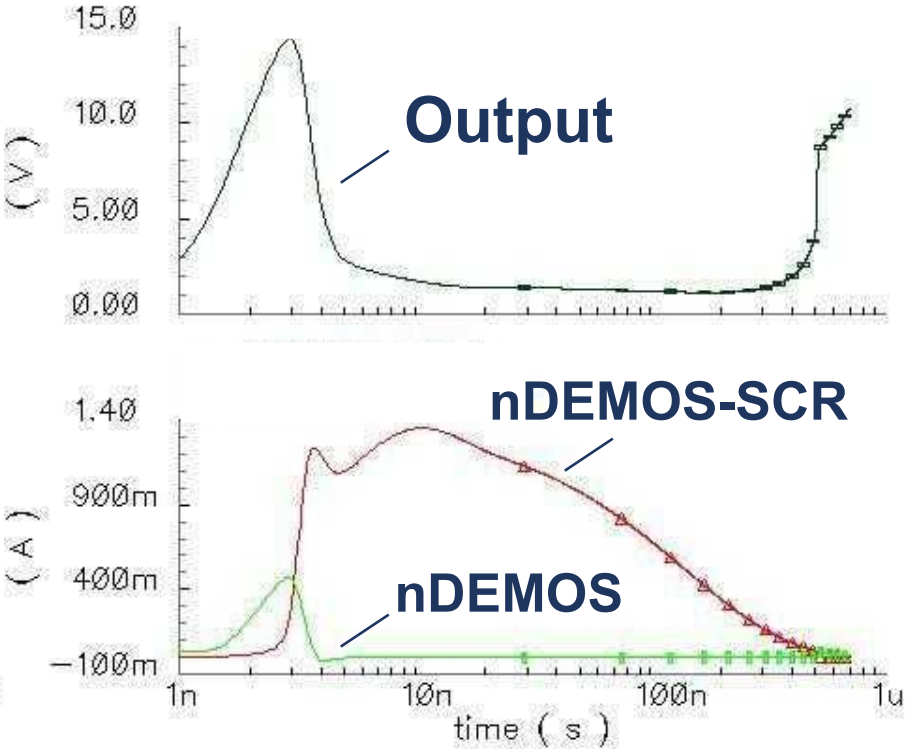
Application Example – Power Output cell protection

2kV HBM Simulation

R_{GATE}=1kΩ - not OK, no voltage clamping



R_{GATE}=10kΩ - **OK**, good voltage clamping

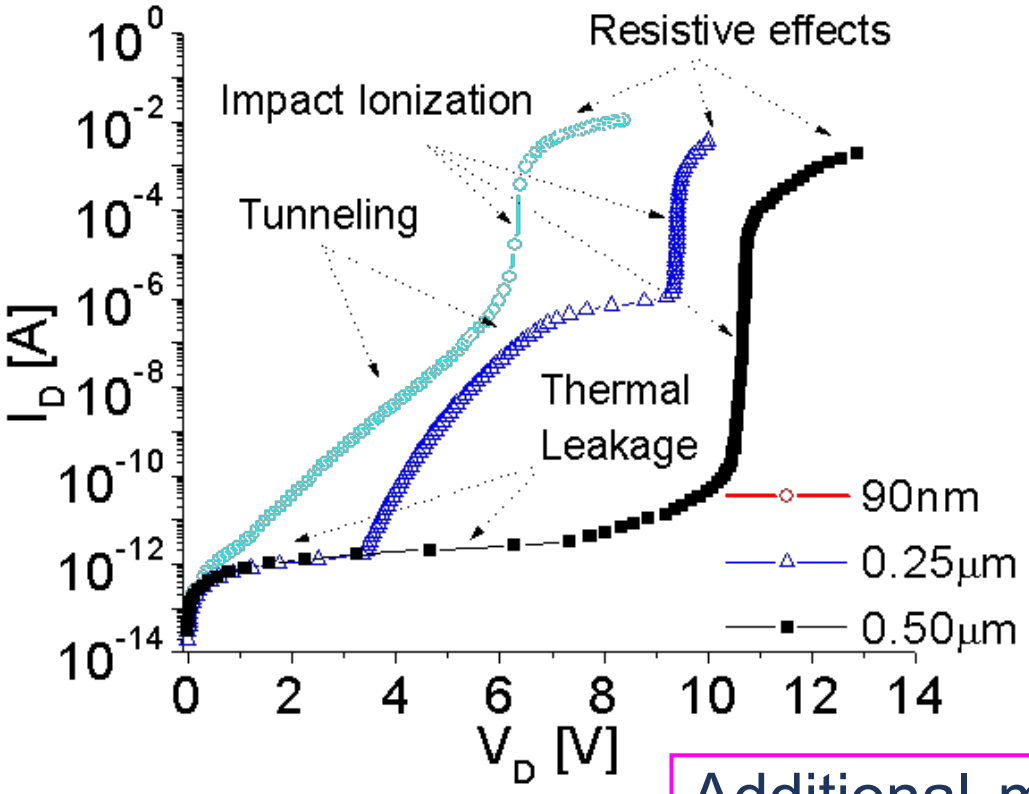


The new ESD device models allow to tune the triggering to achieve maximum ESD performance of the full cell

Special Topic: Accurate modelling of the reverse biased junction leakage currents

Special topic: reverse biased p-n junction leakage model

Impact of the CMOS technology on the junction breakdown



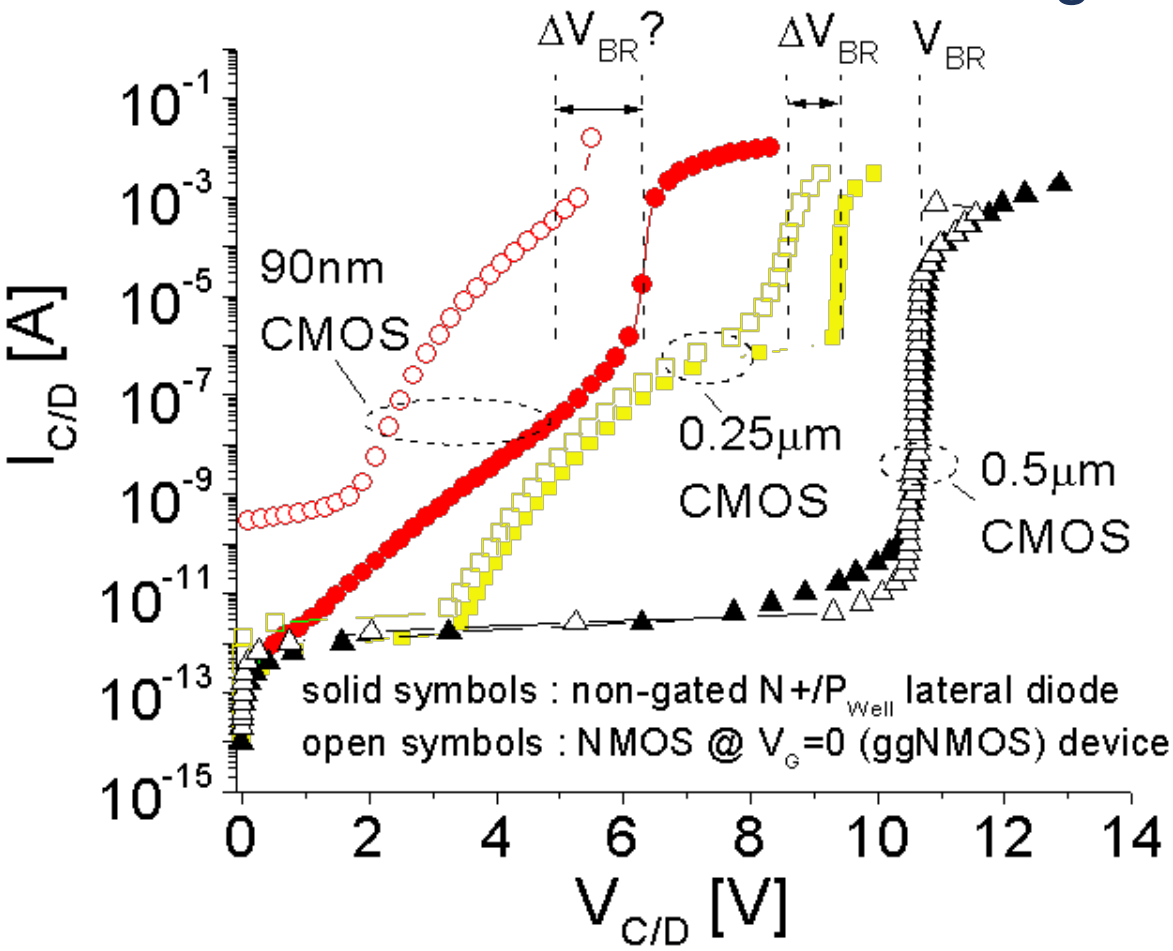
N+/P_{well} junction in reverse bias

The CMOS downscaling leads to:

- ✓Reduced avalanche breakdown voltage
- ✓Increased tunneling leakage currents
- ✓Less importance of the high-injection effects

Additional models beside avalanche need to be considered to describe the junction reverse bias conduction in the presence of gate field!

Impact of the CMOS technology on the junction breakdown behaviour: effects of the drain-gate field



The reverse bias conduction of the gated N+/P_{well} junctions is becoming increasingly dependant on the gate bias !

N+/P_{well} junction in reverse bias conditions

Application Examples: real world IC design optimization for ESD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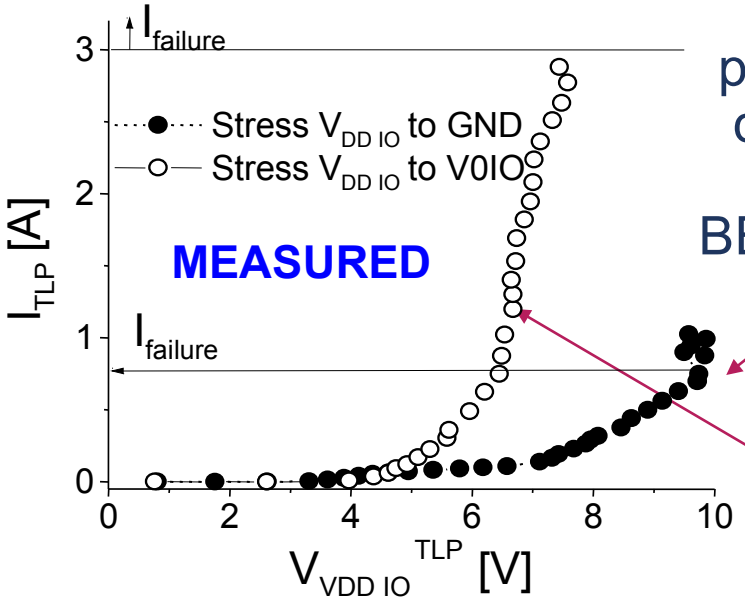
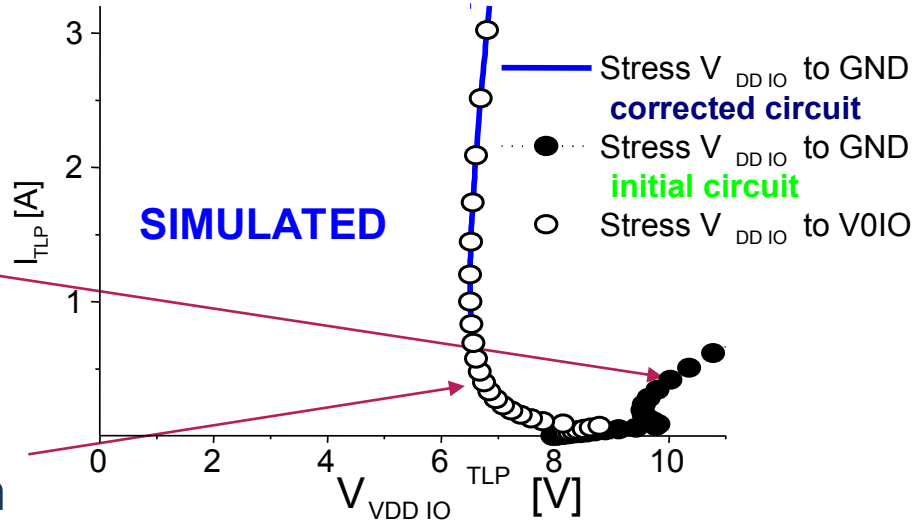
Optimisation of the ESD behaviour of a Power Supply Pad

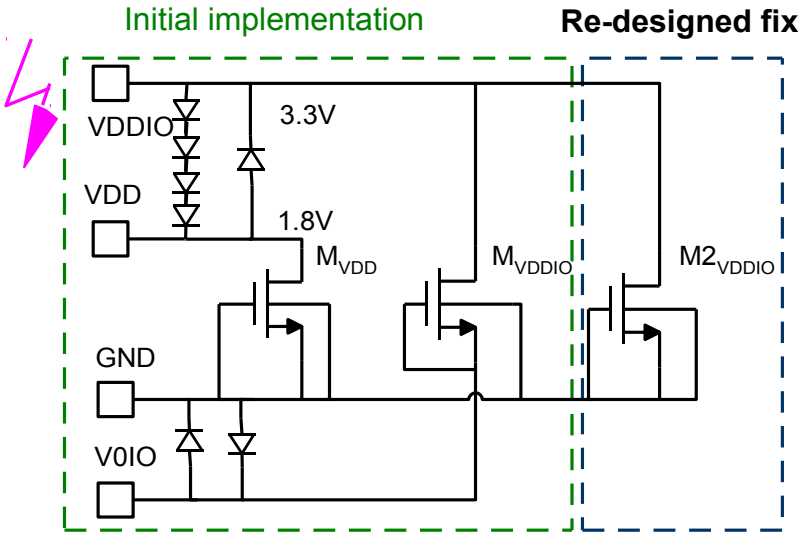
The MEASURED and the SIMULATED ESD performance IV's for a power supply pad ring cell design



protection does not trigger, BEFORE fix

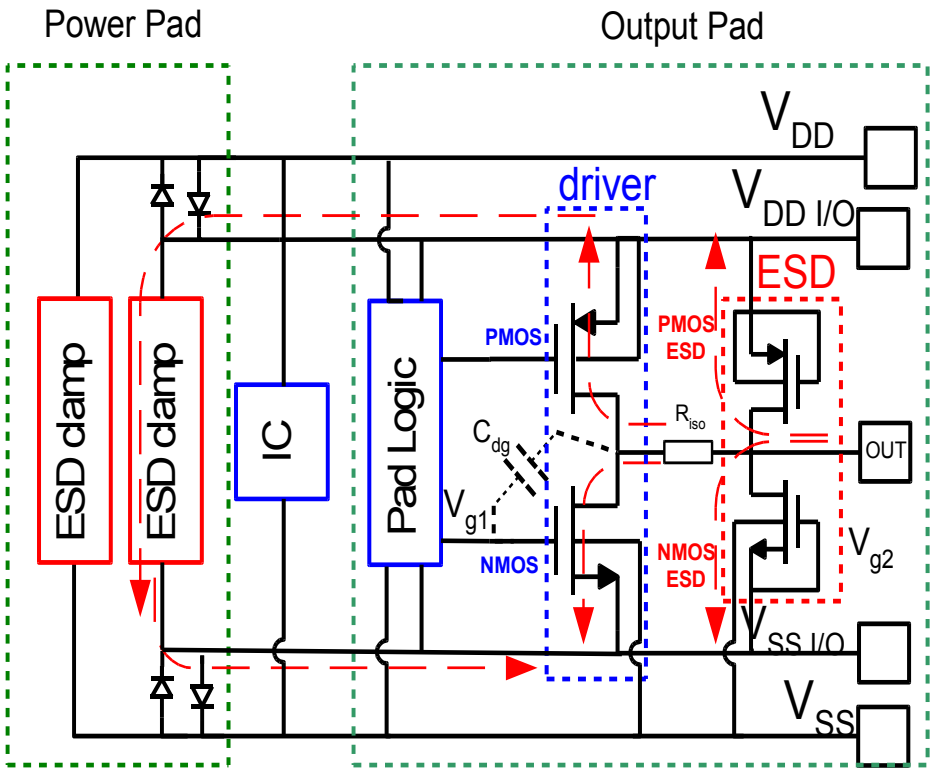
Good operation AFTER fix



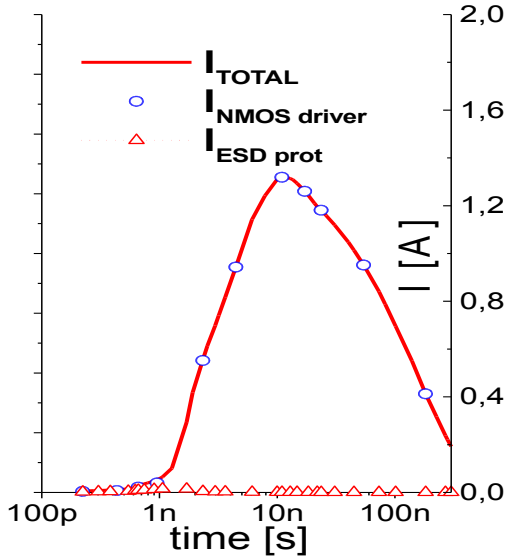


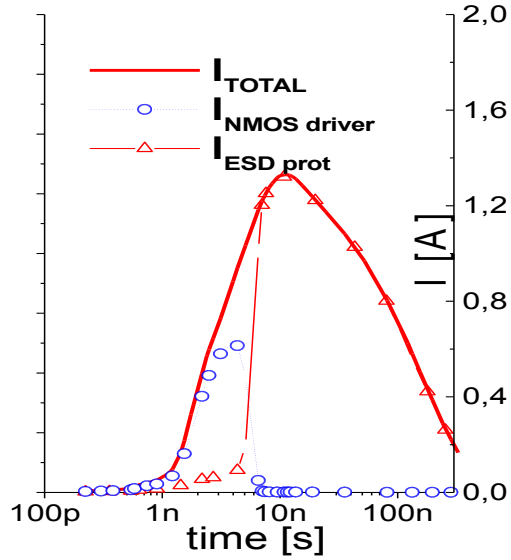
The excellent correlation between the measured and SPICE simulated circuit behavior of an I/O pad cell under ESD conditions illustrates the predictive simulation capabilities of the NOVORELL's ESD EDA tools

Optimization of the ESD protection in a digital Output Pad



2kV Human Body Model ESD stress between OUTPUT and VSS IO





Initial design (no gate coupling)

The ESD protection is too slow and does not activate, the output NMOS takes all the stress – not OK

Improved design (fixed RC gate coupling

The ESD protection activates OK and conducts all the ESD stress current after 10ns

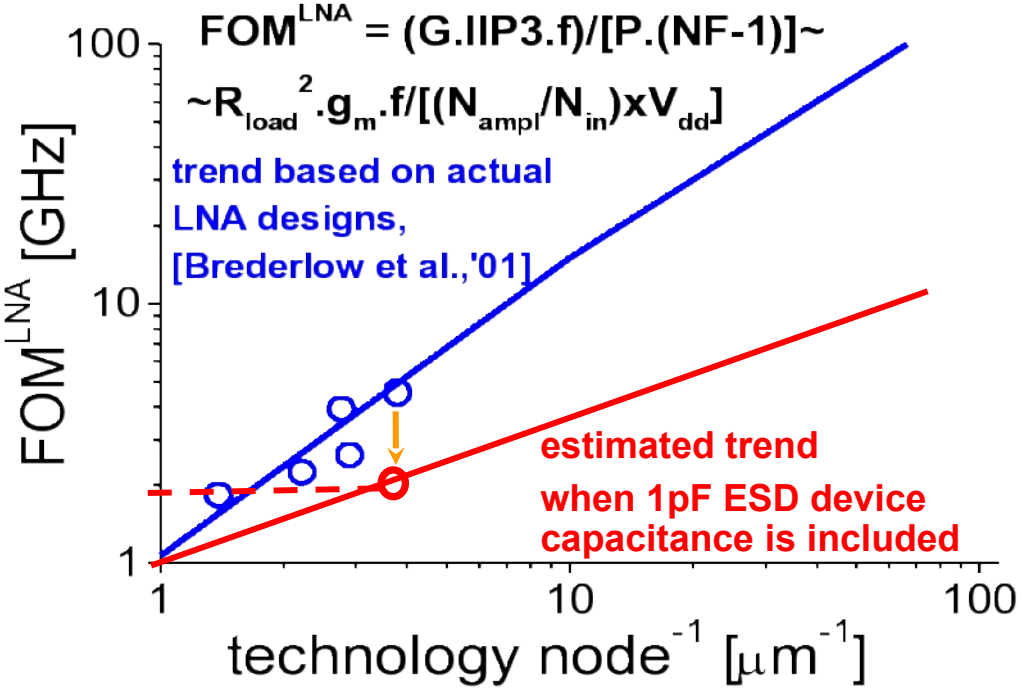
The use of ESD simulation enabled PDK allows to optimize and verify the operation of the ESD protection circuit prior design release

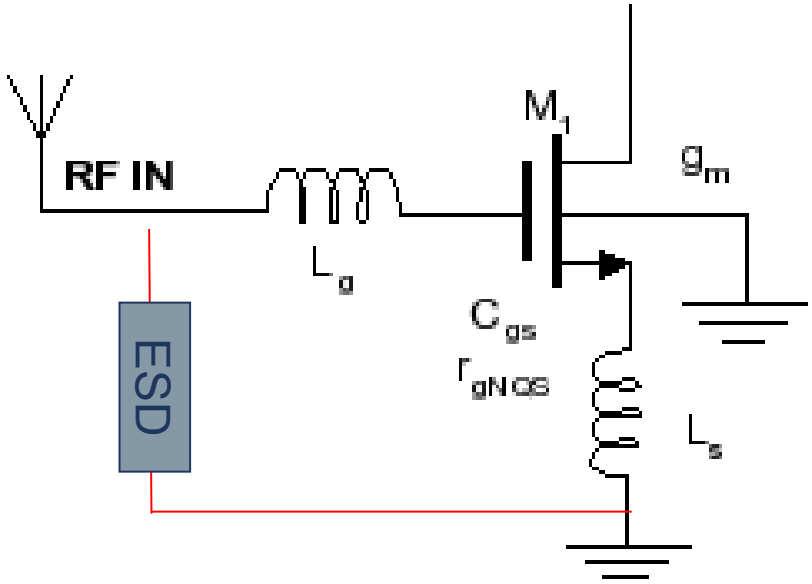
ESD protection for RF I/O's ...

ESD protection for RF I/O's

Problem:

- The parasitic RC behaviour of the ESD protection devices can not be tolerated by the RF circuits and RF product market requirements



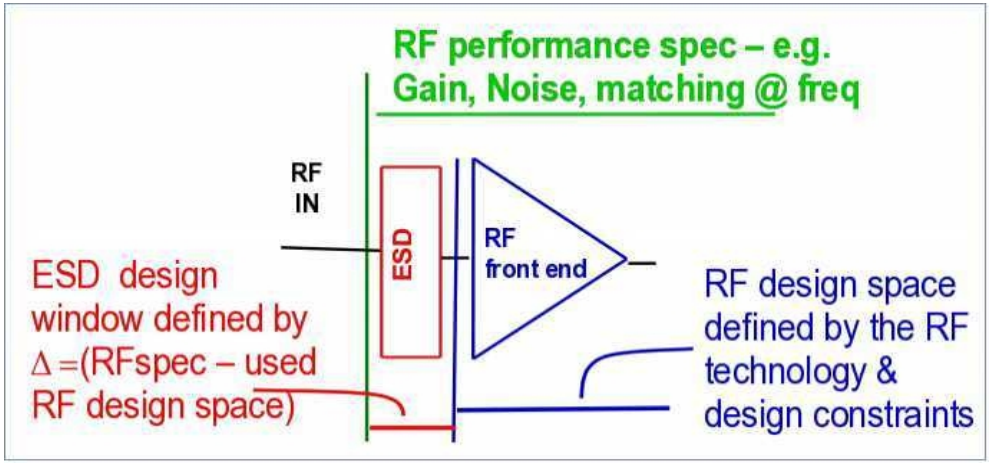


The RC parasitics of the ESD structures decrease the RF circuit performance - reduce gain,increase noise, etc. It is needed to be able to model the RF behavior of the ESD structures

Two possible ESD-for-RF Design Methodologies

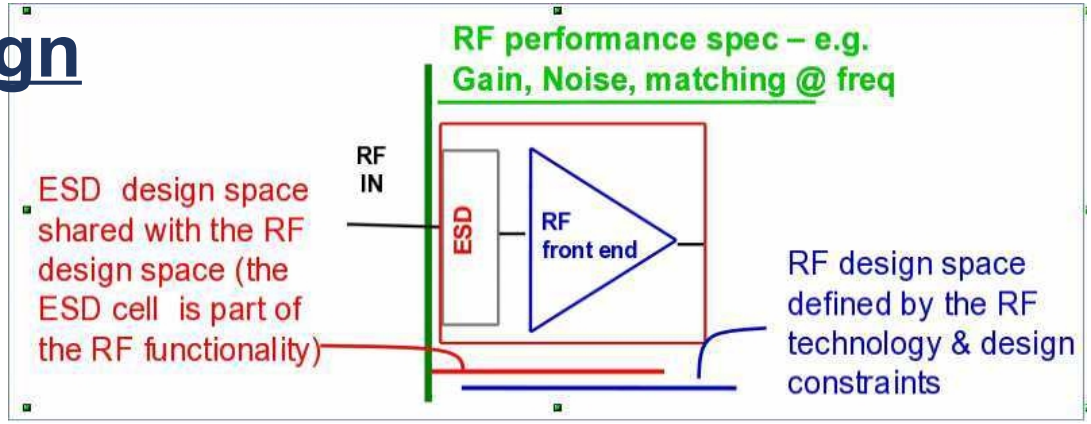
'Plug and Play'

independent RF and ESD designs; fit (shrink) ESD devices into the available RF design window to meet the RF specs; Limited ESD performance possible



ESD-RF Circuits co-design

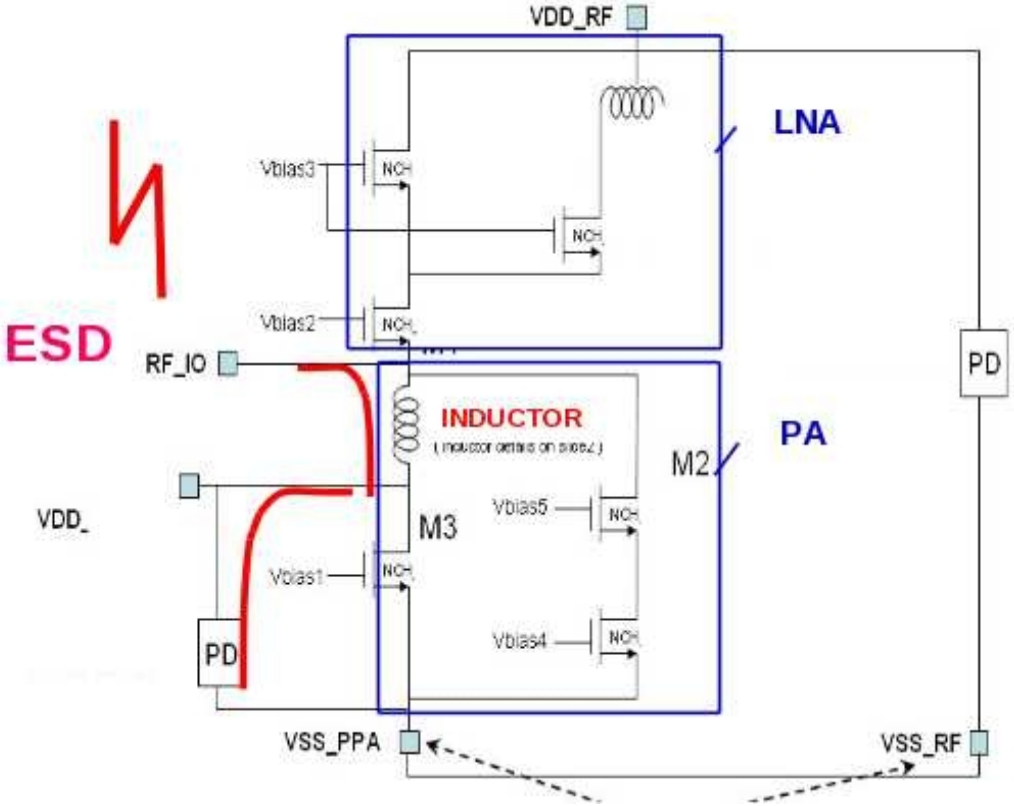
full circuit optimization; ESD structure is part of the RF design space, thus stronger ESD cell can be used. HIGH RF ESD specs can be achieved



Depending on the design space and specific RF product spec, different ESD approaches are feasible

ESD protection for RF I/O's - Co-Design

EXAMPLE : ESD protection for a 65nm Bluetooth transceiver operating at f_o=2.4GHz

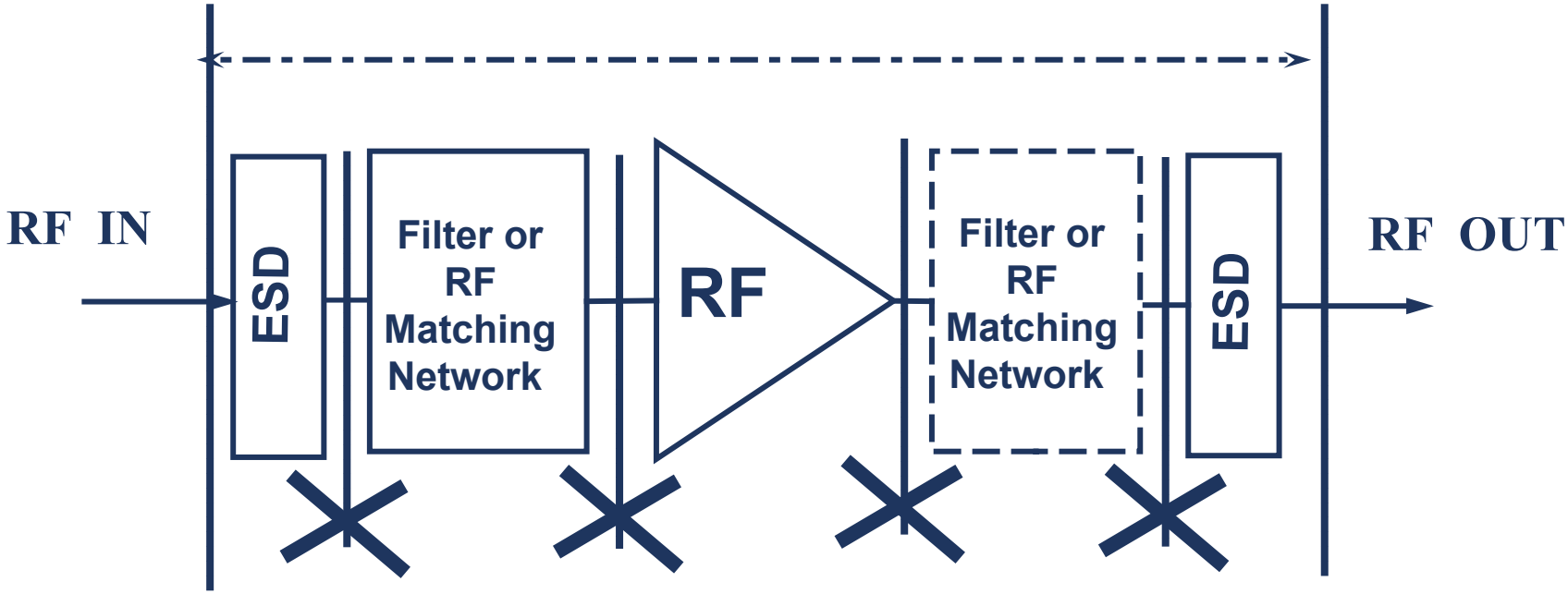


-The ESD current is conducted through the shared LNA / PA inductor
-The inductor is approximately short circuit for the ESD strike, conducted also through the ESD cells in the non-RF pins

-Verified by ESD simulations (HBM and CDM) and product results- meets RF ESD spec of 500V CDM and >1kV HBM
-Reduced CDM sensitivity due to new RF circuit topology

NOVORELL's ESD for RF know-how allows providing in-spec ESD protection levels for the RF IP's

50 Ω environment @ f_x @ NF @ Gain @ …

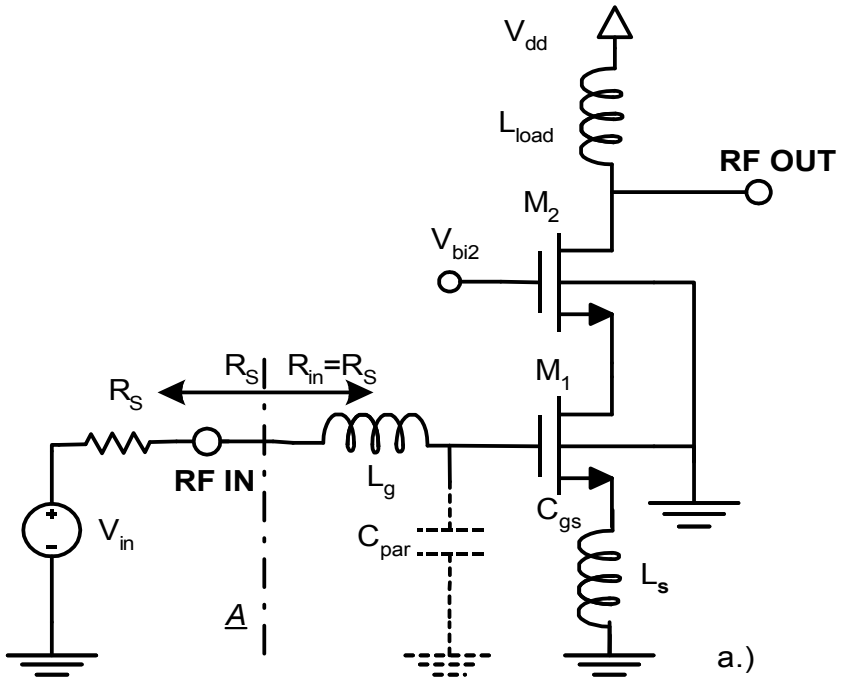


Integrate the ESD (and package) RLC parasitics in the RF functionality (signal path)

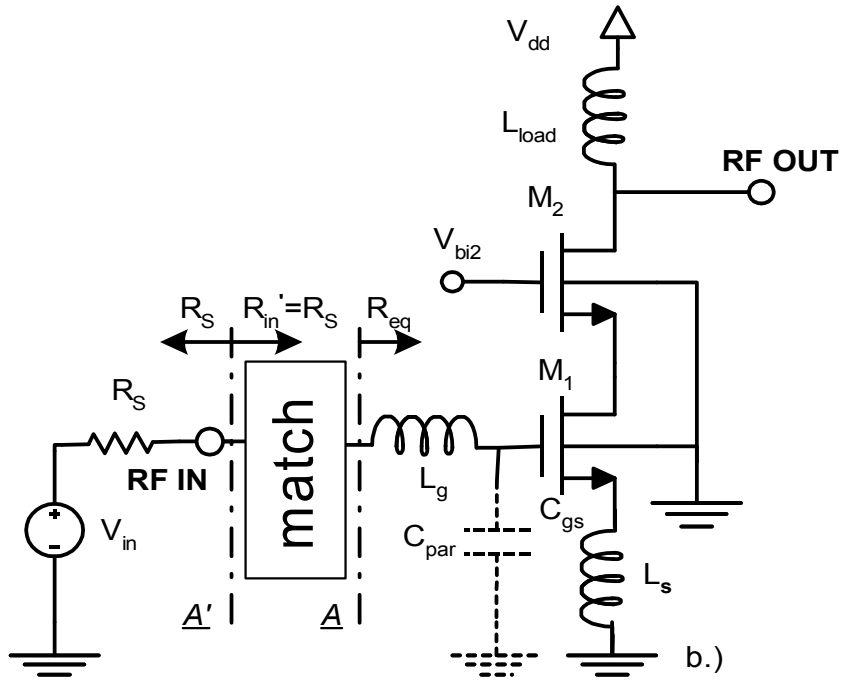
ESD - RF co-design methodology

- The I/O matching blocks are the natural place to integrate the ESD parasitics - increases the ESD design window!
- Resonant cancellation of the parasitics: common for narrow band transceiver design
- Needs accurate (incl. non-idealities) and flexible (scaling) RF models for both core and ESD components
- Feasible solution for the 5-10 GHz applications

Generic common source LNA matching approach



direct match

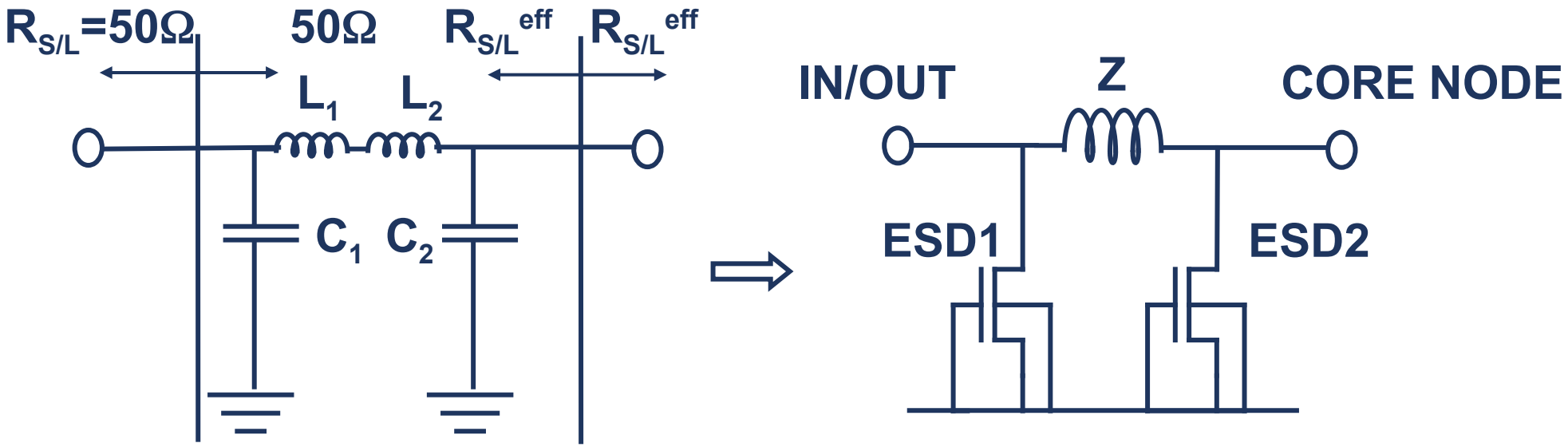


indirect match

The presence of the ESD device imposes an upper limit on the allowable Rin; power match is not always possible

$$R_{in}(=R_s) \leq \frac{1}{2\omega C_{par}(1+\frac{C_{par}}{C_{gs}})}$$

Examples of matching blocks useful in ESD



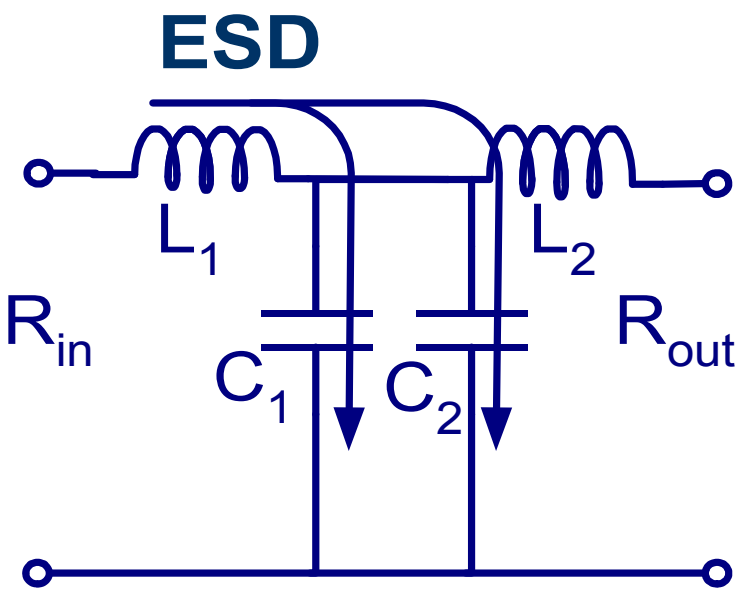
π-type matching:

allows to independently set ω_0, $R_{S/L}$,$R_{S/L}^{eff}$, Q

acts as low pass filter (for off-chip ESD protection)

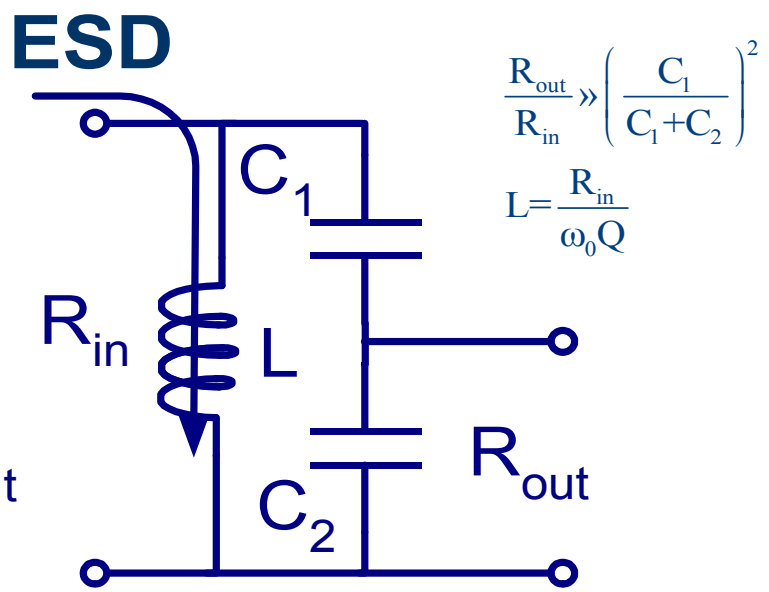
very robust ESD circuit !!!

Examples of matching blocks useful in ESD



T-match
(ex. PA outputs)

$R_{in} > R_{out}$



$$\frac{R_{out}}{R_{in}} \gg \left(\frac{C_1}{C_1 + C_2} \right)^2$$

$$L = \frac{R_{in}}{\omega_0 Q}$$

Tapered capacitor match
(ESD prot. for future high ω appl.)

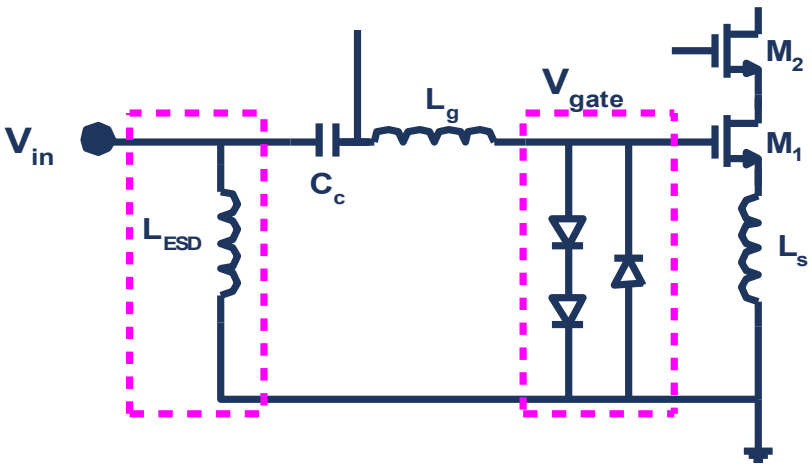
There are various possibilities to integrate the ESD RLC in the I/O matching blocks!

Shunt inductor solutions: Input gate oxide degradation

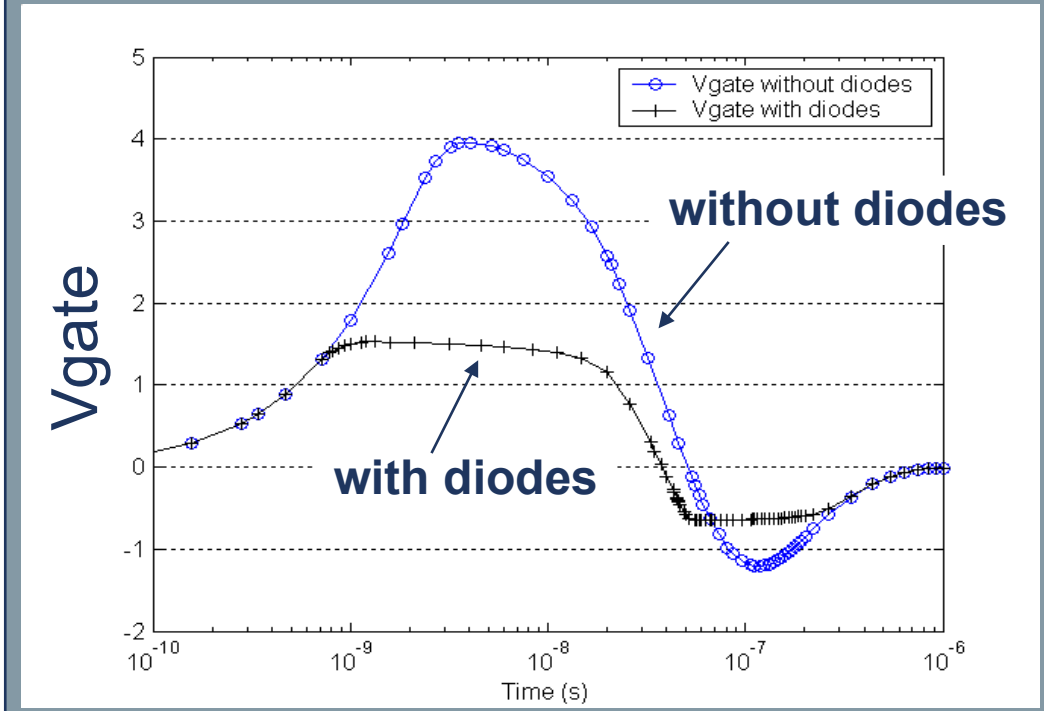
Solution: use small diodes to clamp gate voltage

- Diodes do not have to conduct any significant current (few mA during few ns)
- Can be sized very small: 4x2 µm², 11 fF
- Load on the gate: 16.5 fF

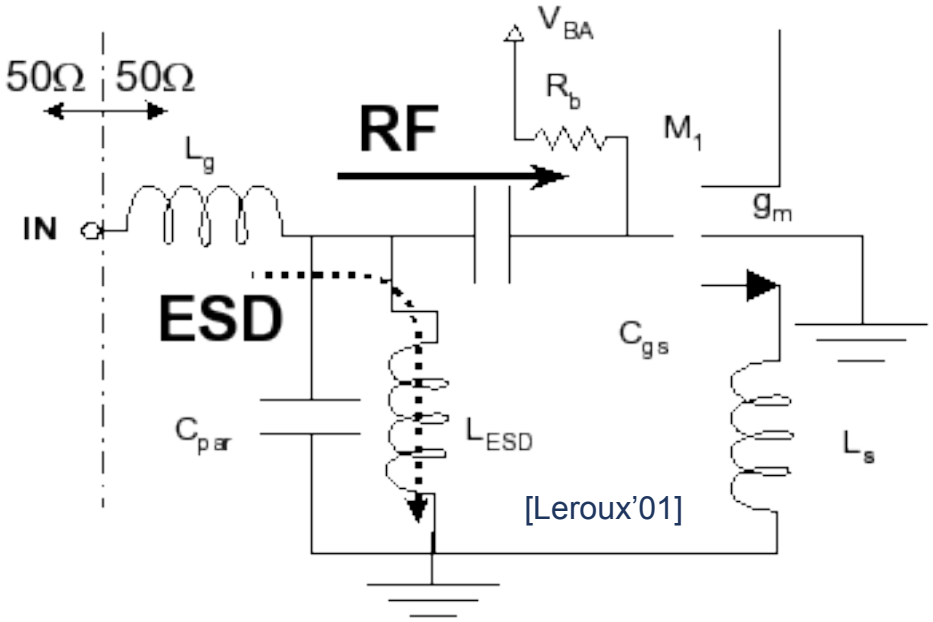
No RF degradation

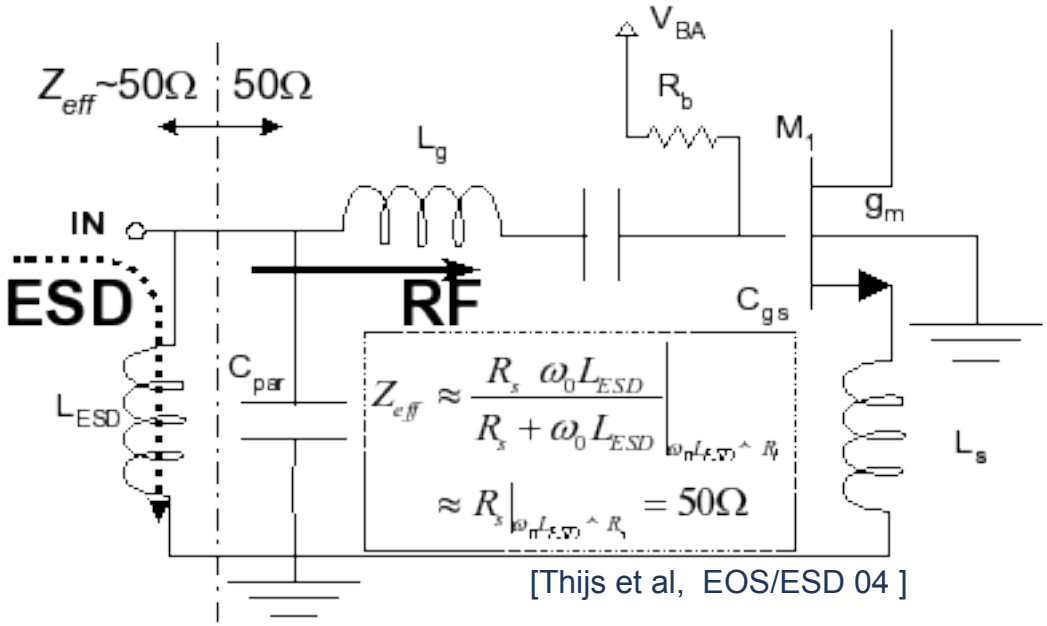


2 kV HBM simulation



Shunt inductor solutions



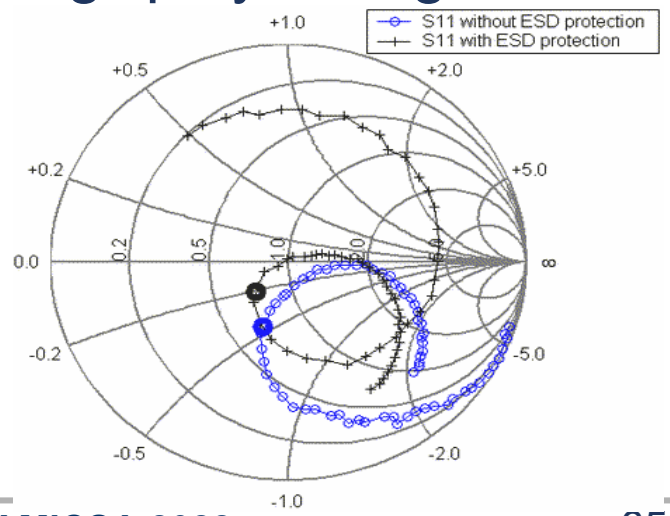


Integrated in the input matching

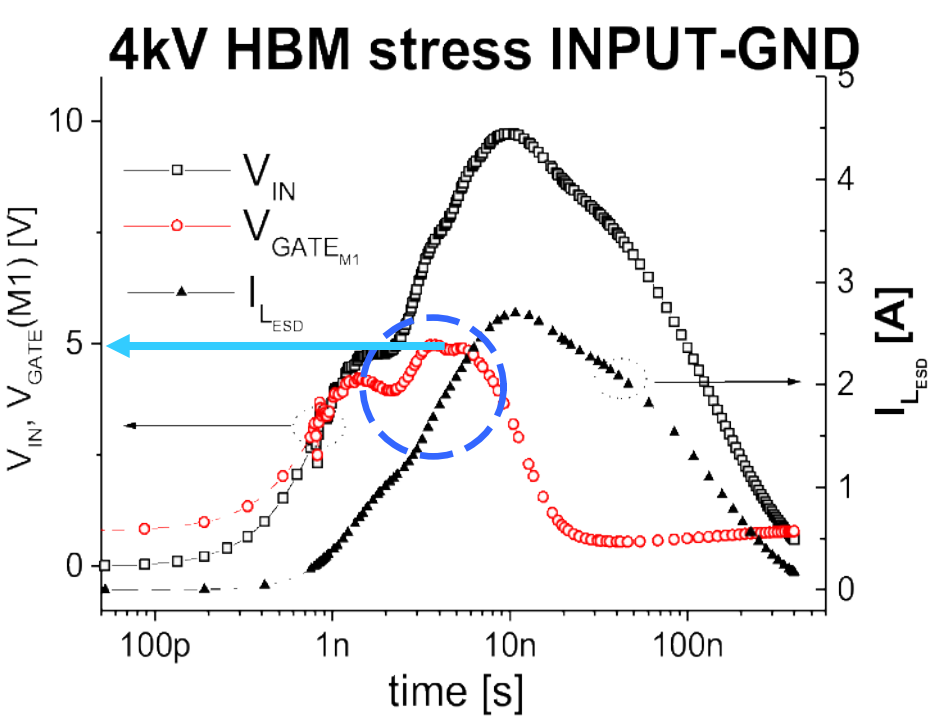
'plug&play' design

Known difficulties

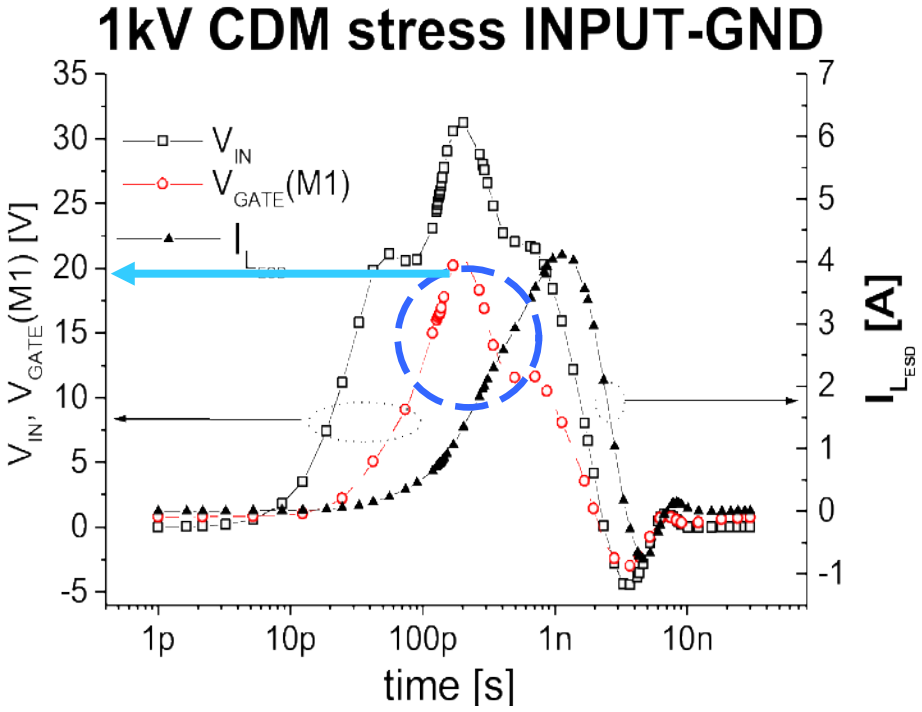
- CDM overshoot
- Input gate oxide degradation danger



Shunt inductor solutions: CDM problem



HBM- OK!

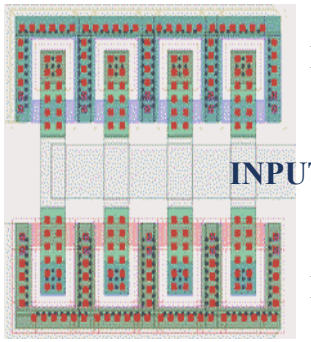


CDM – NOT OK!

In CDM conditions large transient overshoot may appear at the input gate due to the high CDM ESD frequency component that prevents the clamping of the ESD pulse by the protection inductor

Case study: diode protected CMOS GPS LNA

Input protection diodes design



- Large current handling → large perimeter
- Small capacitance → small area

⇒Multiple finger diodes

- Sufficient contacts and vias per finger

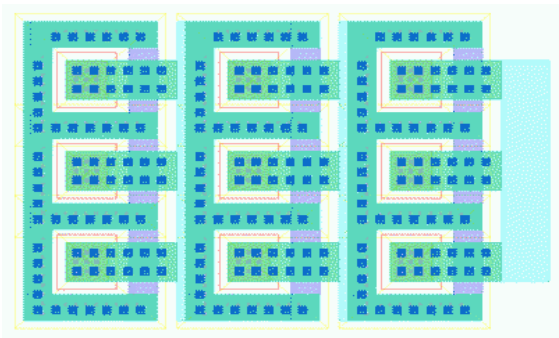
Stripes

- ⑤ Lowest resistance
- ⑤ Current crowding

Squares

- ⑤ Higher resistance
- ⑤ Uniform distribution

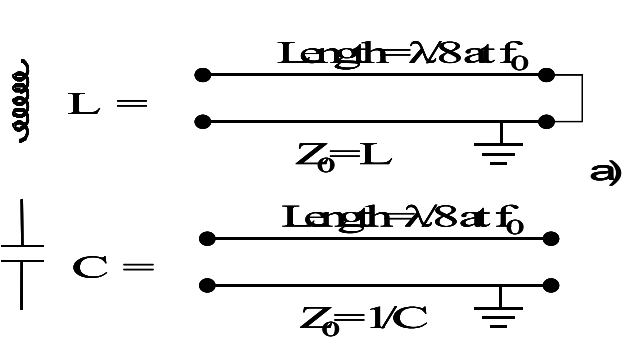
Design of $V_{DD} – V_{SS}$ diode stack



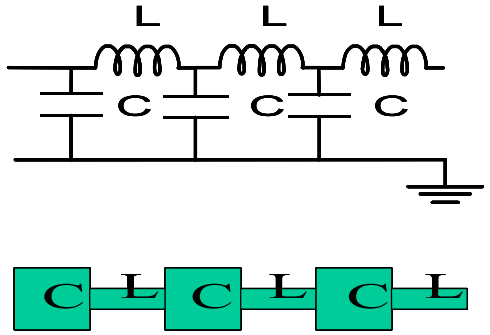
- Diodes in series
  - p+nwell diodes are pnp transistors
- Design based on current leakage specification
- Capacitance irrelevant

Other solutions : shorted stubs

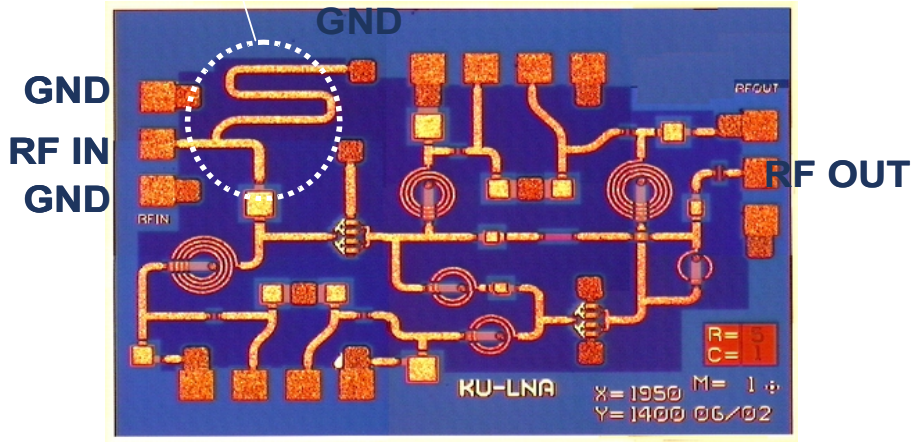
ESD feasible approach only if $\omega_{ESD}L_{ESD}$ is negligible, otherwise high voltage overshoots possible during ESD)



a)



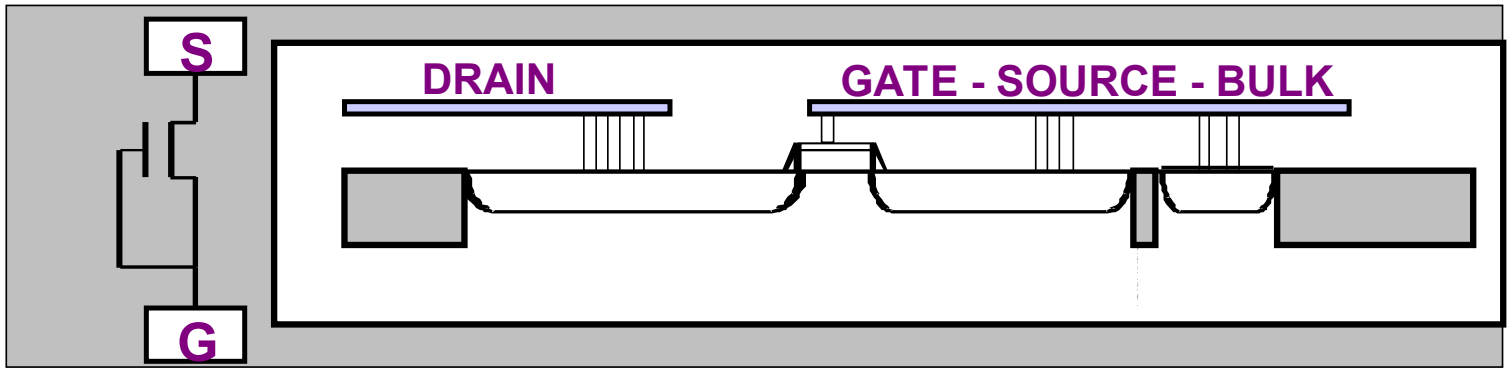
shorted TL (stub) f_0=11-12GHz



[Park, in *Proc. IEEE MTT-S*, June 2003]

For the $f_0 \geq$ 10-15 GHz applications, it becomes feasible to separate the RF and the ESD signals (f_{CDM} < 1-2 GHz) using small value reactive components to ground e.g. lumped inductors or shorted stubs (TL) with $Z_{ESD} \rightarrow 0$ and $Z_{RF} \rightarrow \infty$

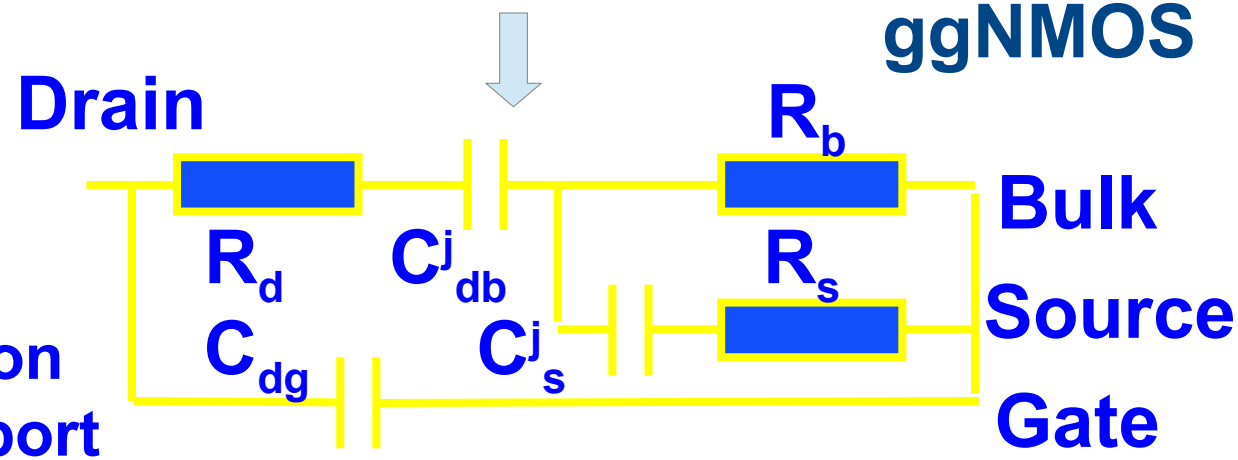
Small signal modeling of the ESD devices for RF



ggNMOS

= potential barrier

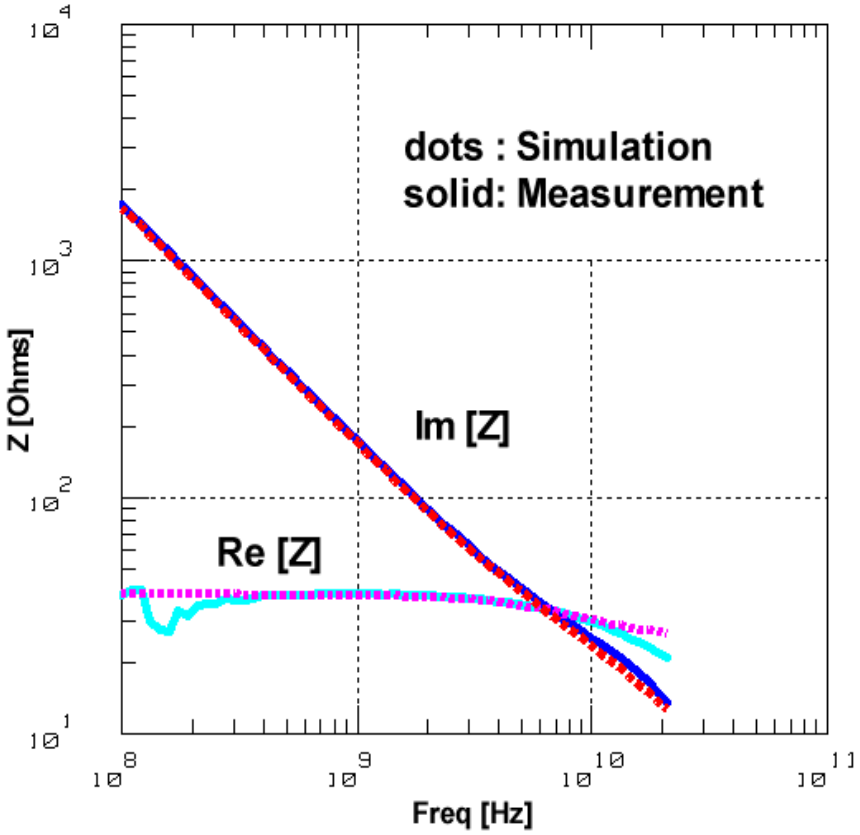
= drift-diffusion charge transport



For accurate representation of the RF properties of the ESD structures, RC equivalent circuit modeling approach is used. These RF-ESD models allow for RF-ESD co-design

Parameter extraction approach

Example: ggNMOS



$$\frac{1}{Z^R} = \frac{\left(C^j_{db} + C_{dg}\right)^2}{(R_d + R_b)C^j_{db}{}^2} + (R_d + R_b)C_{dg}{}^2\omega^2$$

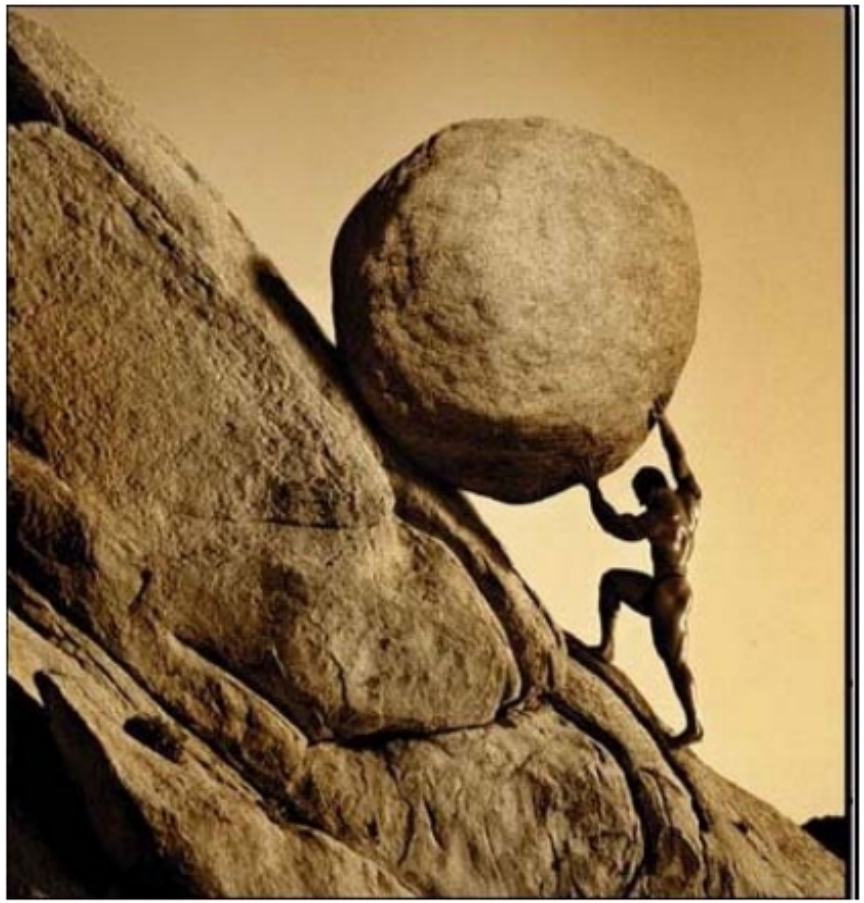
$$Q = -\frac{\left(C^j_{db} + C_{dg}\right)}{(R_d + R_b)C^j_{db}{}^2\omega} - R_d C_{dg}\omega$$

Analytical & numerical optimisation for fine tuning

Excellent RF-ESD model calibration can be achieved

ESD design verification infrastructure

Why ESD EDA Design Tools?



Sisyphus rolling a rock uphill

- Traditional DRC/LVS can complete some checks, but not all
- ***E***xtra ***S***pecial ***D***elay in Tapeout
- Manual checks can be slow and error prone
- Specialized software tools for ESD IC design have been developed to improves efficiency

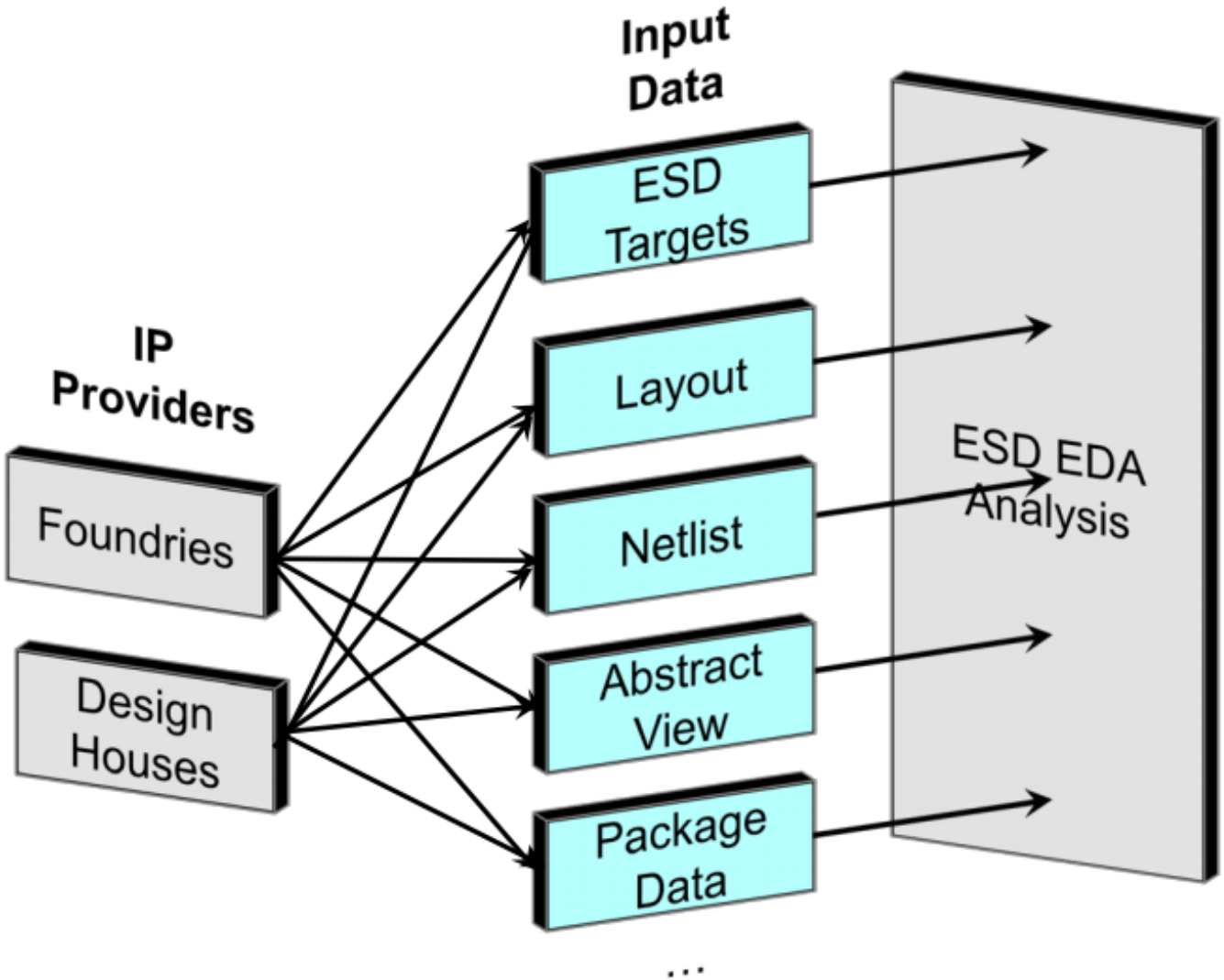
[Consiglio12]

ESD EDA Verification Flow Requirements

- ✔ Provide broad check coverage
- ✔ Allow components' verification along the progress of a design.
- ✔ Include ESD checks during all IC design phases
- ✔ Limit the required manual checks to a minimum
- ✔ Be transparent and seamlessly integrated into the adopted design flow
- ✔ Be run directly by IC designers
- ✔ Provide clear and informative descriptions of violations
- ✔ Generate reports for final design ESD sign-off

- Layout checks
- Netlist checks
- Point to Point Resistance
- Current density checks
- Simulation checks
- Macro integration checks

Input Data for ESD EDA Analysis



Need for standardized data formats

ESD Protection Strategies and Failure Conditions

1. ESD energy is shunted through ESD clamp path (protected devices cannot shunt ESD energy).

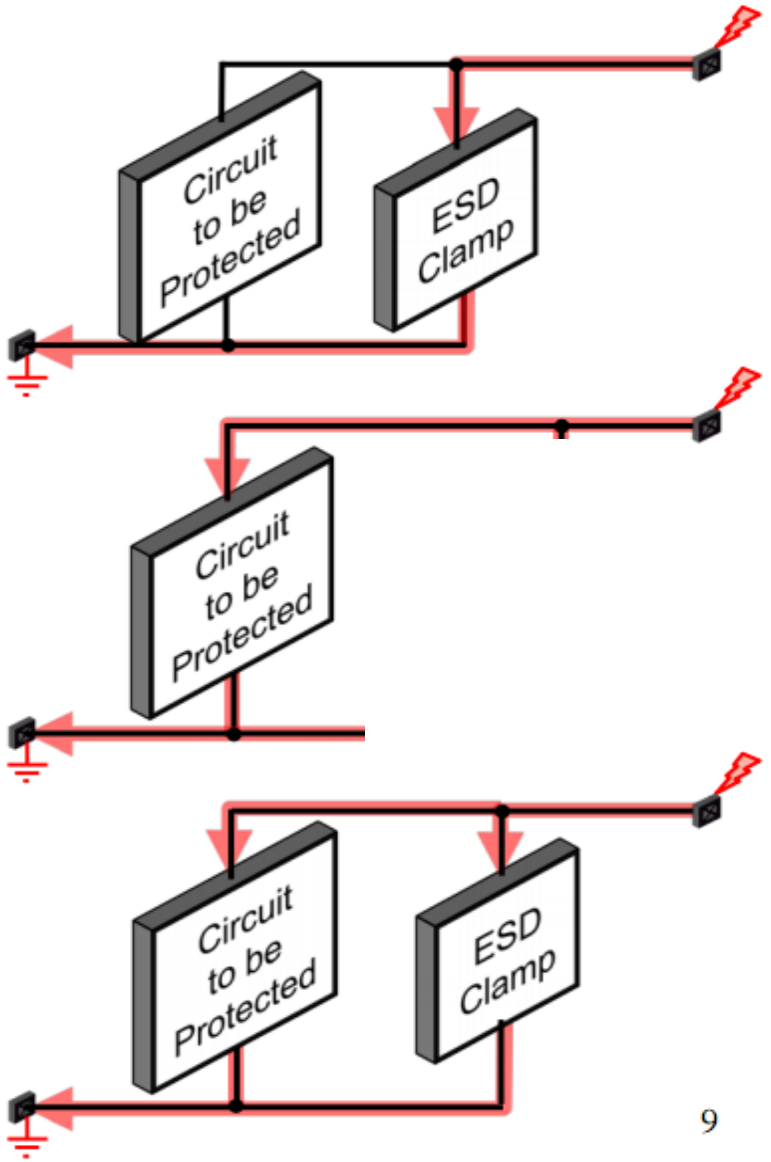
$$V_{ESD\_CLAMPS\_PATH} \geq V_{FAILURE\_CIRCUIT}.$$

2. ESD energy is shunted through the protected circuit.

$$\begin{cases} I_{PROTECTED\_CIRCUIT} \geq I_{FAILURE\_CIRCUIT} \\ V_{PROTECTED\_CIRCUIT} \geq V_{FAILURE\_CIRCUIT} \end{cases}.$$

3. ESD energy is shared between the ESD clamp path and the protected circuitry.

$$\begin{cases} I_{PROTECTED\_CIRCUIT} \geq I_{FAILURE\_CIRCUIT} \\ V_{ESD\_CLAMPS\_PATH} \geq V_{FAILURE\_CIRCUIT} \end{cases}.$$



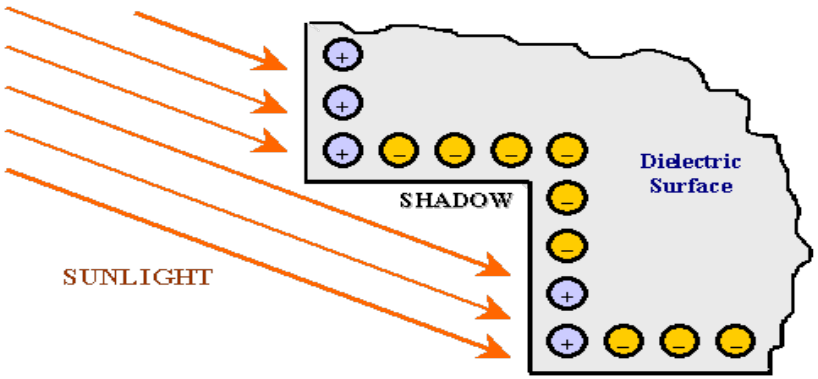
9

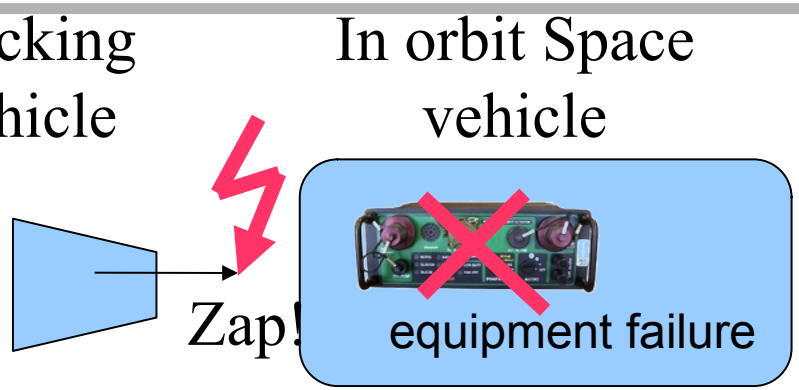
'Must Do' Activities of the ESD design manager

1. Design and Qualification of the used ESD design library cells and IP for company's specific silicon technologies – CMOS, Bipolar.. (not juts rely on Fab's generic solutions)
2. Design, Implement and Review dedicated ESD protection circuits for company's specific IC applications – ASIC, SoC, Analog, RF, Automotive,SPACE…, and for the target stress modes – *HBM, MM, CDM, IEC*
3. Implement Circuit level ESD simulation capabilities for the used standard design kits – to allow its IP designers to design and verify their custom ESD circuit functionality before tapeout
4. Implement automated ESD Design verification tools and flow – ensure the full chip ESD design rule compliance and robustness
5. Provide in-house of an ESD Transmission Line Pulse (TLP) test system to allow fast ESD performance check and design troubleshooting when needed
6. Train its team on ESD design, review and troubleshooting – dedicate 'ESD champions' in the team

Space environment effects

SPACECRAFT Charging – real issue



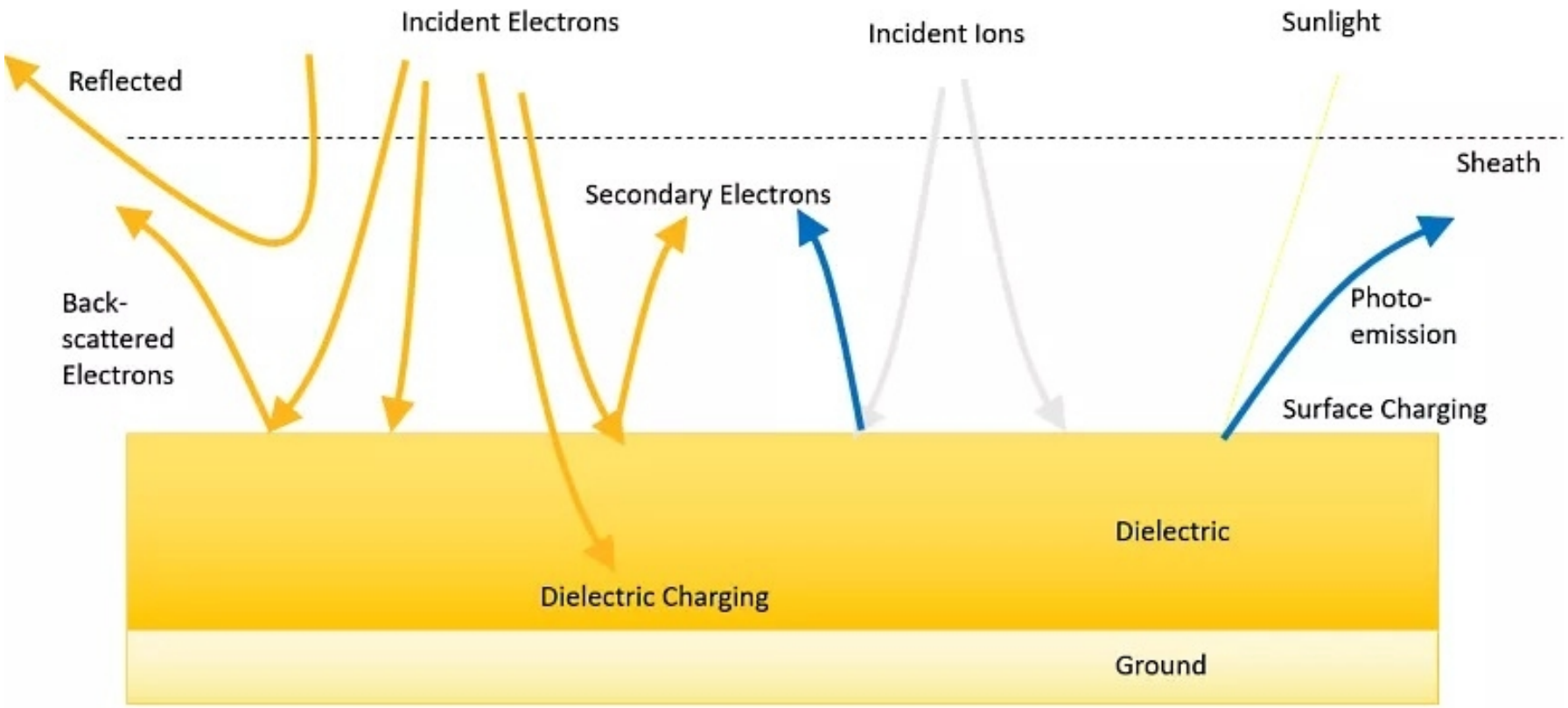


Due to self-shadowing, and other effects in space flight conditions and operations, differential spacecraft surface charging can occur thus creating potential differences (>600V), both outside and inside spacecraft.

Due to the spacecraft charging in space flight environment conditions, severe **Electrostatic Discharge (ESD)** events can happen during the different spacecarft operation regimes, leading to critical failures of the equipment in orbit

Studies on the spacecraft charging began after several occasions of anomalous behavior of satellites in the early 1970s, and especially after the loss of the US military satellite DSCS-9431 in 1973 [1]. A large program was jointly conducted by NASA and the U.S. Air Force to investigate the problem. The USAF P78-2 Spacecraft Charging At High Altitudes (SCATHA) satellite operating between March 1979 and June 1980 was specially designed to obtain environmental and engineering data to allow the creation of design criteria, materials, techniques, tests and analytical methods to control charging of spacecraft surfaces.

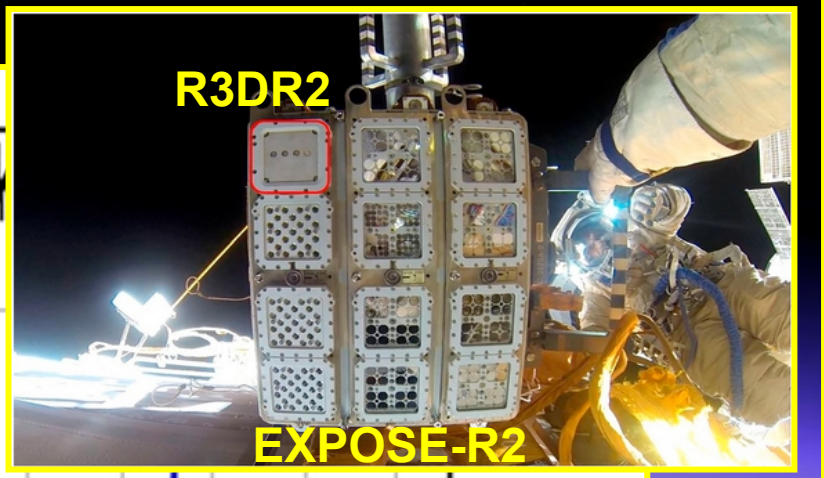
At present , there is a very limited systematic studies on the ESD events happening in space flight conditions and in developing common guidelines for improved reliability design of the spacecraft electronic components and systems



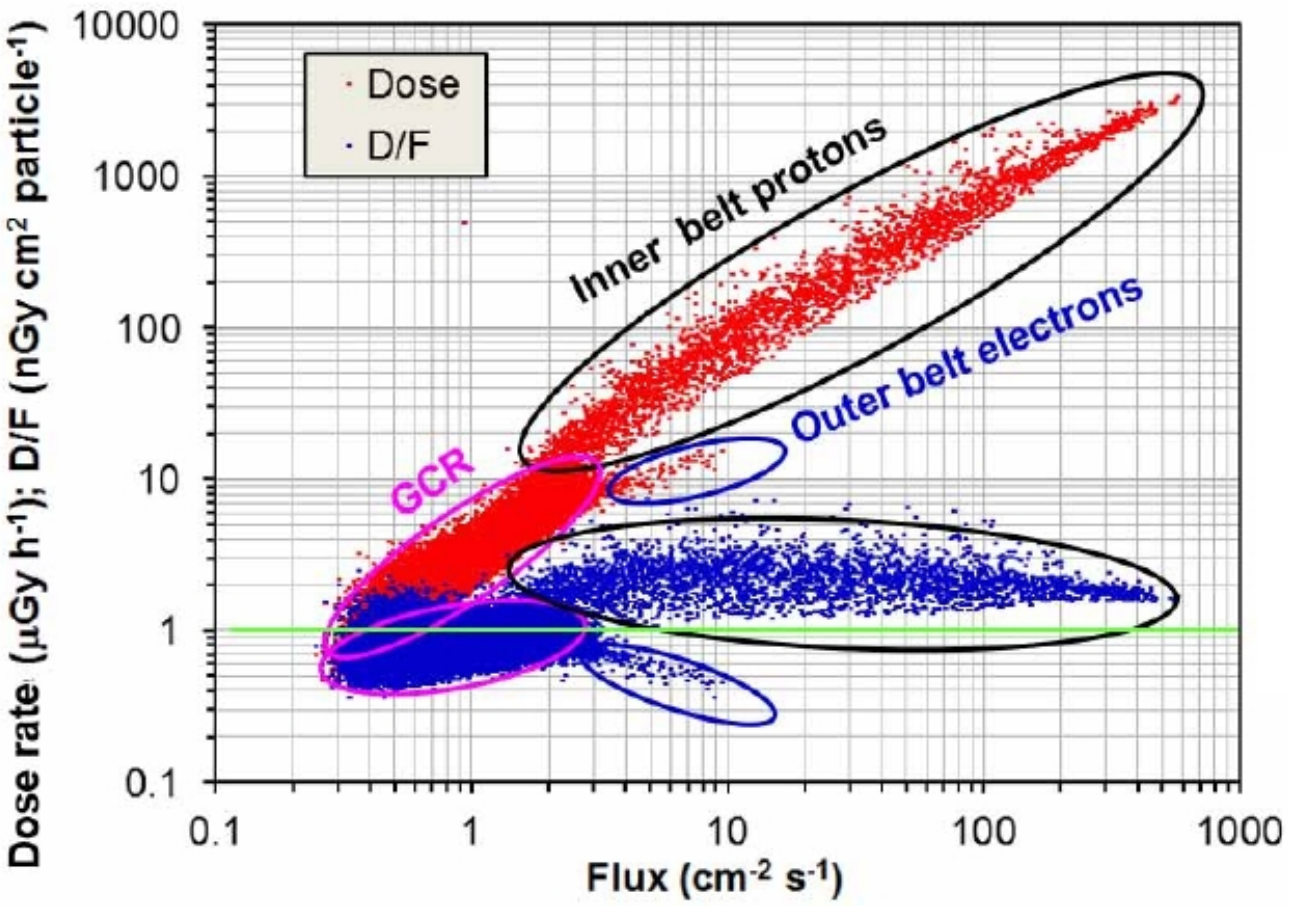
Conceptual diagram of physical processes involved in spacecraft charging

(source: https://fluidcodes.com/news/simulate-to-mitigate-electrostatic-discharge-on-spacecraft/.

Average daily dose rates - Data from ESA's EXPOSE-R2 platform aboard ISS, R3DR2 dosemeter, (SRTI-BAS, Bulgariq & Univesity of Erlangen, Germany)



Courtesy: prof. Dachev, SRTI-BAS



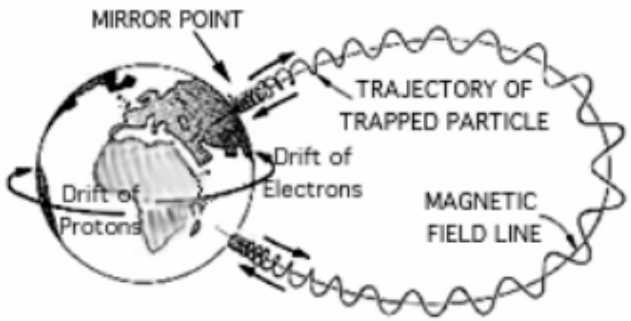


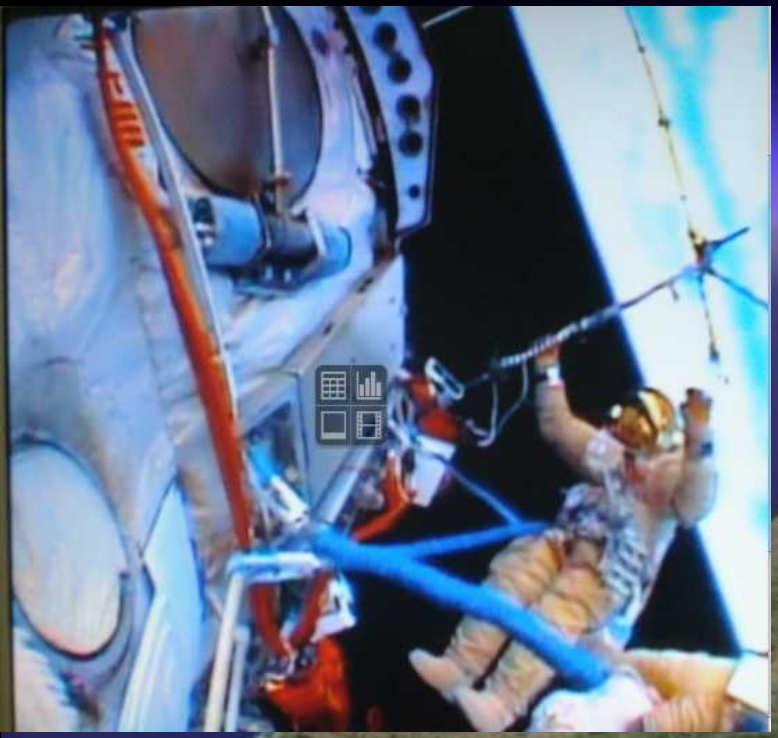
Figure 8. Trapped charged particle motions *(after Stern and Ness, 1981).*

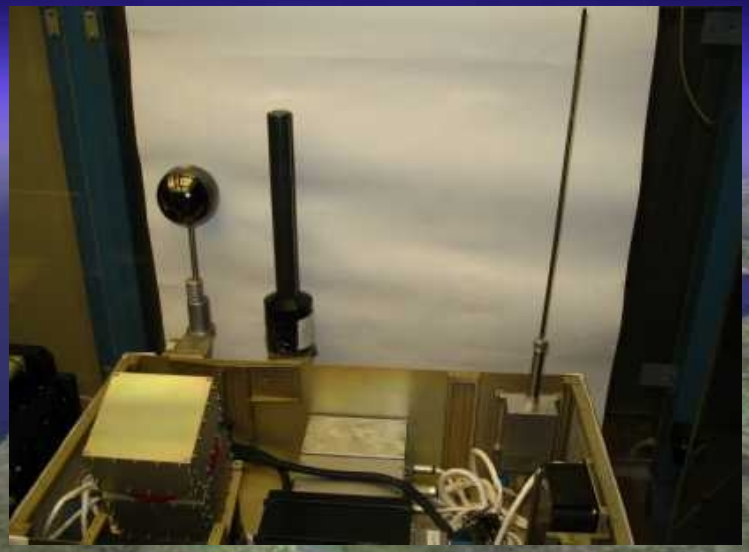
Actual Dose rates from the instrument showing the peculiarities of the space radiation sources.

Spacecraft Charging- ISS

BAS-RAS collaboration example: ISS plasma charging study – OBSTANOVKA Experiment

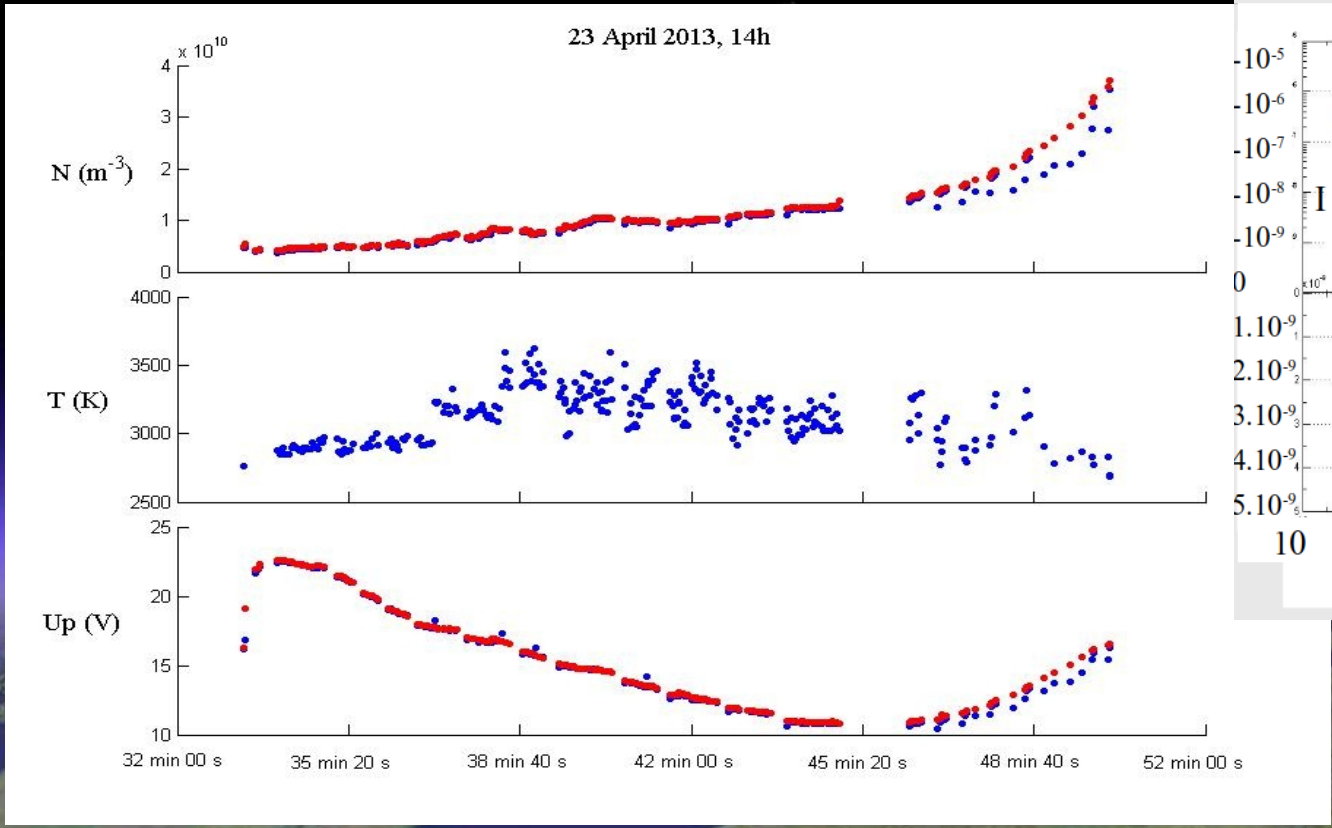
(Prof. Boyan Kirov, SRTI-BAS, bkirov@space.bas.bg

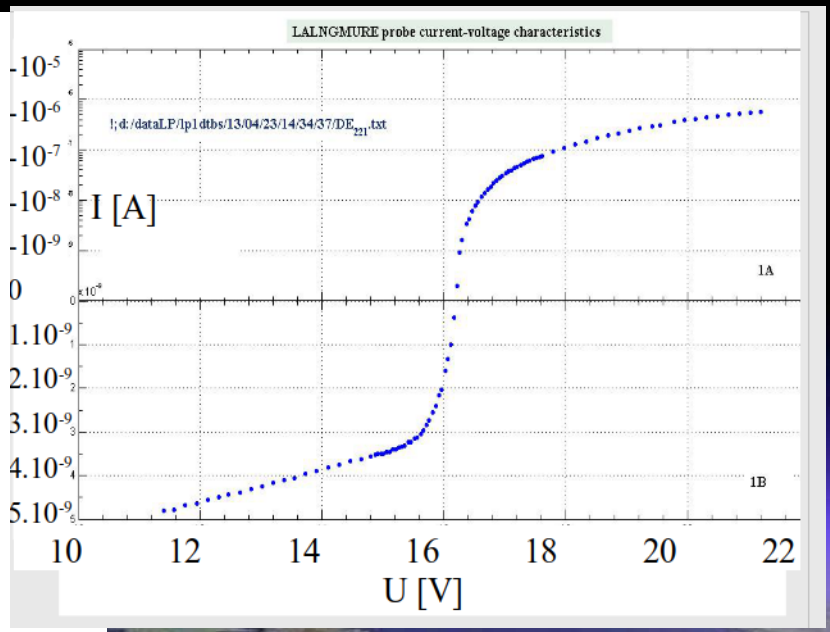




OBSTANOVKA payload and placement outside ISS

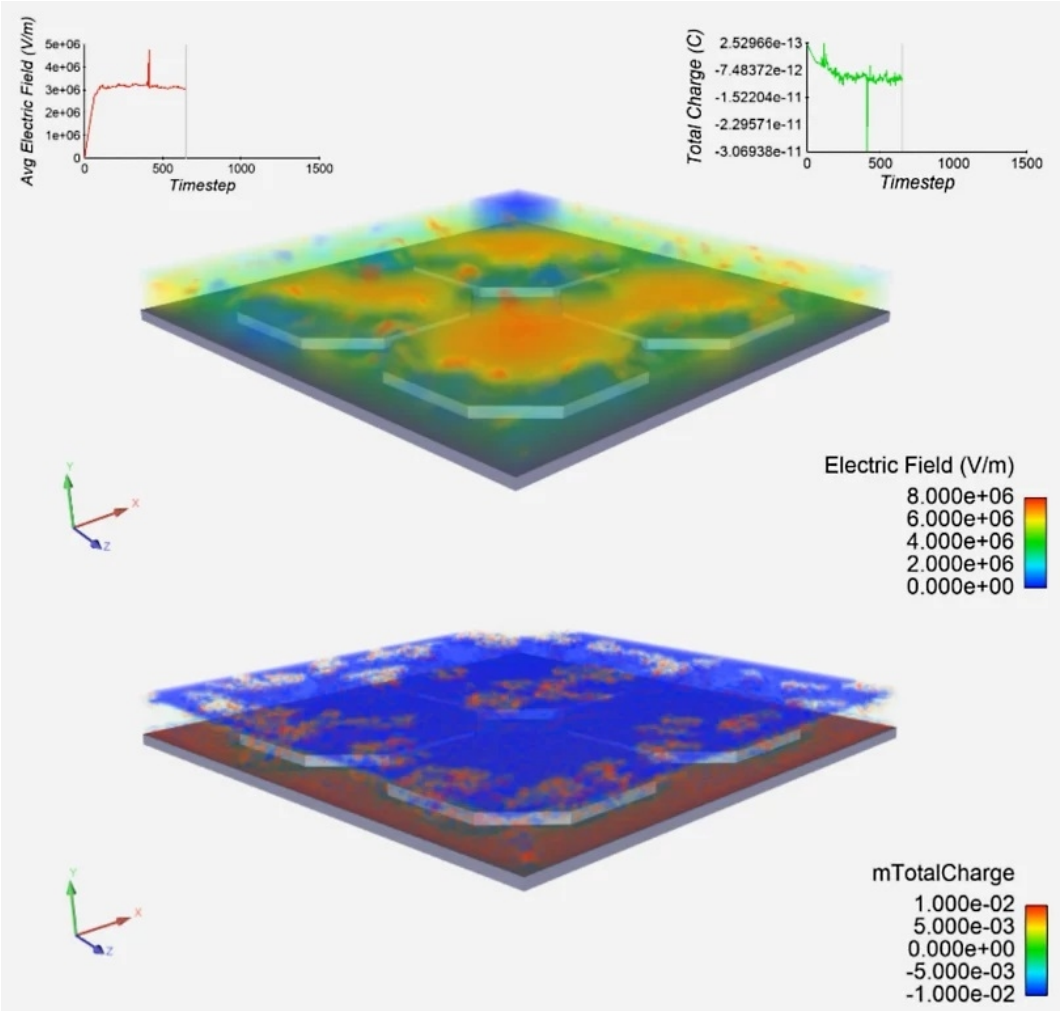
ISS Charging



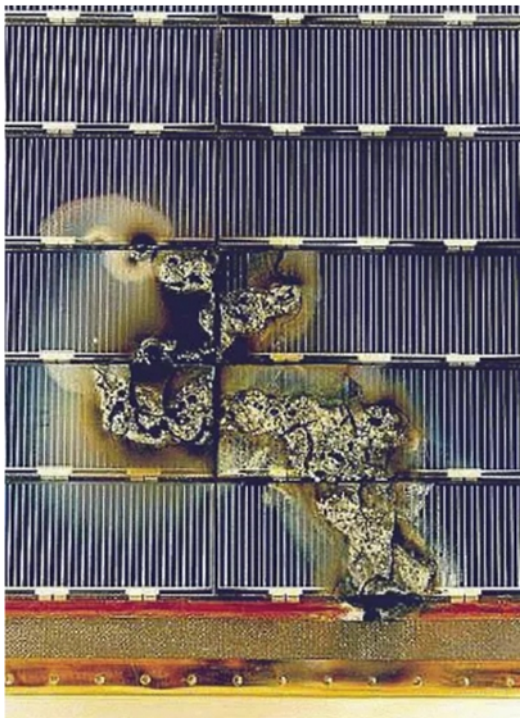


Experimental IV of the Langmuir probe providing data to characterise the plasma surrounding ISS

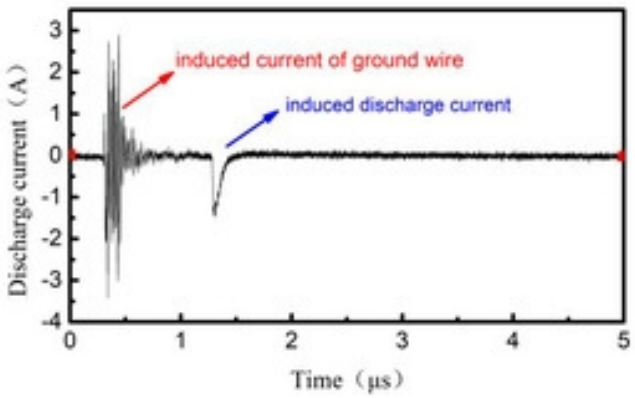
The evolution of the extracted plasma parameters in a typical 20 minutes measurement session. An interesting observation is that the ISS surface potential Up varies and never drops bellow 10V. This is not quite yet understood and needs further investigation



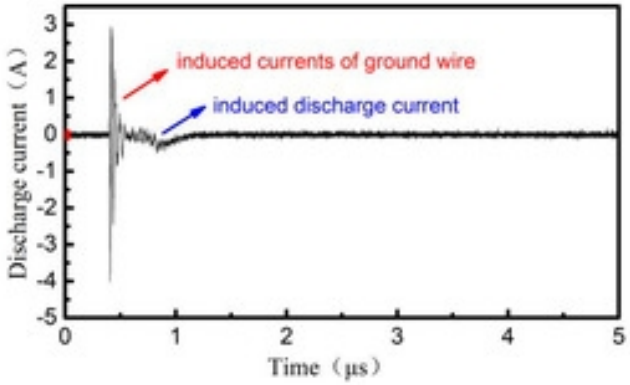
On the top, line plots of the average electric field and the total charge through time. In the middle, a 3D color map of the electric field after 700 timesteps. On the bottom, a 3D map of the charge density in the glass.



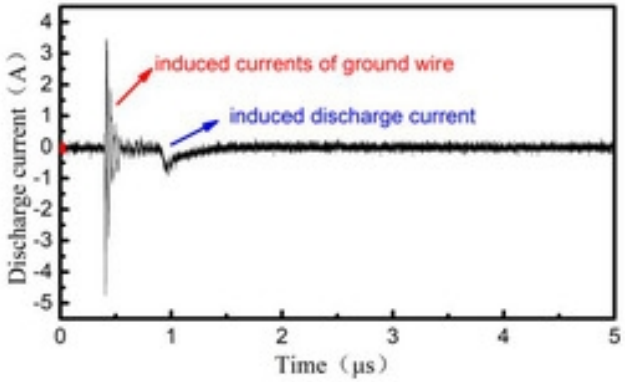
source: https://fluidcodes.com/news/simulate-to-mitigate-electrostatic-discharge-on-spacecraft/.



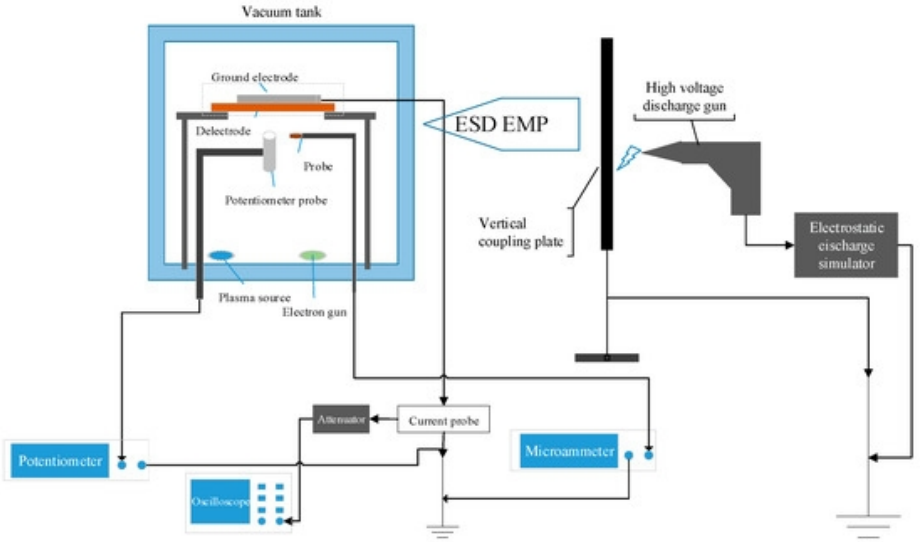
(a)



(b)



Under the radiation field with a peak field strength of 12.3 kV/m in ESD field pulse, the typical induced discharge waveforms of PTFE, PI and EP with 0.5 mm thickness are shown inÂ Figure 6, which in conditions that the charge electron beam energy is 30 keV and the beam density is 17 nA/cm2Â



Source:Research on the Induced Electrostatic Discharge of Spacecraft Typical Dielectric Materials under the ESD Pulse Irradiation, https://www.mdpi.com/1996-1944/15/6/2115/htm,

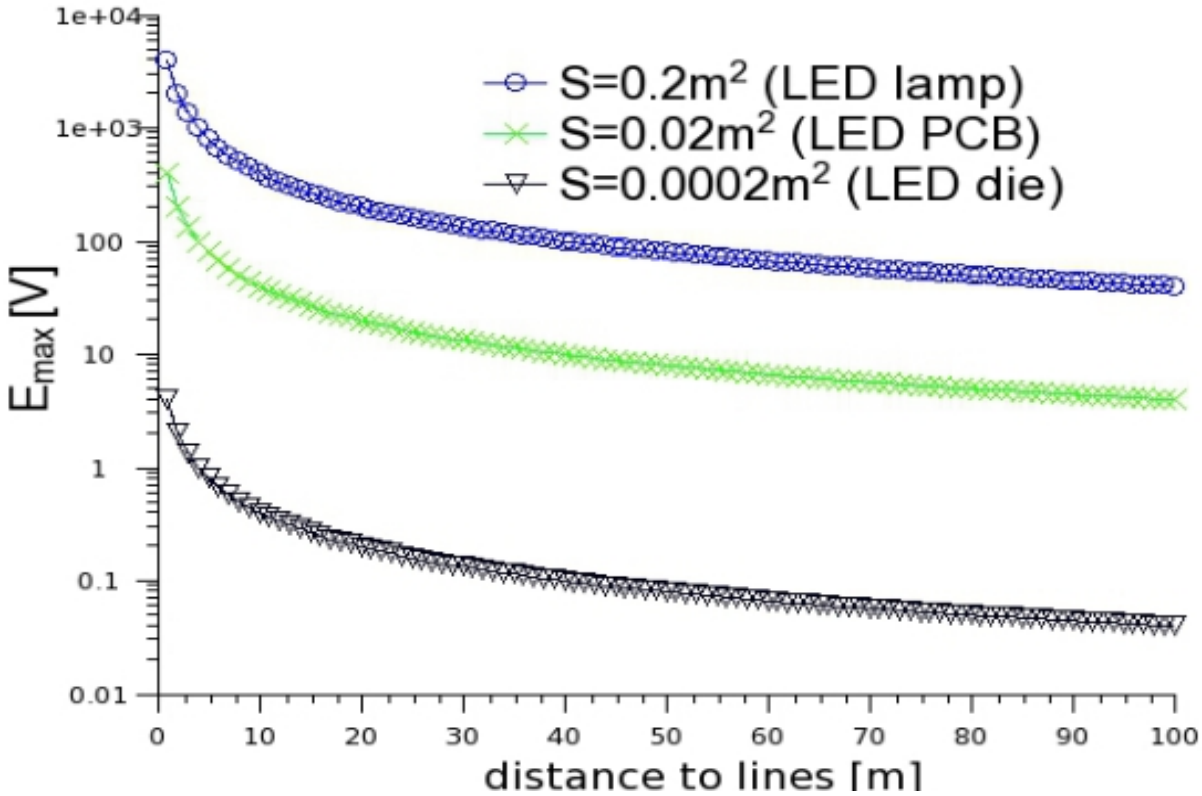
Xiaofeng Hu et all. 2022

ESD events in aerospace- Private discussion with experts..

Historically, EMC/EMI robustness is primarily considered for the on-board service electronics (avionics) in the aero-space industry. The reason is the typical for the aircraft architectures long wiring (total wire length typically of several km), susceptible to picking up EM noise from the environment and transforming the generated impulses to the avionics components leading to disturbing their operation or a failure. The 'typical' ESD-like event related to aerospace (from system point of view) should be considered originating from such field induced transients. The most commonly referenced IEEE surge standards used in practice are known as the Trilogy: *IEEE C62.41.1 – 2002(IEEE Guide on the Surge Environment in Low-Voltage (1000 V and Less) AC Power Circuits),* IEEE C62.41.2 – 2002 *(IEEE Recommended Practice on Characterization of Surges inLow-Voltage (1000 V and Less) AC Power Circuits*), and IEEE C62.45 – 2002 (*IEEE Recommended Practice on Surge Testing for Equipment Connected to Low-Voltage (1000 V and Less) AC Power Circuits*). IEC 61000-4-2 is still used at board level, however there seems to be a gap in characterizing the impact of the actual in-flight, in orbit conditions (humidity, temperature, pressure, etc) which affect the proprieties of the actually generated surge waveforms, compared to those on ground level. It seems there is no currently a standard test method (need to confirm) for equipment/systems level susceptibility to ESD-like events in flight conditions.
Other standards in use for EMI robustness at component level are:MIL-STD-461 (military), RTCA DO-160, EUROCAE ED-14 (Commercial). At aircraft level - US Military MIL-STD-464, and, again RTCA DO-160, EUROCAE ED-14

Performance /robustness targets : Having in mind that the most-common origin of ESD-like events in the airspace applications are the field-induced transients (similar in physics to the CDM events), at present it is typically targeted achieving robustness to transients generated at EM field strengths of 200 V/m. This value is primarily defined from the stand-point of safety requirements providing robustness margin. It is obviously required to re-evaluate such a target spec based on a detailed study and data for the actual field strength thresholds leading to avionic failures
On the other hand, according the ITRS Electrostatics roadmap, the state of the art semiconductor technology components have robustness boundaries much bellow the 200V/m level. This implies substantial challenge in designing the target performance of the avionics systems.

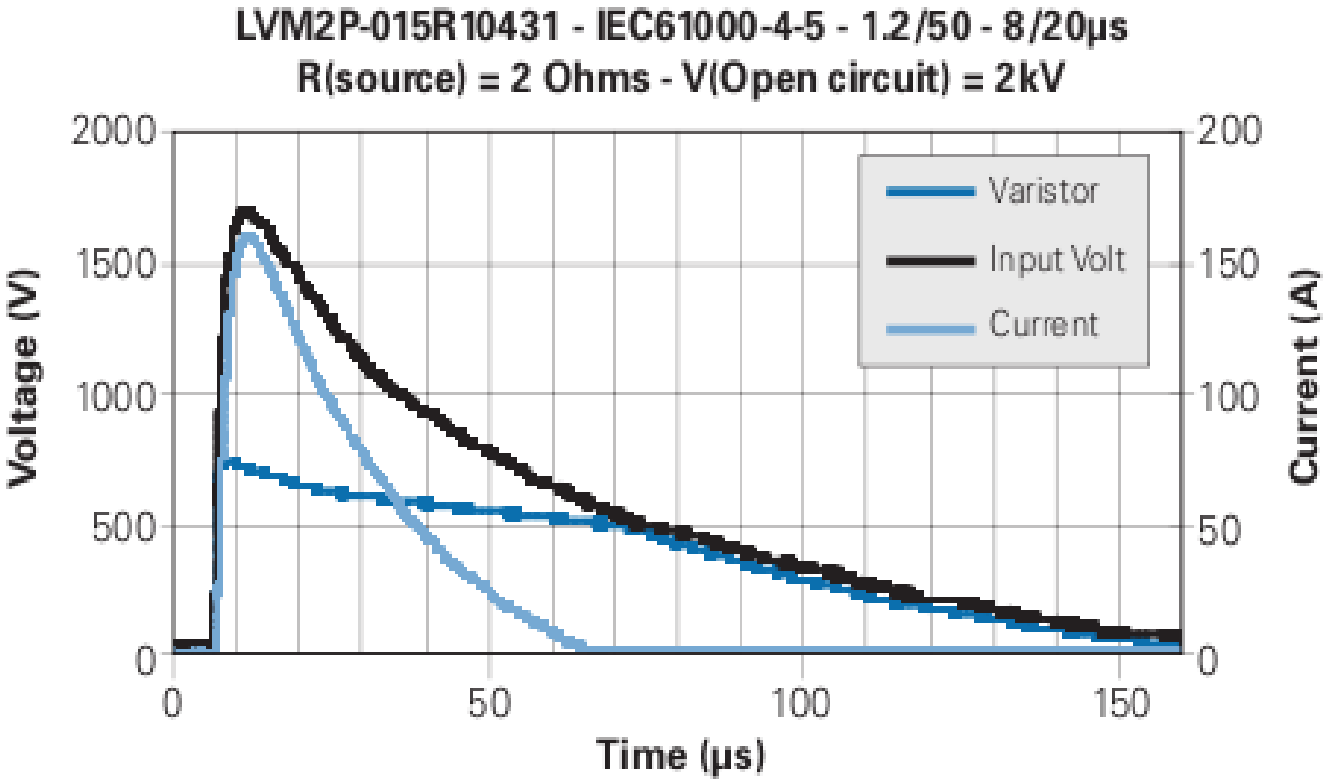
Some Simple Math



$$E_{ind}^{MAX} = \mu_0 S \frac{A_i^{MAX}}{(2\pi \cdot r_K)}$$

The Induced voltages inside an electronic system could reach severe amplitudes. Combined with the huge current injection ~ 1MA/µs on the external power or communication lines, leads to high requirement on the protection strategies

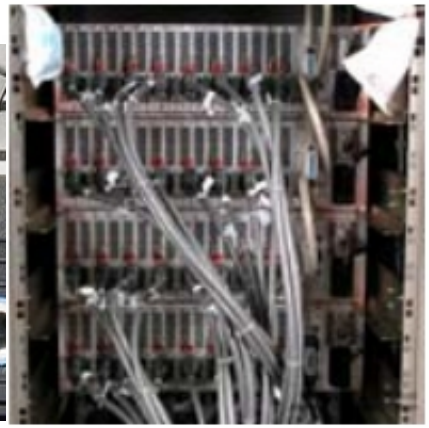
SYSTEM PROTECTION APPROACHES



Typical clamping characteristic of a commercial discrete clamp for PCB level application

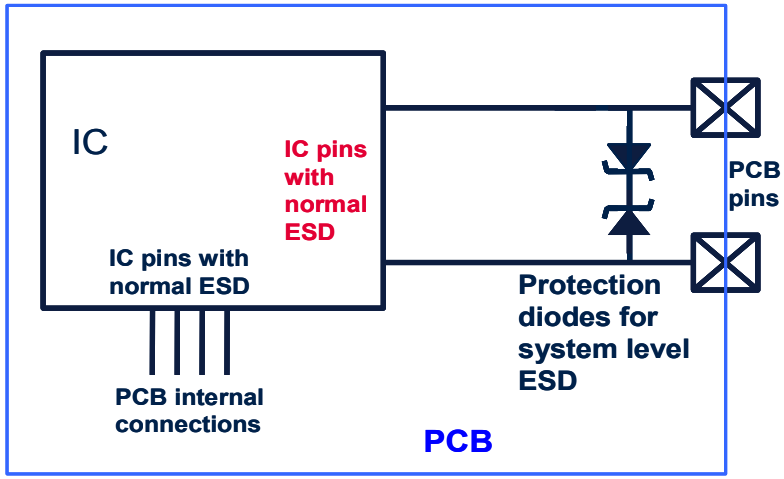
❖ Need to understand final product

- Will people handle the electronics (e.g. I-Pod)?
- Is the electronic system connected to cabling (e.g. a laptop to an ethernet cable)?
- Does the system operate in a controlled environment (e.g.
- server farm) or in an uncontrolled environment (e.g.
- automobile)?
- Does the system operate in an environment with electrical
- transients/crosstalk (e.g. the burn-in test floor)

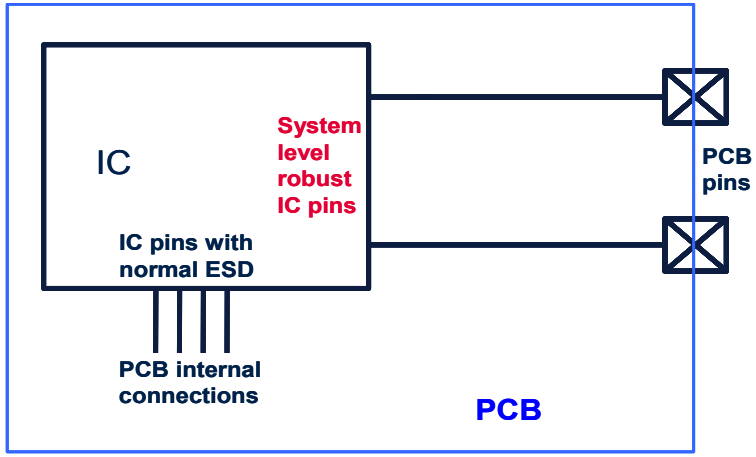


Courtesy Semitracks Inc

IEC Protection Approaches



Common strategy with PCB protection

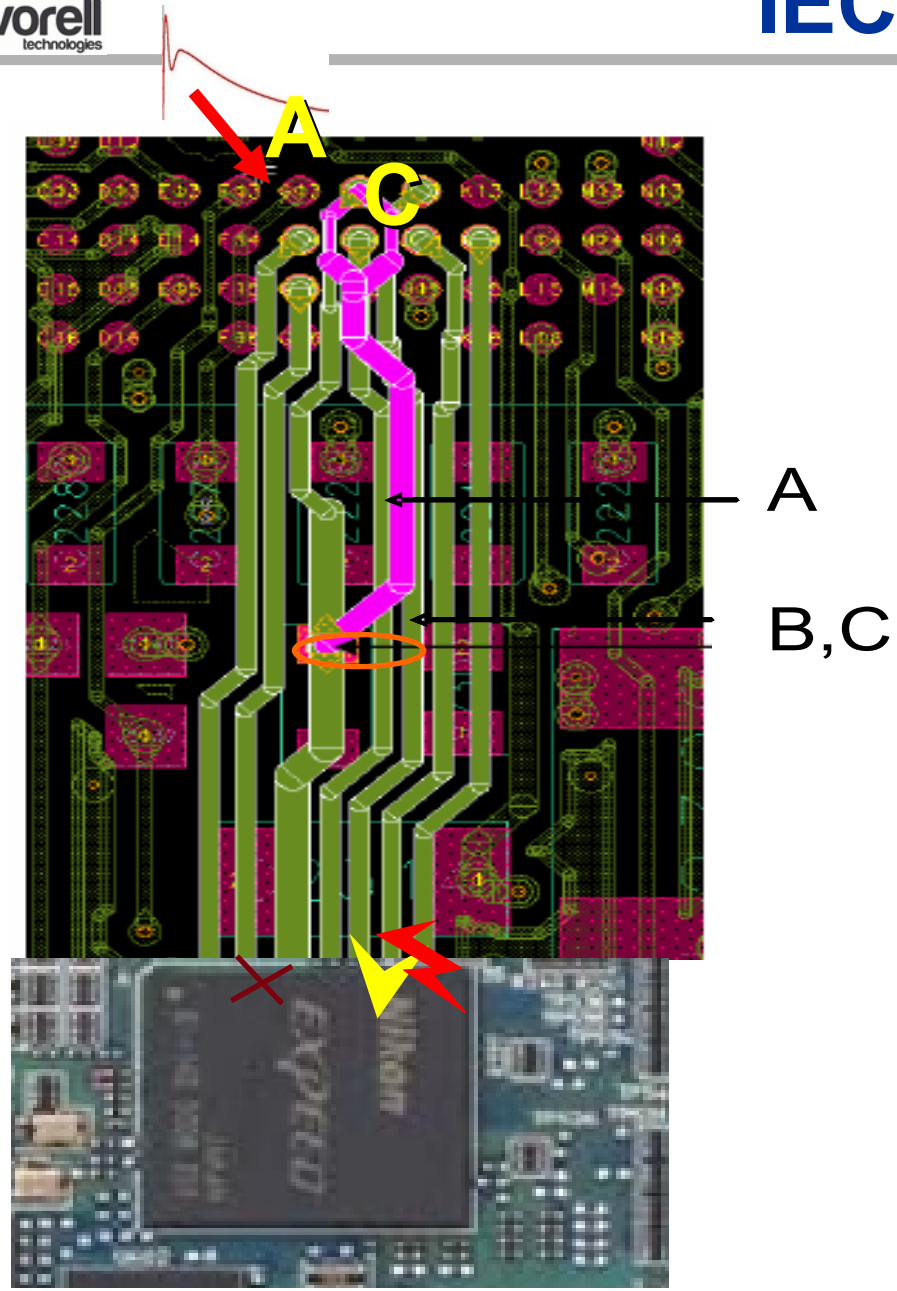


Inherently robust IC pins
(on-chip protection far beyond 2 kV HBM)

On-chip IEC protection is not ideal; increases pad capacitance and degrades high speed performance

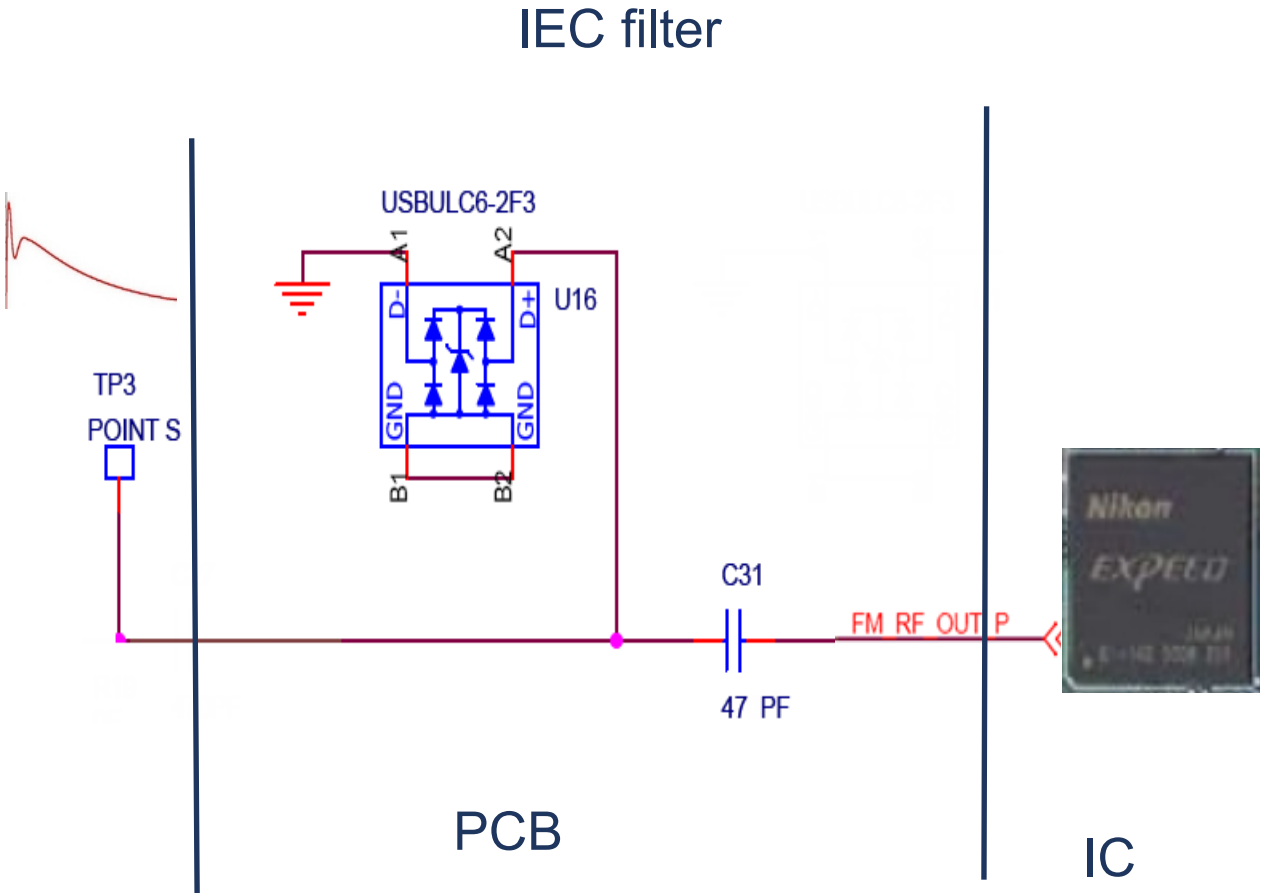
Duvvury at EOS/ESD

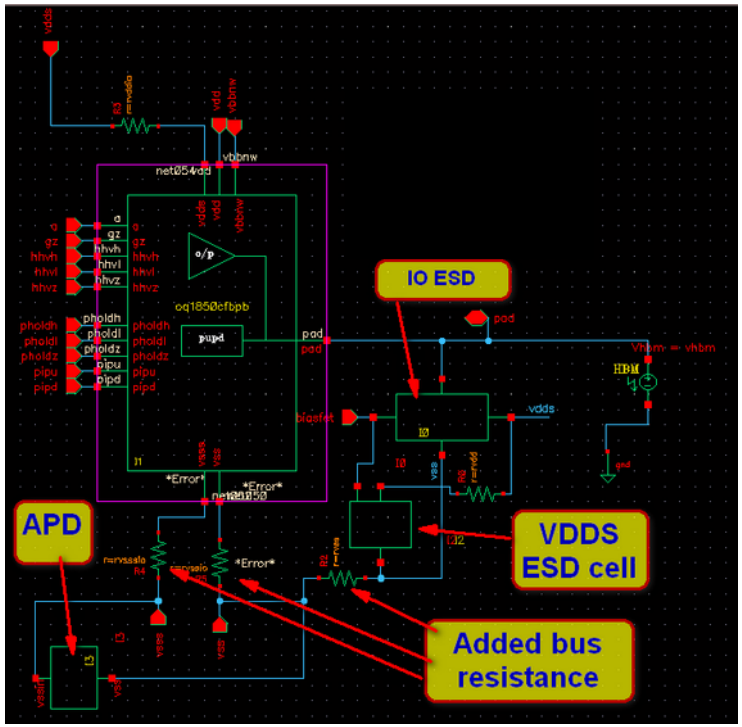
IEC Protection peculiarities



Example of a package trace design in which the ball connected to trace A needs to sustain on chip IEC stress event. Due to the parallel trace design, electromagnetic_coupling can easily happen to balls connected to e.g. traces B, C and cause failure to the inner circuits connected to the corresponding bond pads

IEC Protection design = IC + PCB co-design!





ESD REQUIREMENTS (U.S.A.)

1. **MIL-STD-HBM**
   - +/- 2 KV Required by most customers
   - Waivers given at 1 KV in some cases
   - 4 or 8 kV On Special Automotive Pins (Power Outputs)

2. **MACHINE MODEL**
   - Some customers require 200 V
   - Waivers given to 100 V in some cases
   - Is this model really needed?

3. **CHARGED DEVICE MODEL**
   - No clear standard
   - +/- 1000 V Some customers who require this
   - +/- 500 V level was generally found to be reliable

ESD REQUIREMENTS (U.S.A.) (continued)

4. SPECIAL TRANSIENT TESTING

Required By Auto Manufacturers With Many Different Transient Pulses

'Load Dump' Test - High Energy Pulse of 100 V Magnitude and 10-100 MS Long

'Chatter Test' - Toggle Output While Exercising The Part EMI Testing

5. IEC SYSTEM LEVEL TEST

Important for chip pins exposed to outside world (examples in cell phones and computer interface connections)

8 kV Contact Discharge Level required by most customers

ESD Standards

Standard: A precise statement of a set of requirements to be satisfied by a material, product, system or process that also specifies the procedures for determining whether each of the requirements is satisfied.

Standard Test Method: A definitive procedure for the identification, measurement and evaluation of one or more qualities, characteristics or properties of a material, product, system or process that yields a reproducible test result.

Standard Practice: A procedure for performing one or more operations or functions that may or may not yield a test result. Note: If a test result is obtained, it may not be reproducible between labs.

Technical Report: A collection of technical data or test results published as an informational reference on a specific material, product, system, or process

http://www.esda.org/standards.html

http://www.ce-mag.com/ARG/ESD_Standards.html

ESD Standards : Who defines them?

- ESD Association
- EIA/JEDEC
- U.S. Military/Department of Defense
- International/European

Sources of Standards

- ESD Association, 7900 Turin Road, Building 3, Suite 2, Rome, NY 13440. Phone: 315-339-6937. Fax: +1 315-339-6793. Web Site: http://www.esda.org/
- Electronic Industries Alliance/JEDEC, 2001 Pennsylvania Ave., NW, Washington, DC 20006. Phone: 202-457-4900. Fax: 202-457-4985. Web Site: http://www.eia.org/
- HIS Global Engineering Documents, 15 Inverness Way East, Englewood, CO 80112. Phone: 800-854-7179. Fax: 303-397-2740. Web Site: http://global.ihs.com/
- International Electrotechnical Commission, 3, rue de Varembe, Case postale 131, 1211 Geneva 20, Switzerland. Fax: 41-22-919-0300. Web Site: http://www.iec.ch/
- Military Standards, Naval Publications and Forms Center, 5801 Tabor Avenue, Philadelphia, PA 19120.

U.S. Military/Department of Defense ESD standards

MIL-STD-1686C : Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)

This military standard establishes requirements for ESD Control Programs. It applies to U.S. military agencies, contractors, subcontractors, suppliers and vendors. It requires the establishment, implementation and documentation of ESD control programs for static sensitive devices, but does NOT mandate or preclude the use of any specific ESD control materials, products, or procedures. ***It is being updated and converted to a commercial standard by the ESD Association.***

MIL-HBDK-263B: Electrostatic Discharge Control Handbook for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)

This document provides guidance, but NOT mandatory requirements, for the establishment and implementation of an electrostatic discharge control program in accordance with the requirements of MIL-STD-1686.

MIL-PRF 87893—Workstation, Electrostatic Discharge (ESD) Control

This document defines the requirements for ESD protective workstations.

MIL-B-81705—Barrier Materials, Flexible, Electrostatic Protective, Heat Sealable

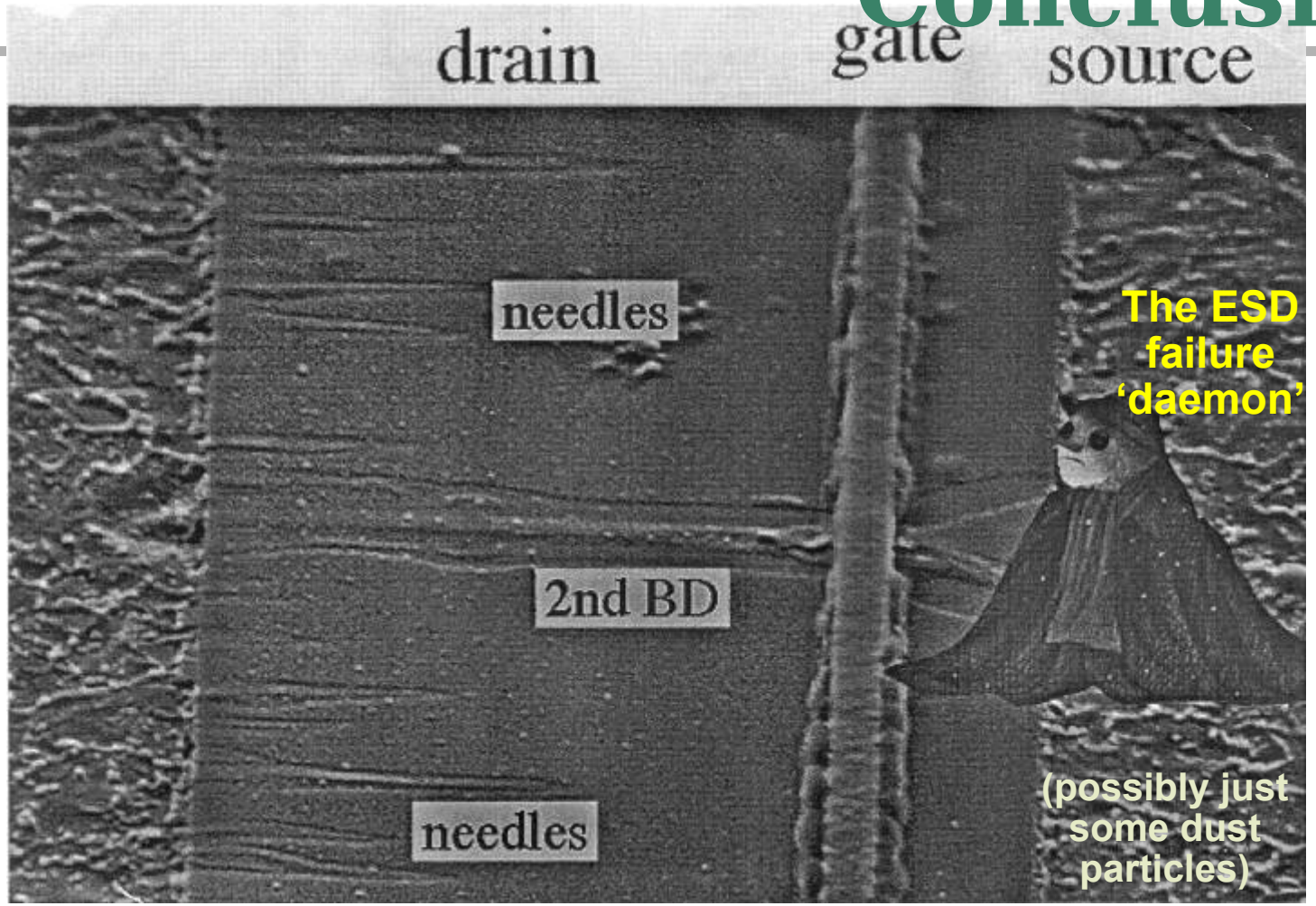
This documents defines requirements for ESD protective flexible packaging materials.

MIL-STD-129—Marking for Shipment and Storage

Covers procedures for marketing and labeling ESD sensitive items

Conclusions

REAL Image from Physical Failure Analysis of ESD induced MOSFET degradation



The modern ESD design approaches help to avoid using any 'Black Magic' techniques in defining the ESD reliability solutions for the nowadays ICs