Flight Computer Initialisation Sequence Generic Specification

(Overview of the modifications)

Version number: issue 2, revision 1
Objective

To update the Flight Computer Initialisation Sequence Generic Specification to cover multicore architectures.

**SAVOIR.BOOTSW.BIN.242**

**Initialisation by a Single Core**

In case of multi-core processors, only one core must be responsible for the initialisation sequence.

- **Option Info:** OBC; PLM
- **Requirement Rationale:** Ensuring a deterministic and easy to test behaviour. In case other cores would be active and executing SW or interacting with HW in other way, it could be difficult to demonstrate this deterministic behaviour.
- **Verification Method:** T

**SAVOIR.BOOTSW.BIN.245**

**Secondary core(s) states**

In case of multi-core processors, secondary core(s) shall be disabled (i.e. powered-down) all time during the boot software execution.

- **Option Info:** OBC; PLM
- **Requirement Rationale:** Only one core must be responsible for the initialisation sequence.
- **Note:** initialisation of the secondary core(s) is performed by the ASW after it is started on the primary core. This requirement is applicable only if such feature is available in the Chip.
- **Verification Method:** T
Work Logic

1. Collecting RIDs
2. One to one meetings with domain experts
3. Updating the specification

Iterations to reach out all stakeholders

1. Internal to TEC-SWF
2. Extended to other TEC sections:
   - TEC-EDD
   - TEC-SWT
   - TEC-QQS
   - SAG
Changes triggered by reviewers

- **FPGAs** in the *initialisation* chain (observations)
- **Autonomous** hosted payloads (observations)
- To standardize *document styles*
- To include *interface requirements* (PUS-C services)
- To improve descriptions of **BITE and self-test**
- Inconsistencies, definitions, …

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<th>Category</th>
<th>Total</th>
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<td>SECONDARY COREs</td>
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<td>GENERAL (figures, inconsistencies, definitions)</td>
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<td>10</td>
<td>5</td>
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<td>I/F Reqs (PUS)</td>
<td>8</td>
<td>7</td>
<td>1</td>
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<td>0</td>
<td>1</td>
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emerging HW assumption:
FPGAs in the initialisation chain

When FPGAs are used to initialise the OBC (e.g. it includes the management of interfaces), they are expected to be configured either:
- prior the initialisation of the main processing core (e.g. by loading predefined configuration).
- Otherwise, by the ASW.
Standardizing document styles

Each requirement section has its own style
(this somehow simplifies the import procedure of the spec. to IBM Doors)
emerging HW assumption:
Autonomous hosted payloads

observation: hosted payloads might be independent from OBC to exchange TCs with Ground. In this case, the Standby scenario of the Payload Computer is treated similarly to the one of the OBC.
General observations

1. missing definitions of <Parameter> and <Hardware Assumption>
2. inconsistent requirement's rewording
3. detailing Fast Boot initialisation sequence

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Fast Boot Path sequence

When Fast Boot Path is selected, the Boot SW Fast Sequence shall execute a subset of the step of the nominal sequence.

Note: The selected subset of nominal sequence’s step is defined following mission constraints.
Proposed PUS-C subservices

Service ST[01] - Request verification
- acceptance and reporting subservice
- execution reporting subservice

Service ST[03] - Housekeeping
- housekeeping reporting subservice

Service ST[05] - Event reporting
- event reporting subservice

Service ST[06] - Memory management
- raw data memory management
- check raw memory data

Service ST[17] - Test
- test subservice

Service ST[20] - Parameter management
- parameter management subservice
- set parameter values
PUS-C ST[17] Test subservice

Source ECSS-E-ST-70-41C Annex C

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<tr>
<th>system</th>
<th>interface</th>
<th>message type</th>
<th>comment</th>
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<td>8.17.2.1</td>
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<td>8.17.2.2</td>
<td>TM[17,2]</td>
<td>are-you-alive connection test report</td>
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Conclusions

Discussed the main changes of the:

SAVOIR Flight Computer Initialisation Sequence Generic Specification

addressing multi-core and emerging hardware architectures

Several comments received and addressed (i.e. to formalise the PUS-C subservices expected by a Boot SW).

For existing Boot SW based on PUS-A, it is advisable to report on any deviation to PUS-C requirements.
Thank you for listening!
Questions?