european space technology harmonisation

On-Board Computer, Data Handling Systems and Microelectronics Dossier

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Agenda

Technical Perimeter of the OBCDHSM Dossier

Overview of the main technology objectives (AIMS)

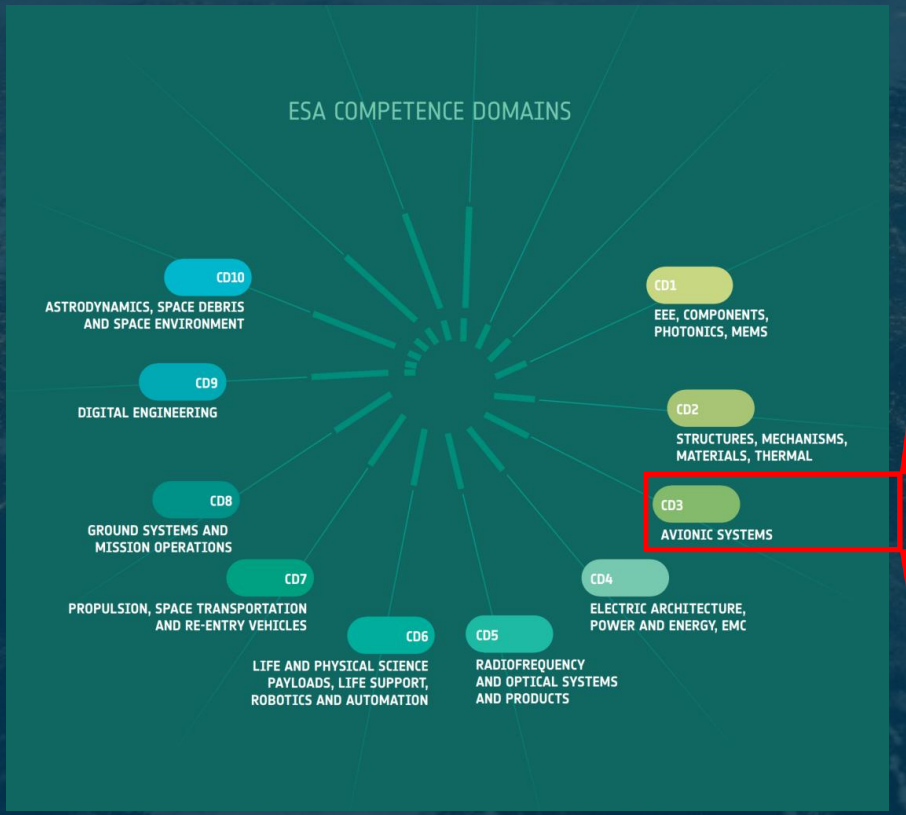
AIMS introduction

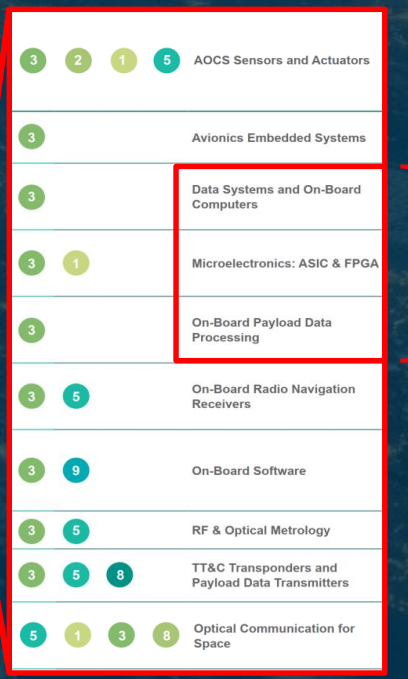
Global Budgets Overview

Conclusions

Questions/Answers Session

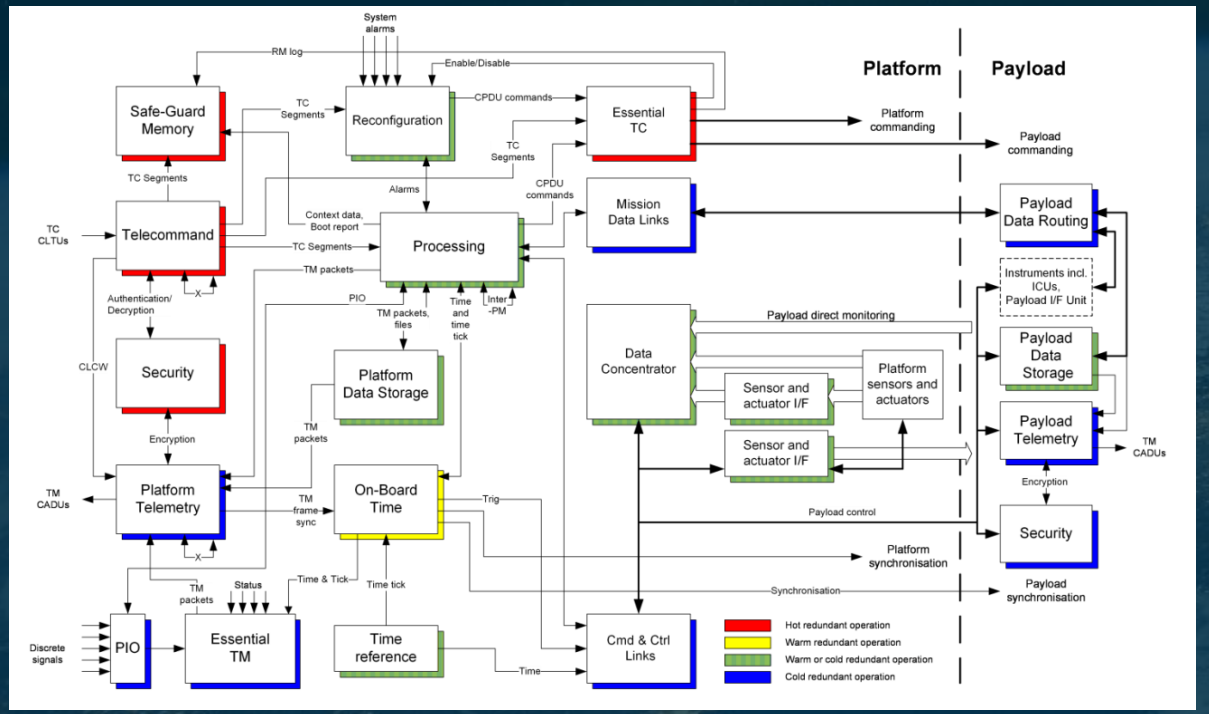
Technical Perimeter of the OBCDHSM Dossier



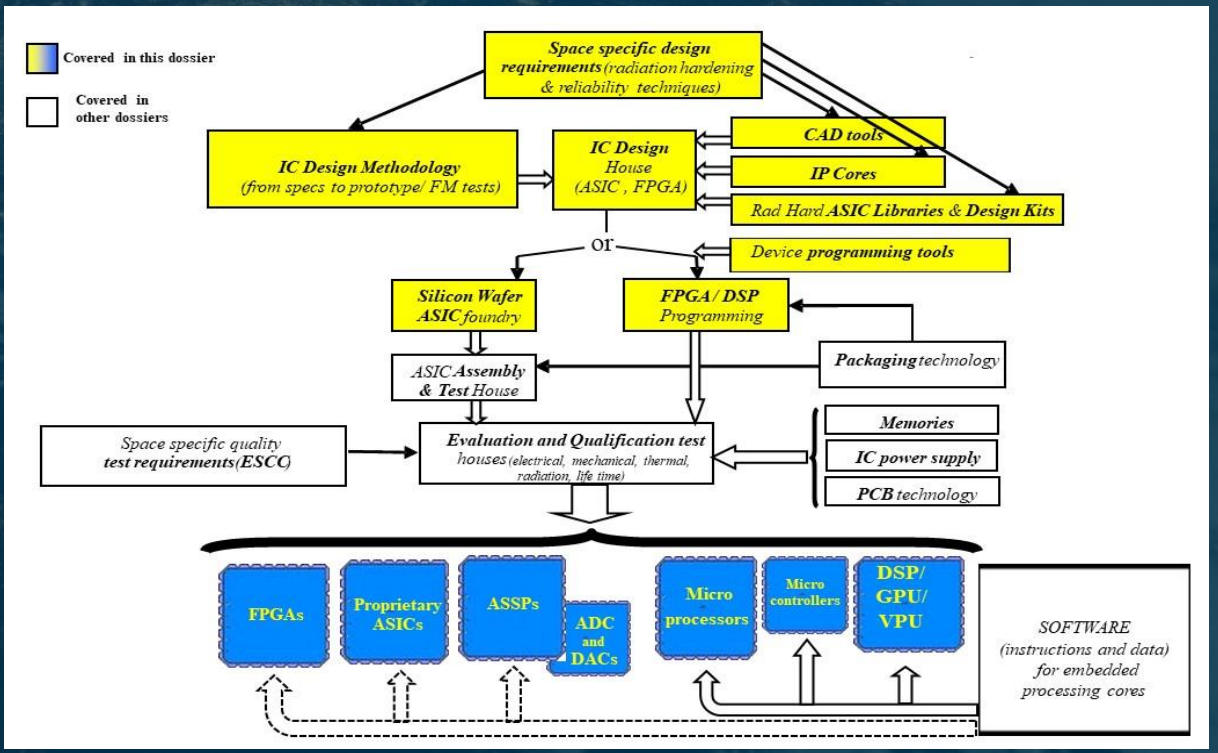


Merging in one document:
On-Board Computer, Data Handling Systems & Microelectronics (OBCDHSM) Dossier

Technical Perimeter of the OBCDHSM Dossier



SAVOIR
space avionics open interface architecture



Technical Perimeter of the OBCDHSM Dossier

Technology Family 1: CDHS Architecture, units, modules and communication systems

- Platform and Payload CDHS Architectures Background
- CDHS Units, Modules and functions (Platform and Payload)
- CDHS communication links, buses and networks

Technology Family 2: Microelectronic devices and enabling technology

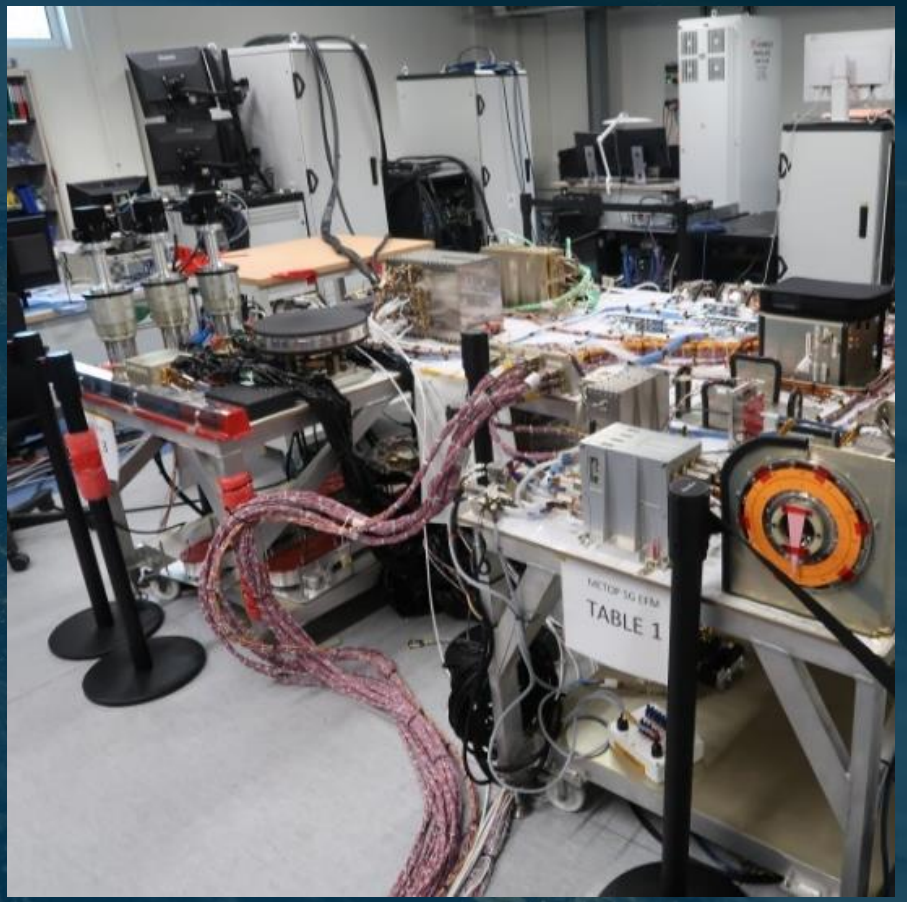
- FPGA
- Microprocessors, microcontrollers, DSP
- Application Specific Standard Products (digital, analogue and mixed-signal)
- ASIC platforms (rad hard cell libraries, IP, Design Kits, packaging, supply chain space quality)
- IP Cores

Technology Family 3: CDHS EGSEs & Microelectronics Development methods and tools

- EGSE and tools for CDHS used at satellite level or instrument level
- EGSE for CDHS Units
- EGSE that are used to verify the proper functionality of a module to be then integrated in a CDHS unit.
- Microelectronics development methods and tools

AIMS overview: Top Down Approach

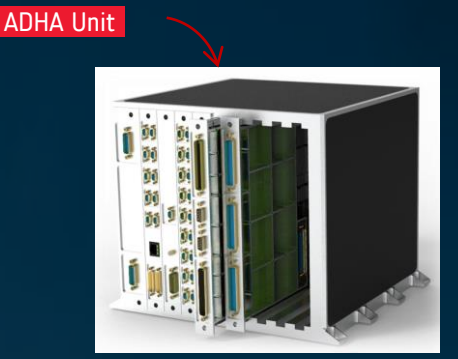
1. AIM A Define and adopt unified OBCDH architectures based on modules
2. AIM B Design, develop, manufacture and qualify buses, network and communication technologies
3. AIM C Design, develop, manufacture and qualify OBCDH modules (including AI, ML and COTS with adequate radiation mitigation techniques)
4. AIM D Develop Building Blocks to support OBCDH module(s) development(s)
5. AIM E Develop EGSE to support the test and integration of OBCDH units/modules and benefit of synergies and commonalities
6. AIM F Enhance characteristics/functions of current ASIC Platforms and develop USDM ASIC Platforms
7. AIM G Improve and expand the European rad-hard FPGA family
8. AIM H Improve and expand the European rad-hard Microprocessors, Microcontrollers and DSPs
9. AIM I Improve and expand the European rad-hard ASSP family
10. AIM J Improve and expand the European IP Cores catalogue and respective Design Methods and Tools



AIM A: Define and adopt unified OBCDH architectures based on modules

Objective:

Provide modular and standardized HW architectures for AVIONICS and PAYLOAD data handling in order to improve interoperability, flexibility, scalability, competitiveness and ease the procurement.



Key Future Activities

- Advanced Data Handling Architecture. Incremental building approach with:
  - Architecture consolidation and documentation preparation (2022)
  - First EM unit (2023) and then EQM unit (2025)
- OBCDHS architectures study for high reliability (2FT) missions types.
- Study of OBCDHS architectures based on microcontrollers (decentralized DHS Architectures)

2 running activities,
2 M€

5 proposed activities,
16.75 M€

AIM B: Design, develop, manufacture and qualify buses, network and communication technologies

Objective:

- To endorse the usage of standardized protocols (CAN-Bus, MIL-Bus, SpaceWire, SpaceFibre, TTEthernet).
- To develop new qualified network components (end points, routers etc.) to ease integration, reduce development time and costs, and increase performance.
- To promote best practices for verification and validation (e.g. network simulation, physical testing).
- To continuously improve communication buses (incl. protocols) for better usability, reliability, and performance.

Key Future Activities:

- SpaceWire: Deterministic communication (new routing switch), network management, network simulators
- SpaceFibre: Interface chip, routing switch chip, physical layer testing, reference designs
- Ethernet: TTEthernet test bed, end point, and switch; TSN characterization and development
- CAN: Integrated design environment for CAN-based networks

12 running activities, 4.6 M€

14 proposed activities, 5.4 M€

AIM C: Design, develop, manufacture and qualify OBCDH modules

Objective:

Develop a portfolio of OBCDHS modules that:

- can be rapidly implemented in a standardized OBCDHS Architecture (AIM A)
- can increase On-Board Processing capability (Processing Modules (HW/SW) & tools).
- can support disruptive data analysis technologies (AI/ML) for supporting avionics and payload applications (incl. data compression and reduction).

Key Future Activities

- HW Processing Modules based on rad-hard Microelectronics (under development by primes with European processors and FPGAs)
- HW Processing Modules based on COTS
- Cubesat Modules
- ADHA Modules (EM)

ADHA Modules Products (ADHA-MP):
- ADHA On-Board Computer Module (AOBCM)
- ADHA Mass Memory Module (A3M)
- ADHA Computing Modules (supporting Artificial Intelligence)
- ADHA Generic I/O Module (RTU/ICU modules)
- ADHA Specific I/O Module for AOCS sensors & actuators
- ADHA Specific I/O Module for propulsion valves
- ADHA Data Processing Modules
- ADHA Motor Drive Electronic Modules
- ADHA Security Modules for PF and/or PL
- …

21 running activities, 15.1 M€

19 proposed activities, 12.7 M€

AIM D: Develop Building Blocks to support OBCDH module(s) development(s)

Objective:

Develop a portfolio of building blocks techniques to support and ease OBCDHS modules developments

Key Activities:

- COTS activities: selection, characterization, design mitigation techniques, robustness and performance evaluation.

-> See relevant paper "Commercial Off the Shelf Components in Space Avionics and Payload Data Handling".

- Component benchmark activities (OBP mark completion, FPGA / GPU / Accelerators).
- Machine Learning investigations: evaluation & assessment of specific techniques on different HW platforms (NN, Neural Morphic, …)
- Algorithms and relevant datasets (image/video/data compression, data reduction, cloud detection, etc.)

4 running activities,
2.8 M€

33 proposed activities,
12.5 M€

AIM E: Develop EGSE for OBCDH units/modules

Objective:

Develop EGSEs to support the test, integration and verification of OBCDH units/modules and benefit of synergies and commonalities.

Key Future Activities:

- EGSE to test buses, network and communication technologies (SpaceWire, SpaceFibre, Ethernet, TSN, CAN): network simulators, physical layer testing, test bed, bus tester.
- ADHA module crates or racks
- ADHA unit EGSE (incremental approach following the ADHA modularity)

1 running activity,
220 k€

3 proposed activities,
1.6 M€

AIM F: Enhance characteristics/functions of current ASIC Platforms and develop USDM ASIC Platforms

Running evaluation/consolidation activities on several ASIC manufacturing processes and design kits:

12 nm FinFET (GF) - customer chip & IP eval

16 nm FinFET (TSMC) - test chip & IP eval + simulations

22 nm planar FDSOI (GF) - customer chip & test chip & IP eval

65 nm (TSMC & IMEC DK) - customer chip & test chip & IP eval

28 nm & 65 nm (ST) - customer chip eval

150 nm SOI (UMC & MCHP DK, LFoundry & RedCat) - customer chip & test chip & IP eval

180 nm (XFab, UMC & IMEC DK) - customer chip & test chip & IP eval

7 running activities, 14 M€ (ESA 7.7M€ + 6.2M€ EC)

6 proposed activities, 12.4 M€

proposed

6 nm FinFET (TSMC) - test chip & IP eval + simulations

Further development and consolidation of Design Kits and rad hard IP for the various platforms, for high speed digital processing and data communication, detector back-ends, power conversion and control,

AIM G: Improve and expand the European rad-hard FPGA family

Running

European rad-hard FPGA family development and qualification:

>> NanoXplore NG-Medium (65nm), Large, Ultra & Ultra300 (28nm), Ultra6 (6nm)

>> NanoXmap programming tools

Mitigation techniques for complex COTS FPGAs

Reliability evaluation of complex COTS FPGAs

Reliable reconfiguration of FPGAs on-board

15 running activities, 31M€ (ESA 7.6M€ + 13M€ EC + 10.4M€ national prog)

4 proposed activities, 1.5 M€

proposed

Evaluation and demos of embedded FPGA IPs and tools

More evaluations of non-European FPGAs (e.g. PolarFire, KU060)

AIM H: Improve and expand the European rad-hard Microprocessors, Microcontrollers and DSPs

Running

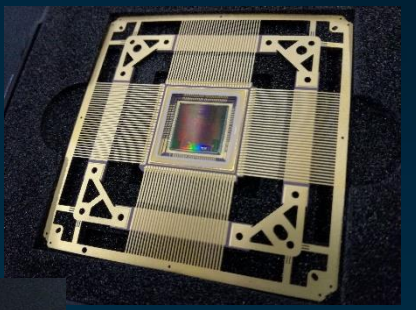
European rad-hard microprocessors and microcontrollers development and qualification:

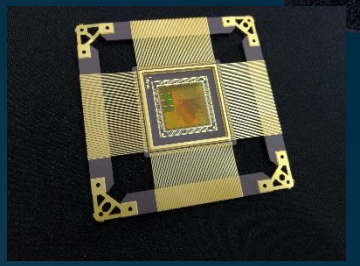
>> based on LEON (SPARC) - Cobham Gaisler GR740 (LEON4), GR765 (LEON5), GR7xV(RISC-V)

>> based on RISC-V - GR7xV(RISC-V)

>> based on ARM – Microchip SAM family

>> other processor cores (e.g. DPC TAS-BE, MORAL IHP Peaktop)





proposed

RISC-V instruction extensions, SW tool ecosystem

RISC-V Fifth Generation Space Microprocessor (VGSM) EM and FM

Next generation ARM MCU (55nm) and MPU (28nm)

Space Microcontroller with open instruction set architecture

14 running activities, 14.2M€ (ESA 9.1M€ + 3M€ EC + 2.1M€ national prog)

4 proposed activities, 6.9 M€

AIM I Improve and expand the European rad-hard ASSP family

Running

European rad-hard Application Specific Standard Products (ASSP) development and qualification:

>> Latch-up protection

>> ADC, DAC

>> electro-optical transceivers

>> power conversion, conditioning and control

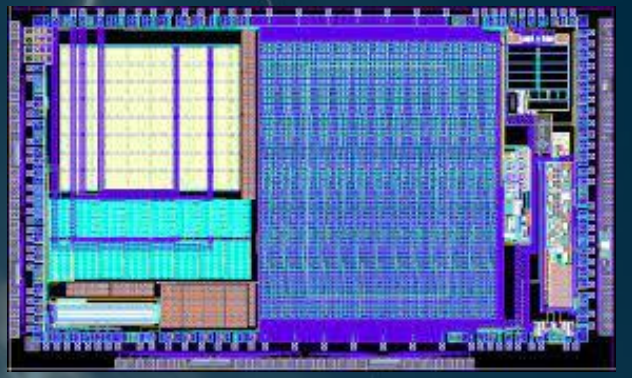
>> LVDS drivers/receivers

>> evaluation of non volatile memories

>> frequency synthesizers

>> high speed communication interfaces and switches (e.g. Space Fiber chips)

>> Telecommand and Telemetry encoder/decoder chips



27 running activities, 21.7 M€ (ESA 13.1M€ + 7.2 M€ EC + 1.4 M€ national prog)

proposed

New developments, evaluations (also of COTS devices), qualifications

22 proposed activities, 28.7 M€

AIM J: Improve and expand the European IP Cores catalogue and respective Design Methods and Tools

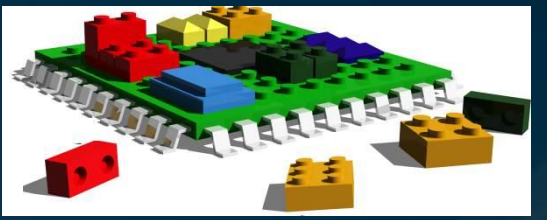
Running

ESA IP Cores catalogue maintenance and expansion (e.g. CCSDS data compression and optical data TX, LEON ISA extensions, ADC, ADPLL)

Universal VHDL Verification Methodology and tools

HW-SW co-design virtual platforms and demos (e.g. TERMA SkyRocket)

Functional and rad characterisation of COTS components



proposed

AI with FPGAs (IPs and tools)

New IP Cores (AMBA to AXI bridge, supervisors for COTS devices, RISC-V extensions, high speed communications, DSP accelerators, ADHA functions/interfaces, TSN, TTEthernet, etc.)

Validation tests functional coverage methods and tools

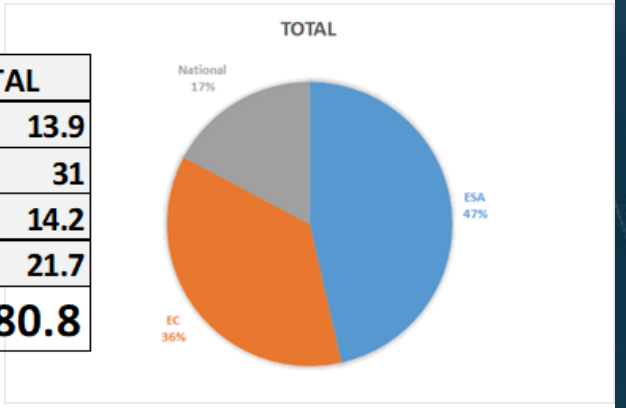
Mitigation techniques for COTS and rad tolerant (non rad hard) FPGAs

16 running activities, 3.6 M€ (ESA)

17 proposed activities, 5.5 M€

Only **running** and **funded** 64 activities, in M€

	ESA	EC	National	TOTAL
ASIC	7.7	6.2	0	**13.9**
FPGA	7.6	13	10.4	**31**
mP/mC	9.1	3	2.1	**14.2**
ASSPs	13.1	7.2	1.4	**21.7**
TOTAL	**37.5**	**29.4**	**13.9**	**80.8**



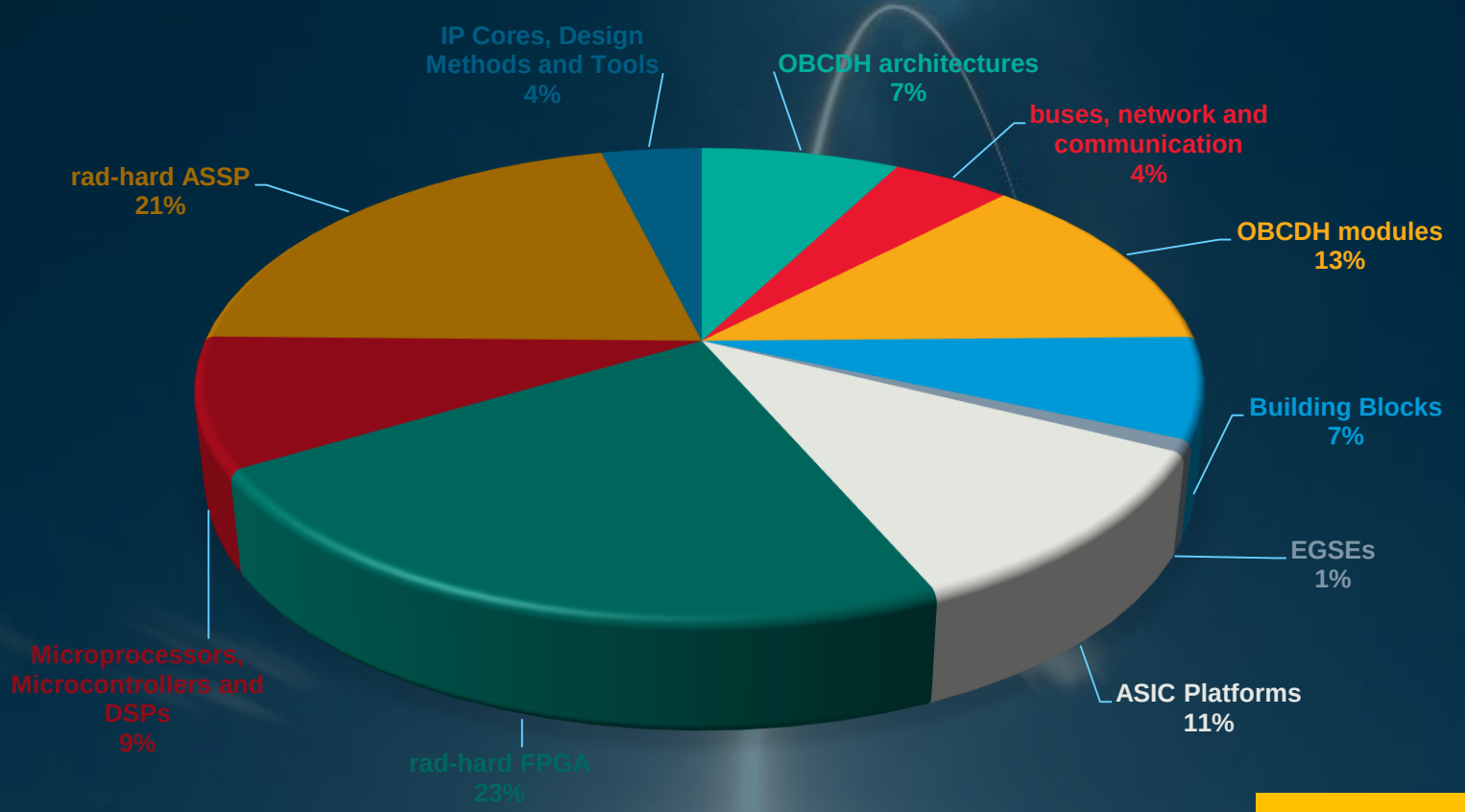
Plus 16 more activities for IP Cores, tools and methods – 3.6 M€

New (not funded) activity proposals

	NEW proposals	# proposals
ASIC	12.4	6
FPGA	1.5	4
mP/mC	6.9	8
ASSPs	28.7	22
IP Cores, tools	5.5	17
TOTAL	**55**	**57**

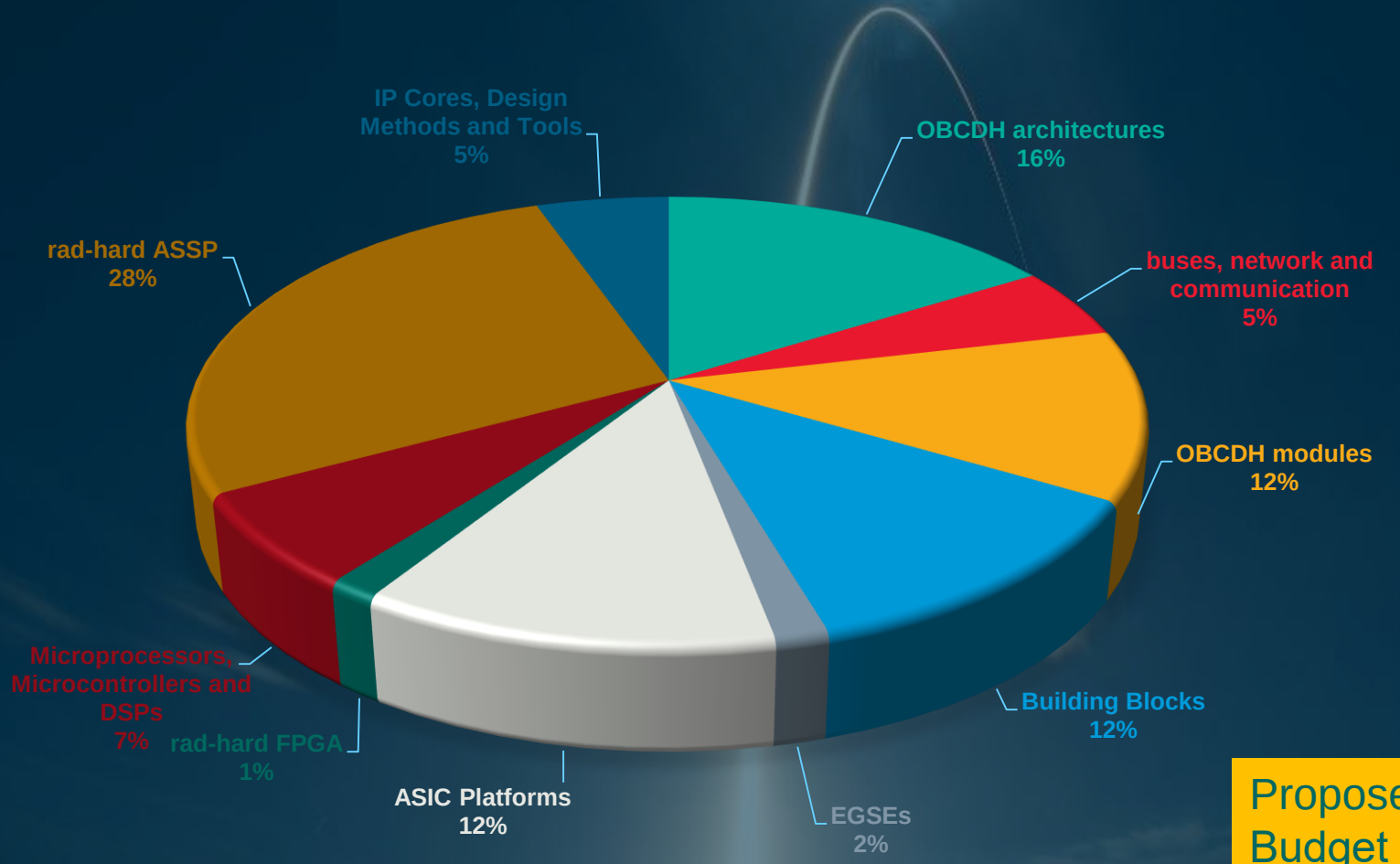
- UDSM ASIC platform+devices
- European RISC-V for space
- European FPGAs
- Mixed-signal ASSPs (ADC/DAC/power/high speed i/f)
- IPs to support all

Budget: Running and Proposed Activities



Running and Proposed activities: Total Budget of 220.7 M€

Budget: Proposed Activities



Proposed activities: Total Budget of 104 M€

Conclusions

A new THD dossier OBCDHSM is now available **(*)** with its detailed Road Map

It has been organized in three technology families

- Technology Family 1: CDHS Architecture, units, modules and communication systems
- Technology Family 2: Microelectronic devices and enabling technology
- Technology Family 3: CDHS EGSEs & Microelectronics Development methods and tools

The objectives have been organized in 10 AIMs with a top-down approach from DHS architecture down to microelectronics.

A total budget of 104 M€ is proposed for **130** future activities on top of the 116.7 M€ budget for **131** running activities.

(*) All European space sector stakeholders can request an access to the Harmonisation Document Management System (HDMS/DCCM: https://tec-polaris.esa.int/eclipse) by sending an e-mail to harmo@esa.int (providing business affiliation and position in the company).

Q/A session

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