GOMX5 Advanced Payload including new European space components

18 November 2021

Roland Weigand, ESA Microelectronics Section

GOMX-5 IOD – A Cross-TEC Collaboration

GNSS PPP receiver (TEC-ESN)

Syrlinks

Dual-band GNSS antenna (TEC-EFA)

ANYWAVES

X-band Reflectarray antenna (TEC-EFA)

TICRA

GNSS PPP receiver (TEC-ESN)

deimos SPACE

AI FDIR experiment

aiko INTELLIGENT SPACE SYSTEMS

Radiation monitor (TEC-EPS)

CZECH TECHNICAL UNIVERSITY IN PRAGUE

BRAVE-Large, GR716 & GR740 processors (TEC-EDM)

UNIVERSIDADE FEDERAL DE SANTA CATARINA

COBHAM Cobham Gaisler AB

gmv

Electric propulsion (TEC-MPE)

ThrustMe

4x mini star trackers (TEC-SAS)

arcsec

Radiation monitor

CERN

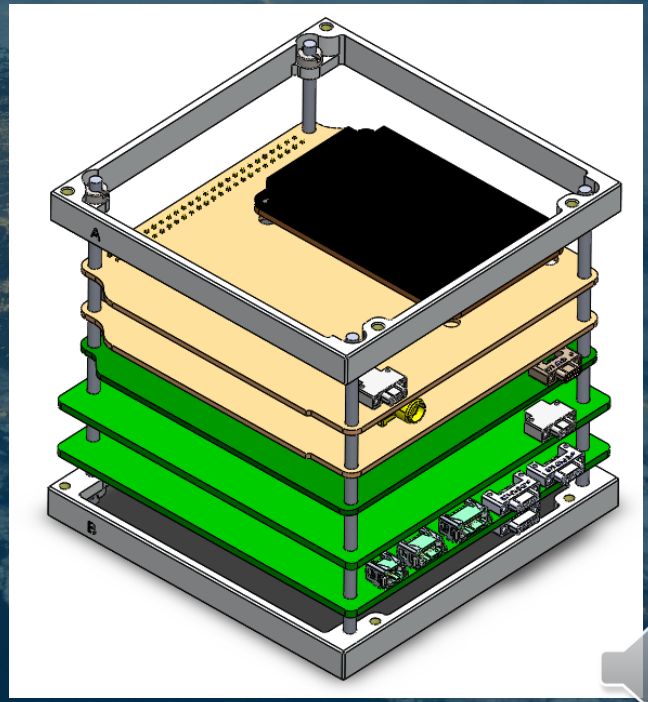
Multispectral imager (TEC-MMO)

TARTU OBSERVATORY space research centre

Launch: Q4 2022

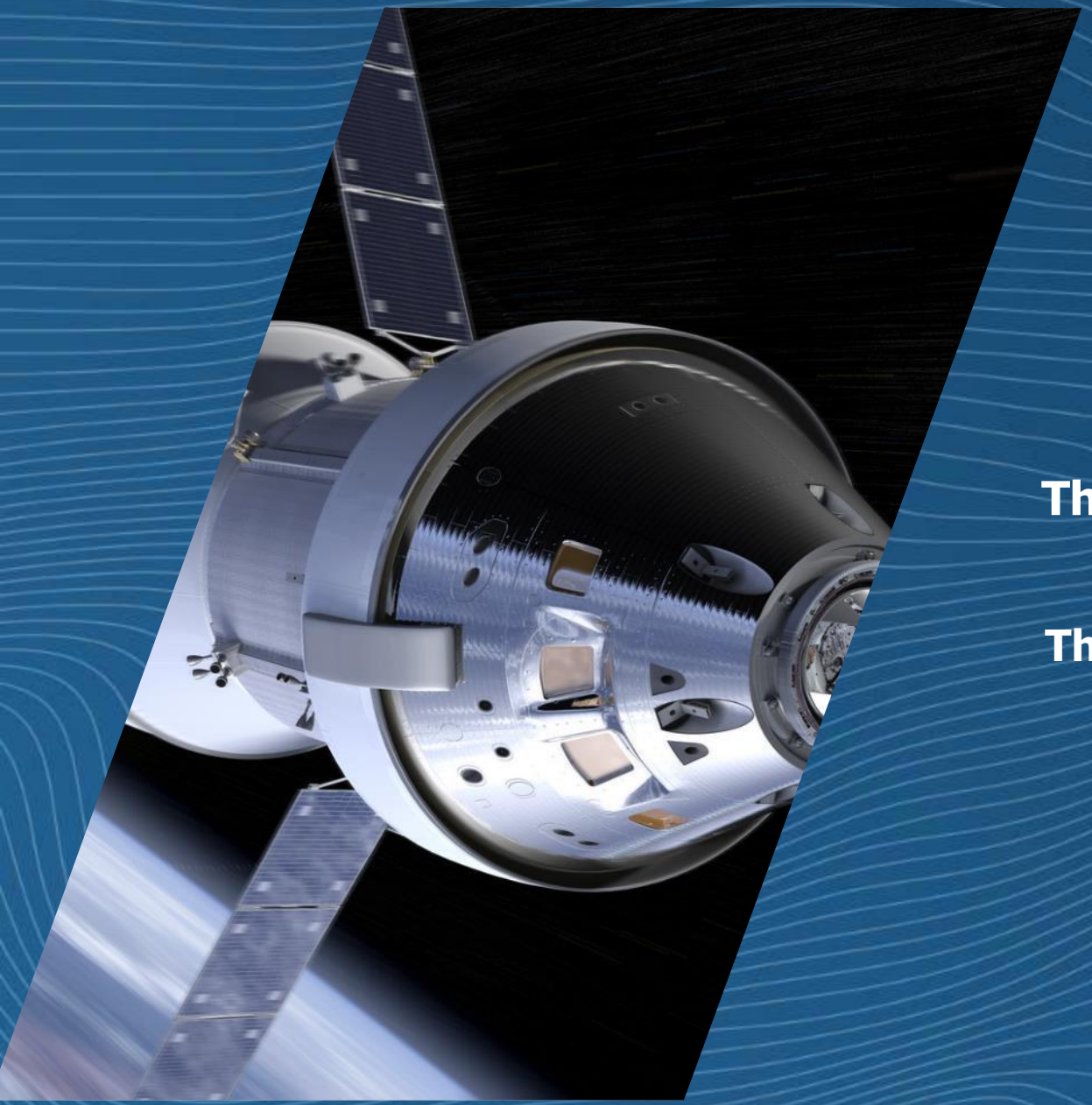
GOMX-5 APPs (Advanced Payload Processors)

- GOMX-5 Cubesat by GOMspace, launch 2022
- IOD Payload unit with 5 PCI104 boards (10x10x10cm)
- GR740 LEON4-Quad-Core
- GR716 LEON3 Microcontroller
- NOEL-V / LEON5 Test Chip
- Nanoxplore (BRAVE) NX-Large FPGA
- Xilinx Zynq FPGA, GNSS Front-End
- GNSS Receivers on GR740 and Zynq
- Informal consortium:



The Presenters

- Arne Samuelsson (Cobham Gaisler, SE)
  - → GR740, GR716, LEON-5/NOEL-V processors
- Artur Kobyłkiewicz (GMV, PL)
  - → GNSS hardware (front-end and Zynq board)
  - → GNSS SW Receiver
  - Team with CBK (Centrum Badań Kosmicznych, Polish Academy of Science)
- Eduardo Augusto Bezerra (UFSC Universidade Federal de Santa Catarina, BR)
  - Department of Electrical / Electronic Engineering, Florianopolis, BR
  - Prior experience developing a NG-Medium board for FloripaSat
  - → NG-Large FPGA board



CAES PIONEERING ADVANCED ELECTRONICS

GOMX-5 APPs

The Advanced Payload Processors IOD for the GOMX-5 Mission

The 15th ESA Workshop on Avionics, Data, Control and Software Systems (ADCSS) 2021-11-18

Arne Samuelsson

2021-11-18

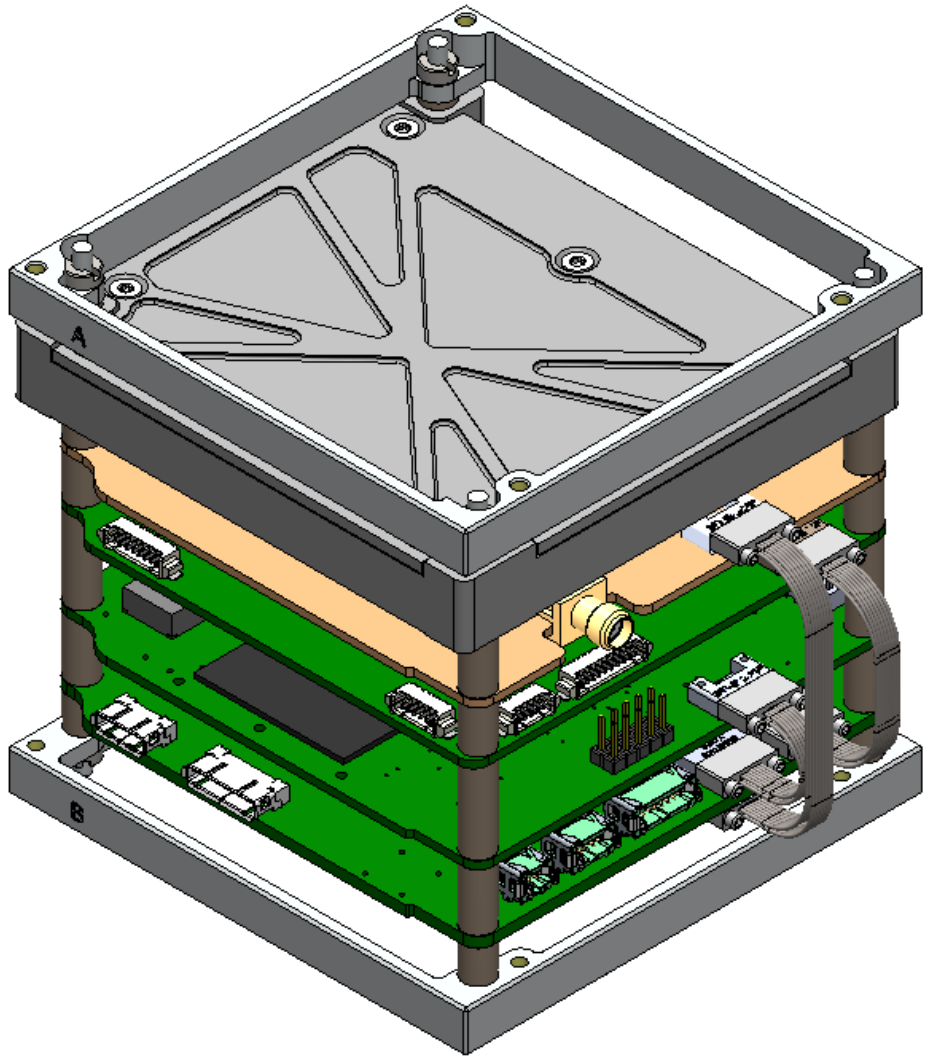
Contents

- Introduction
- APPs design
- APPs GR740 board
- APPs GR716 board
- Main components
- Objectives and experiments
- Test campaign

Introduction

Main objective

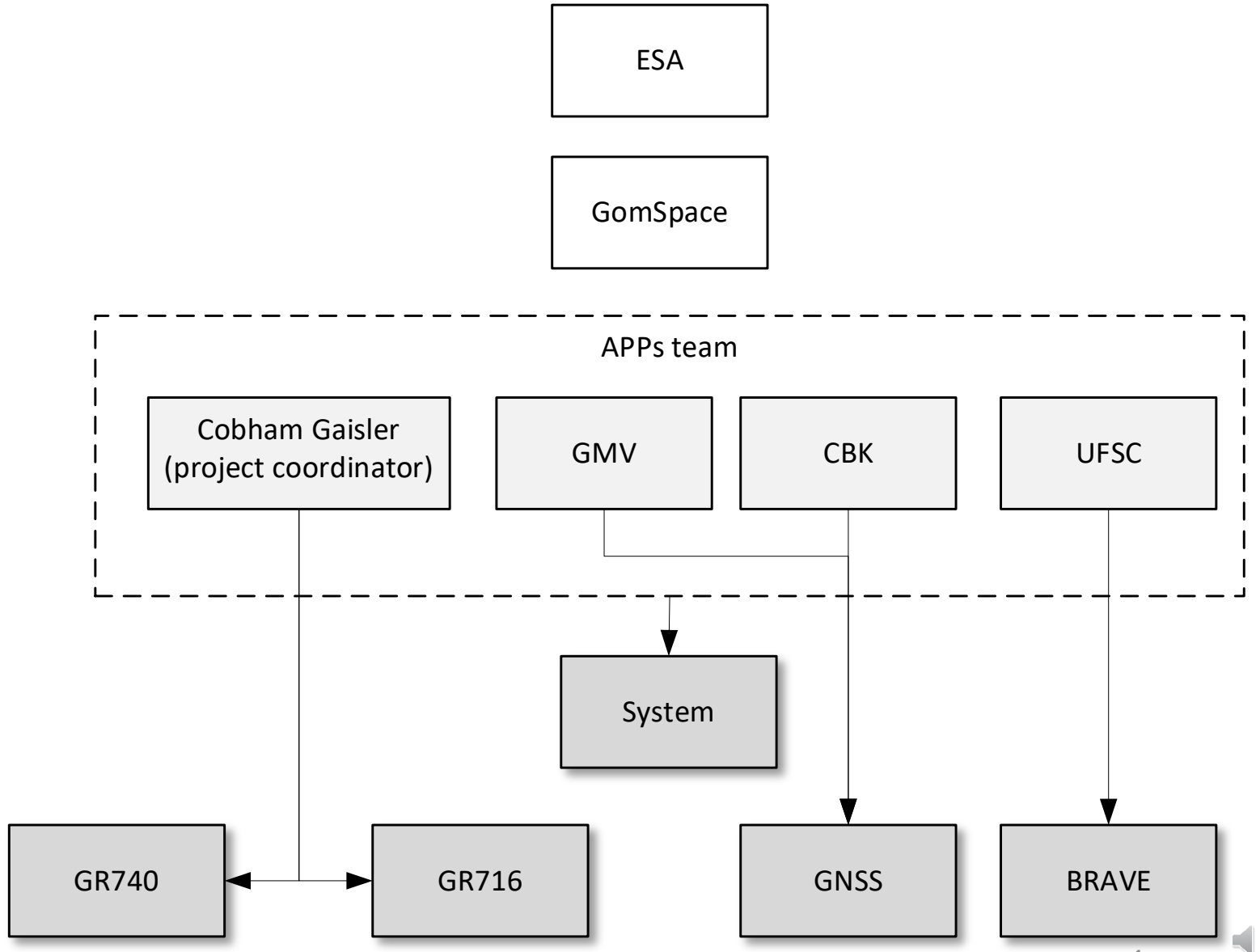
- Demonstrate multiple processing technologies developed within ESA activities and acquire flight heritage from related components
- By means of
  - Combination of processors and reconfigurable logic in APPs allowing for multiple IOD experiments.
  - Realization in the Advanced Payload Processors (APPs) 1U size payload module



Introduction

Consortium and responsibilities

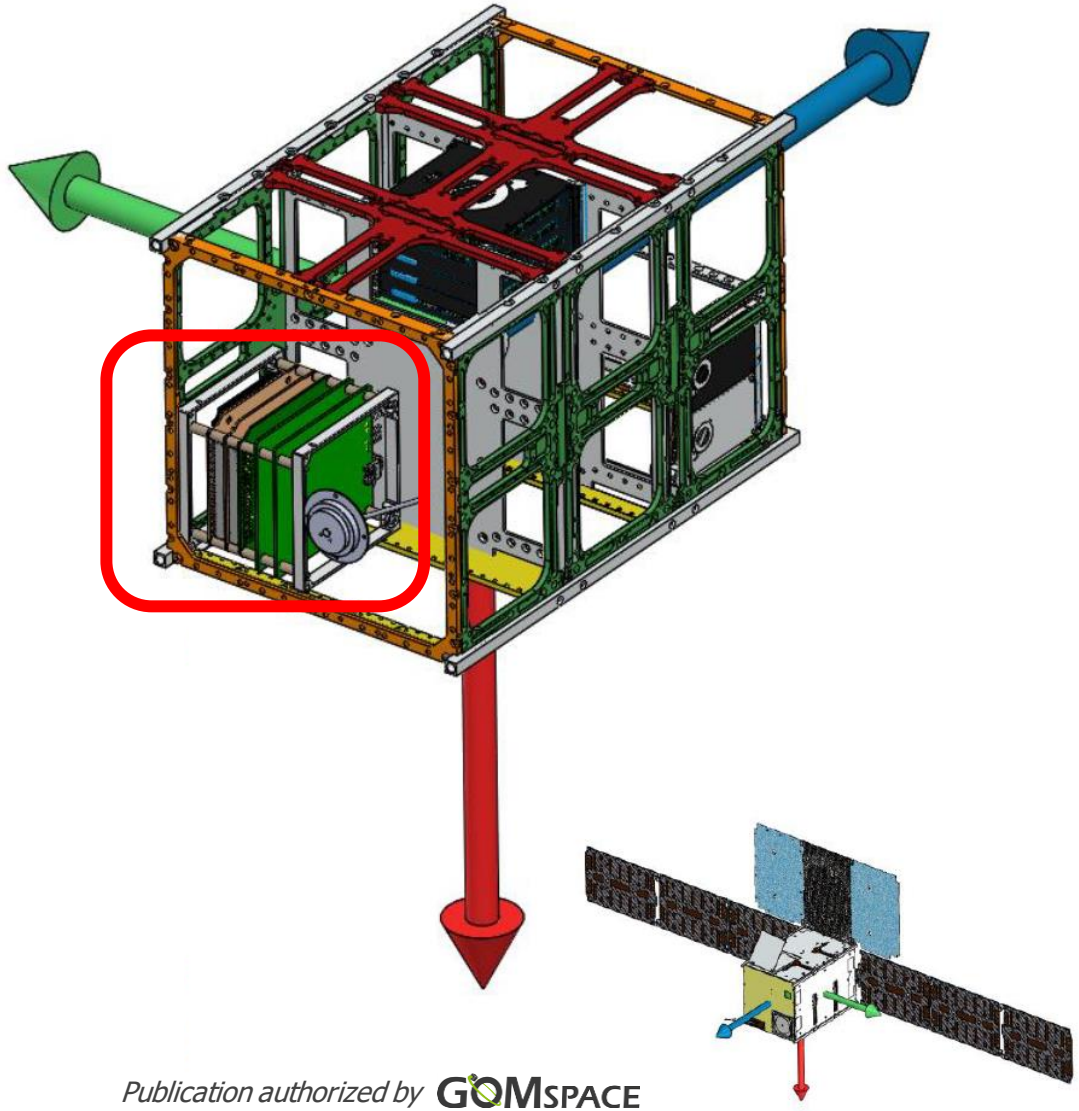
- Cobham Gaisler AB, Göteborg, Sweden
- Centrum Badań Kosmicznych Polskiej Akademii Nauk, Warsaw, Poland
- GMV Innovating Solutions Sp, Warsaw, Poland
- Space Technology Research Laboratory, UFSC, Florianópolis, Brazil



APPs design

Spacecraft integration

Integrated as a 1U module in the 12U GOMX-5 satellite developed by Gomspace

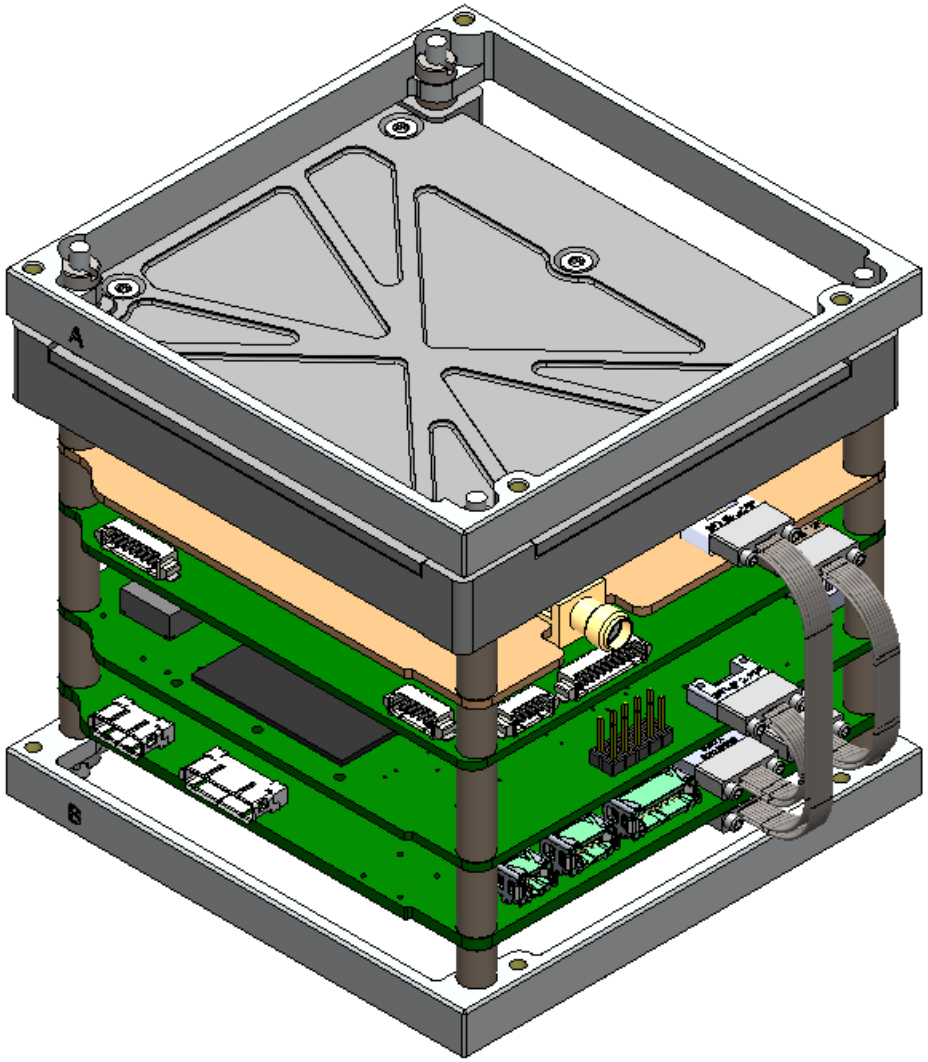


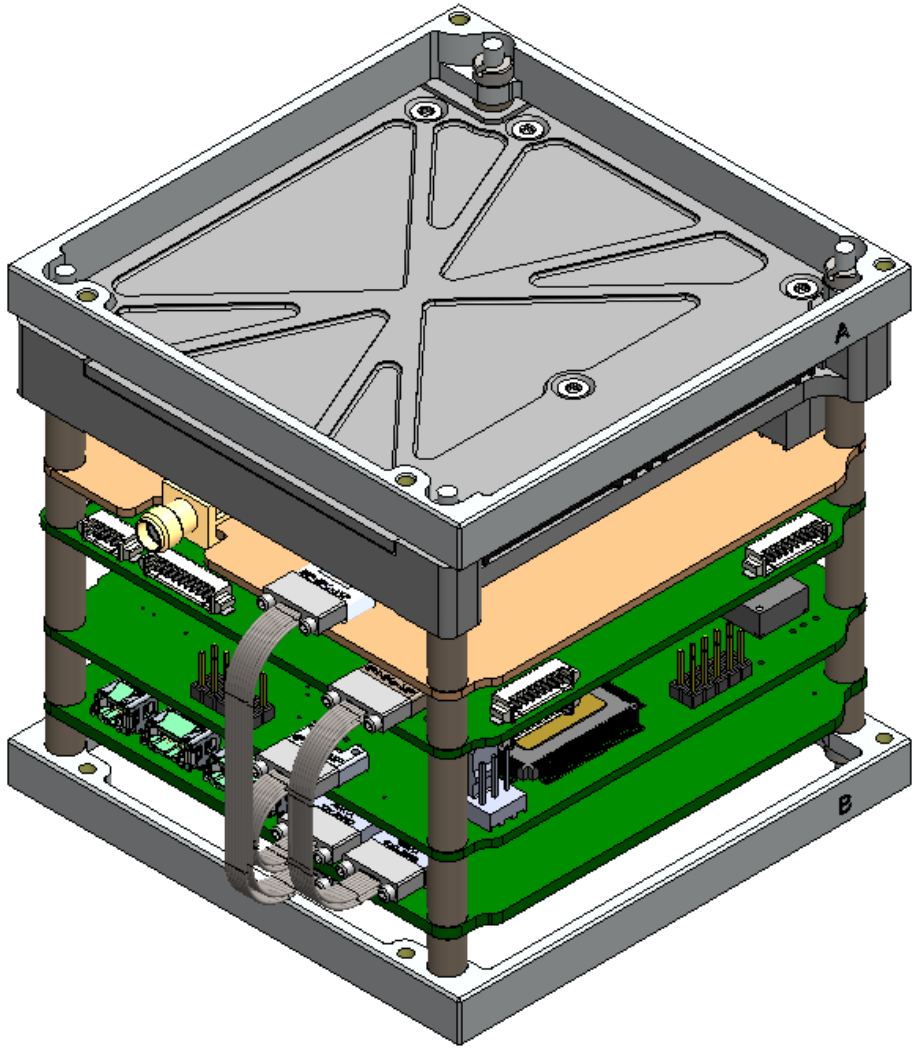
GOMX-5
ENABLING THE CONSTELLATIONS OF TOMORROW

Publication authorized by GOMSPACE

APPs design

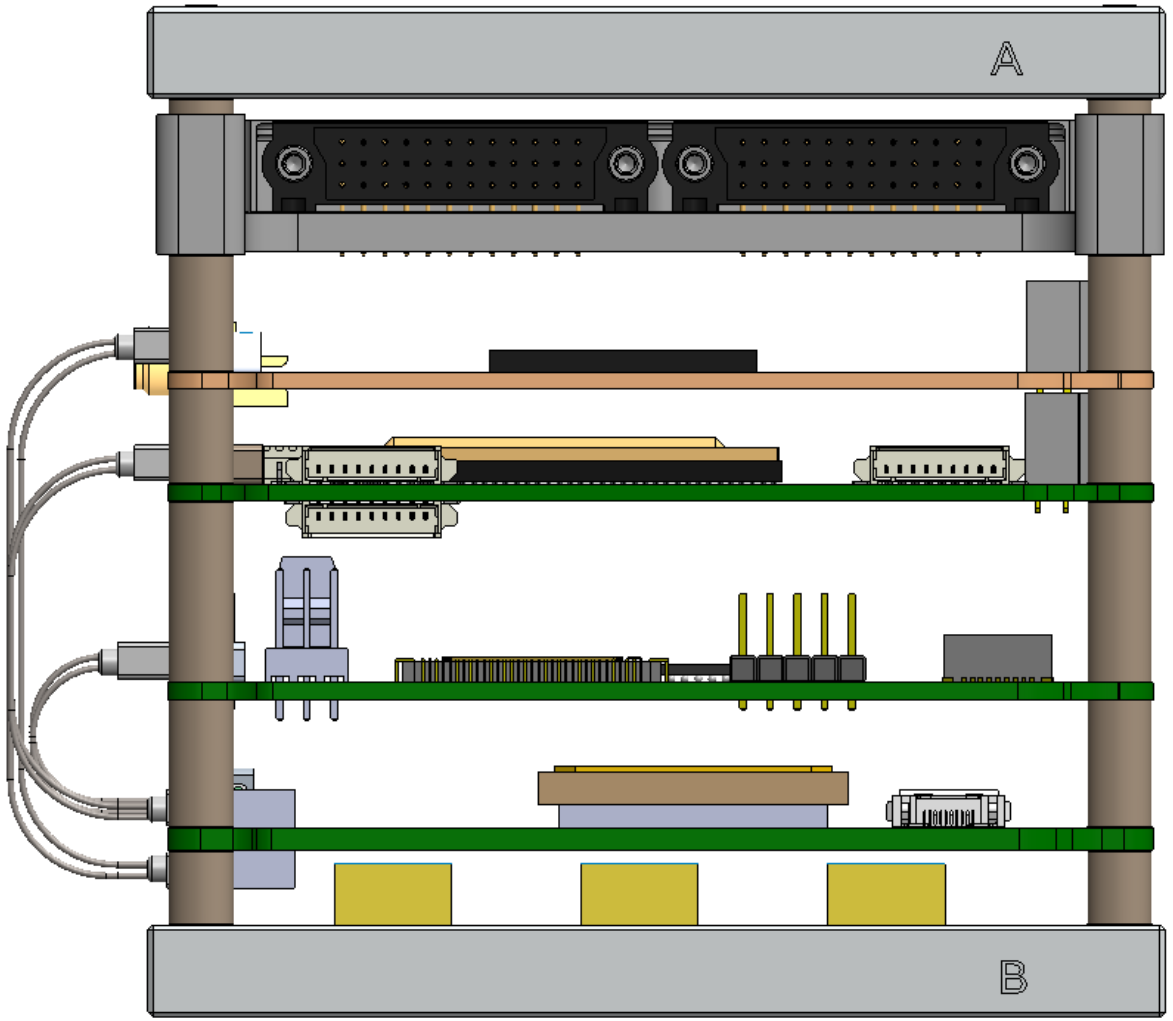
Five stacked boards





APPs design

Main functionalities of the boards

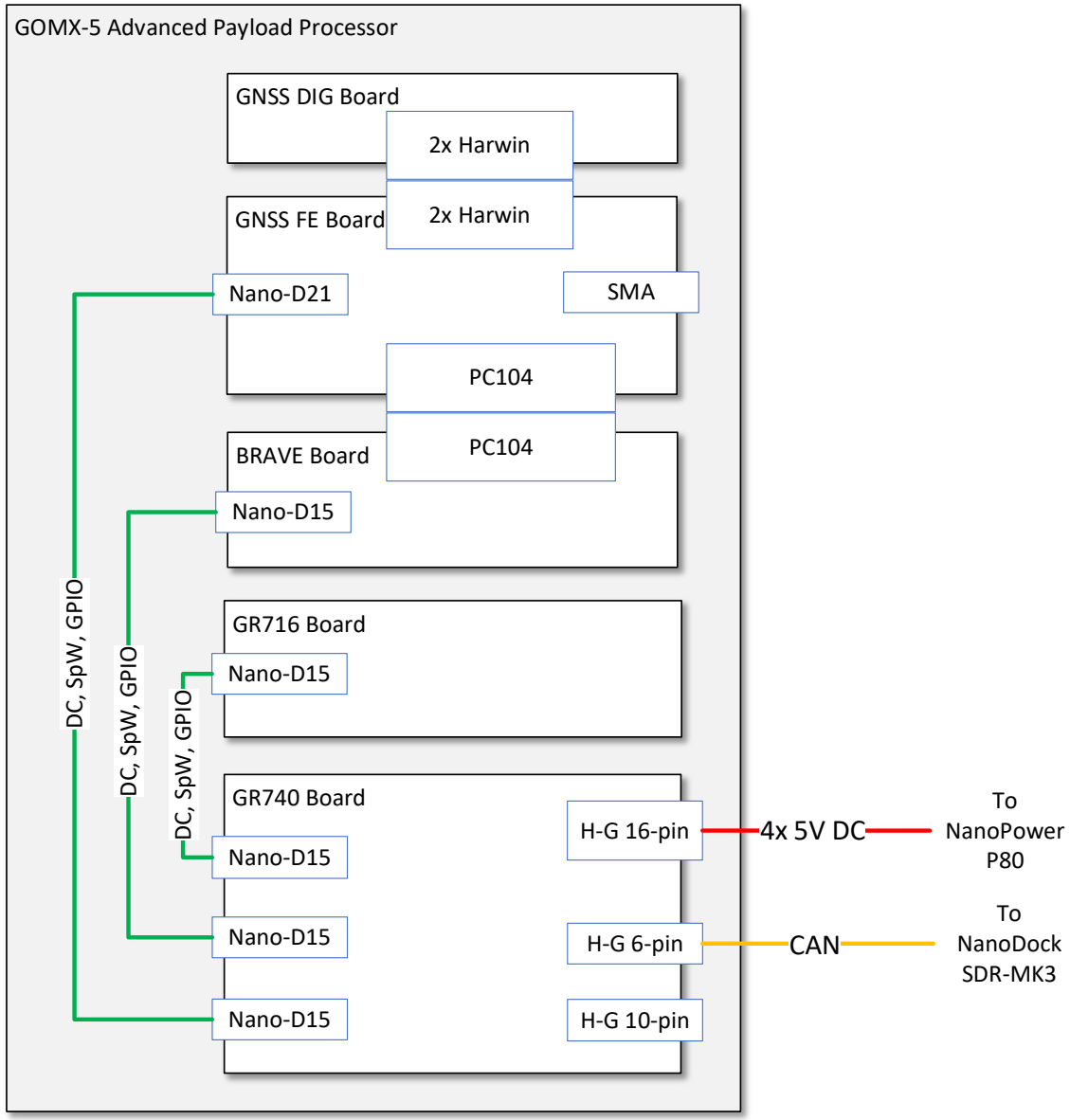


- GNSS Digital[1)]
  - Processor part of GNSS Software Defined Receiver
- GNSS RF Frontend[1)]
  - RF frontend part of GNSS Software Defined Receiver
- BRAVE[1)]
  - Reconfigurable NG-Large FPGA supported by microcontroller
- GR716
  - Microcontroller accompanied by co-processor (LEON5/NOEL-V demonstrator) and radiation sensor
- GR740
  - High performance processor
  - APPs cube controller, power and communication router

1) Separate presentations

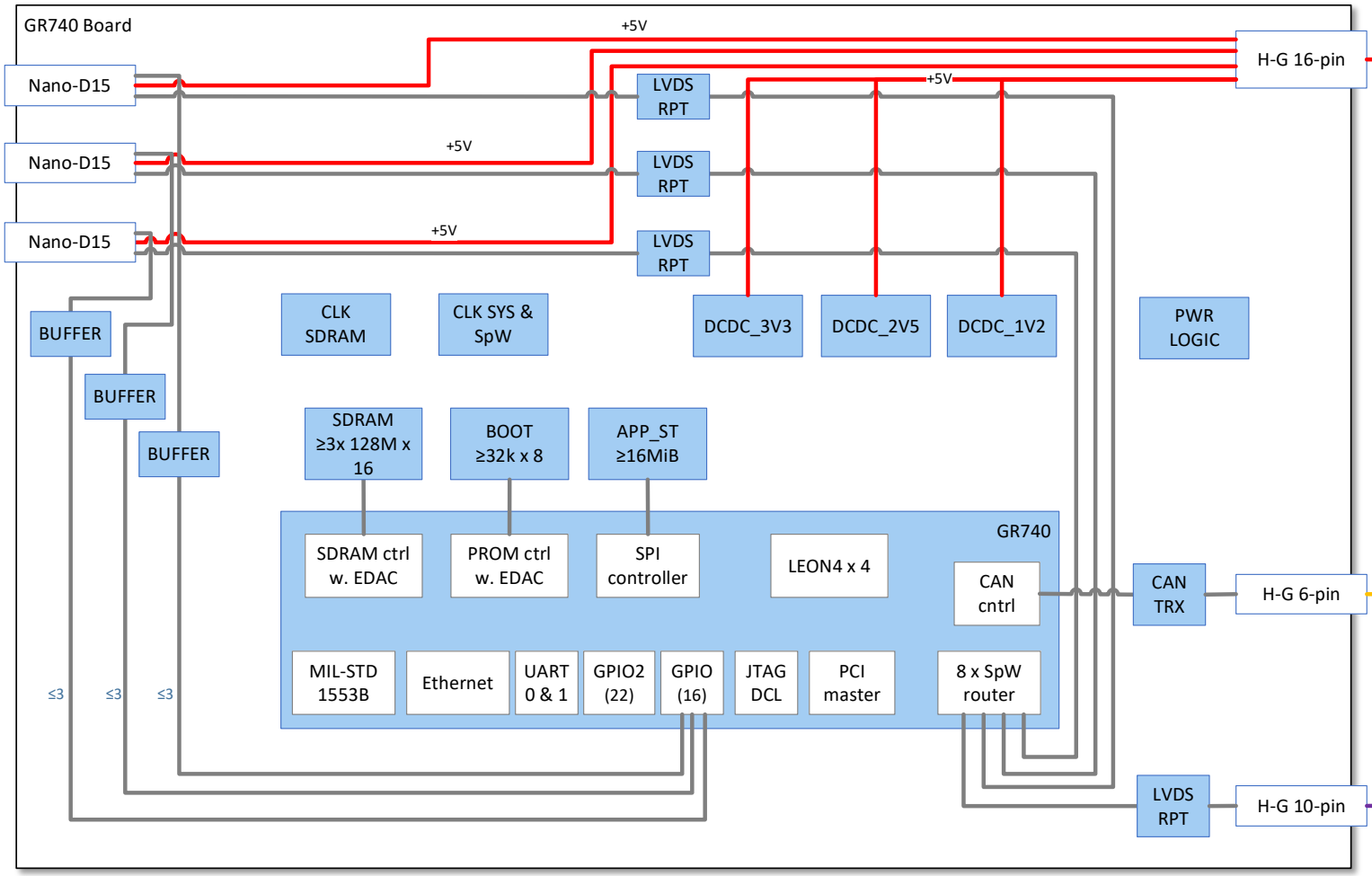
APPs design

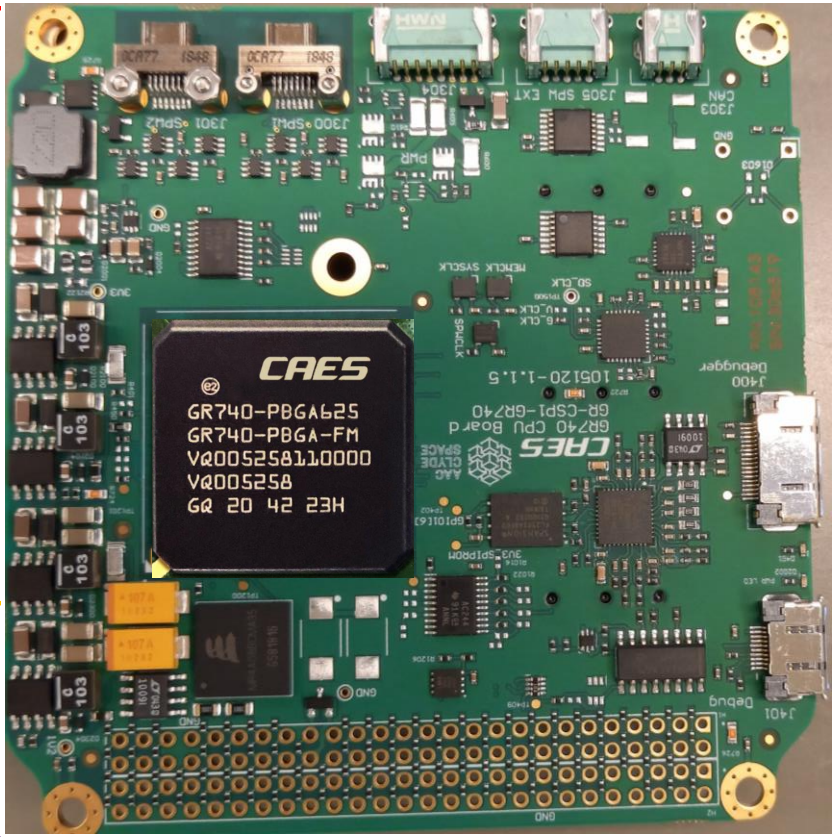
System architecture – internal and external interfaces



APPs GR740 board

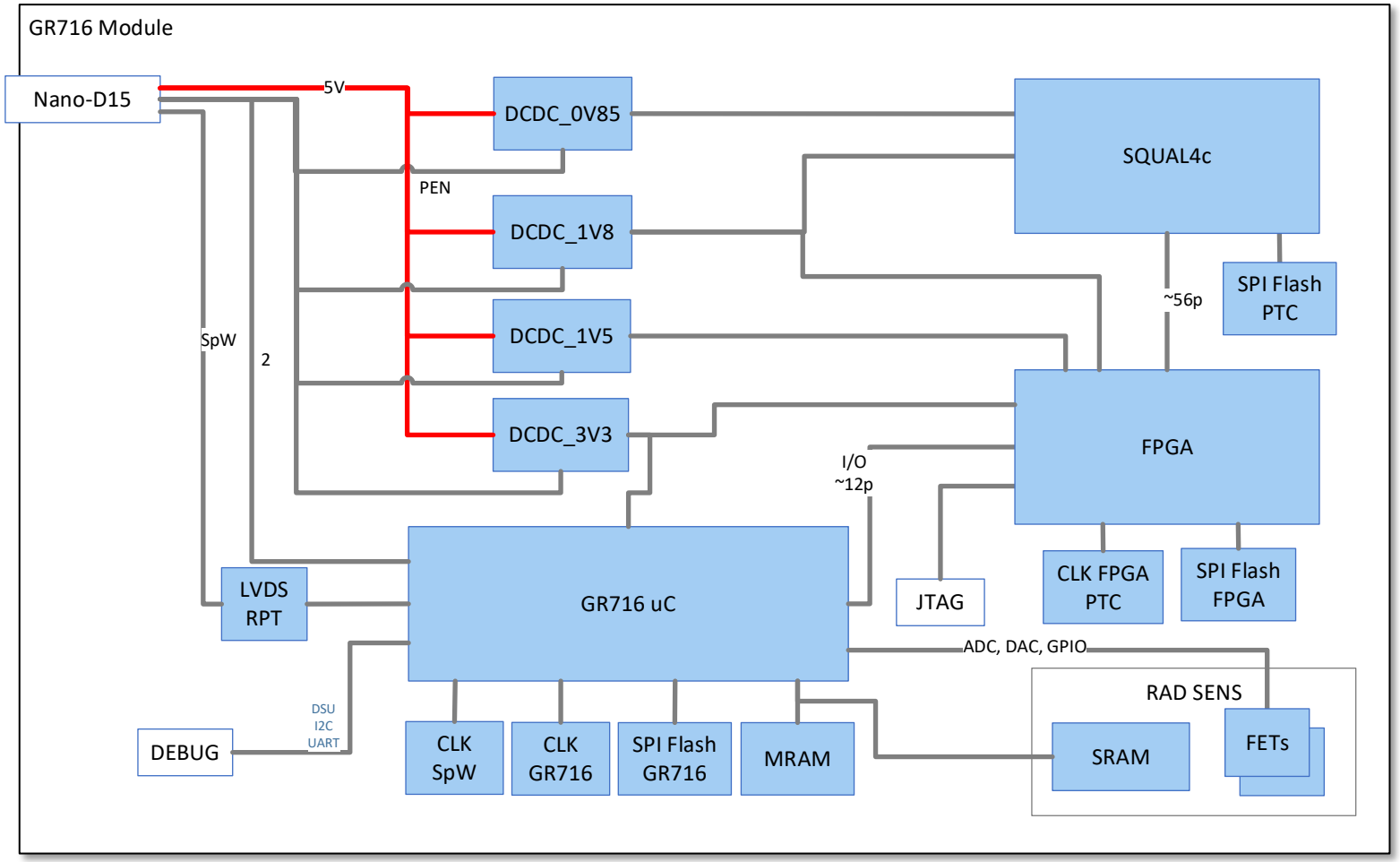
Architecture and realization

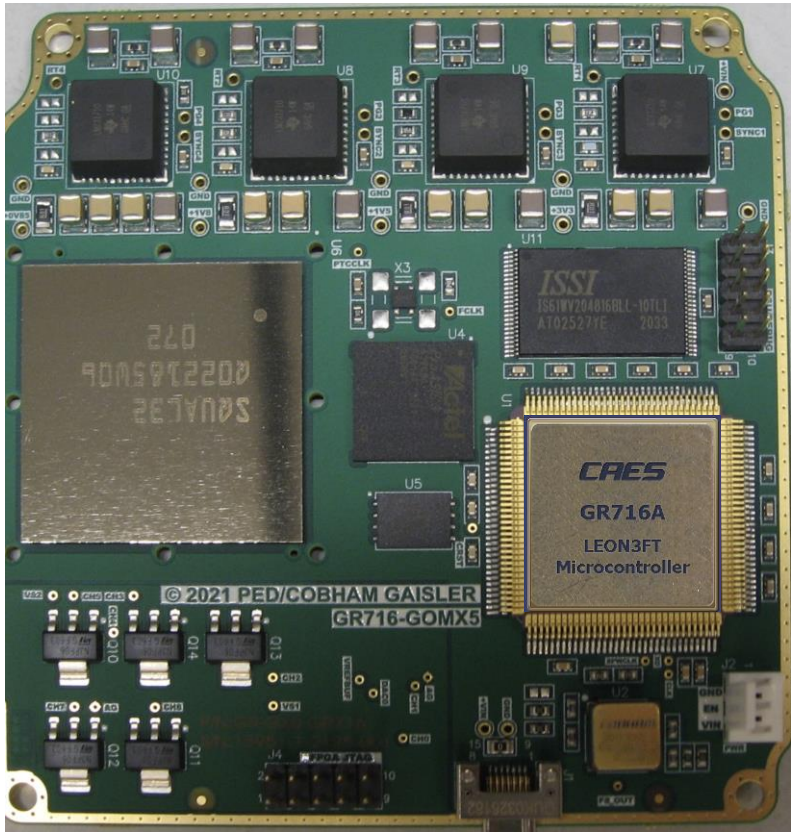




APPs GR716 board

Architecture and realization



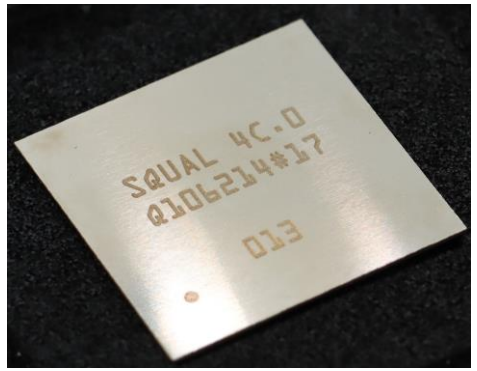


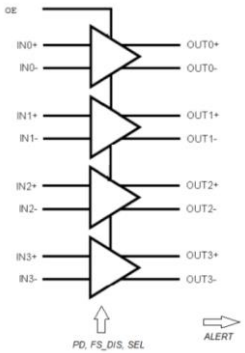
Main components

GR740 and GR716 boards

- GR740-PBGA - Quad-Core LEON4 SPARC V8 Processor
  - Plastic version of the radiation-hard quad-core fault-tolerant LEON4 SPARC V8 processor targeting space constellations
  - Same functionality, fault-tolerance and radiation-hardness as the GR740 system-on-chip device in ceramic package
  - Plastic Ball Grid Array (PBGA) with 625 balls, footprint compatible the GR740 Ceramic Column Grid Array (CCGA)
- GR716A - LEON3FT Microcontroller
  - Fault-tolerant SPARC V8 32-bit processor

- SQUAL4c - LEON5/NOEL-V demonstrator
  - LEON5 and NOEL-V silicon proven on STM 28nm GEO P2
  - Rad-hard demonstrator with LEON5FT SPARC V8 32-bit processor and NOEL-V RISC-V 64-bit processor
- Quad LVDS Buffer/Repeater
  - Part no GR54LVDS054PZ
  - Dedicated design for SpaceWire interfacing
  - 25-pad ceramic land grid array package
  - Radiation hard >300 krad (Si), SEL and SEE immune





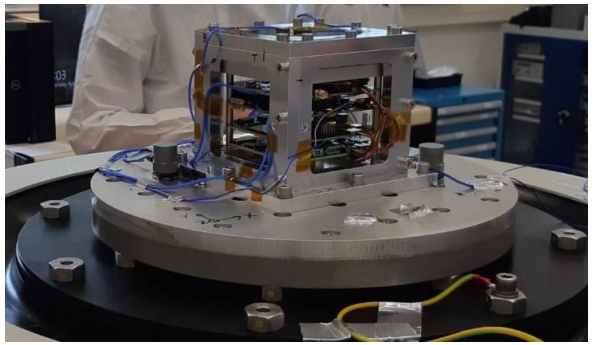
Objectives and experiments

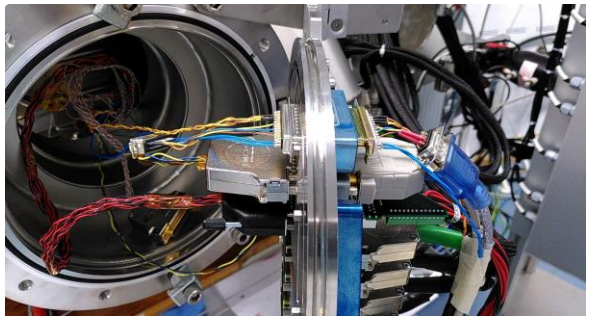
GR740 and GR716 boards

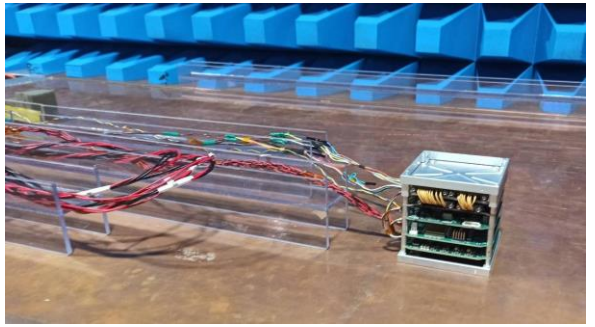
- GR740 board
  - Main objective
    - Acquire flight heritage for GR740-PBGA and GR740 SBC design for cubesats
    - APPs cube control
  - Experiments
    - Processing and memory resource for off-board experiments via SpW (mono-frequency receiver for GNSS SDR experiments (with GMV) and BRAVE board reconfiguration (with UFSC)
    - Memory error detection and correction
- GR716 board
  - Main objective
    - Acquire flight heritage GR716 Microcontroller, LEON5/NOEL-V demonstrator and Quad LVDS Buffer/Repeater
  - Experiments
    - High-performance processing and memory tests
    - Monitor radiation events in low-power mode

Test campaign

- Environmental tests
  - Vibration
  - Thermal vacuum
  - EMC
  - First phase completed at ESTEC, analyses on-going
- Complementary integration tests
  - Functions and performance
  - On-going with each partner







For further information and inquiries

- www.caes.com/gaisler
- sales@gaisler.com

- Thank you for listening!

CAES

PIONEERING ADVANCED ELECTRONICS

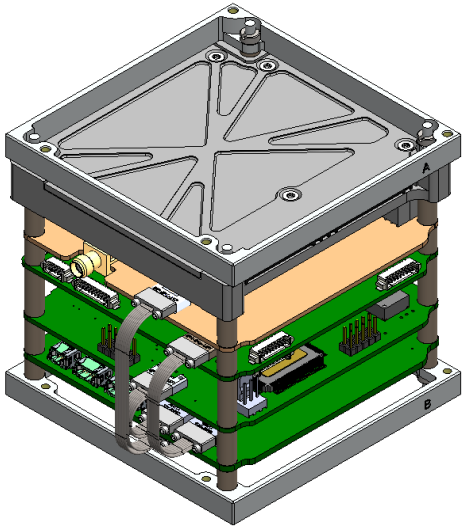
GNSS Software Receiver In Orbit Demonstration on the GOMX-5 Mission

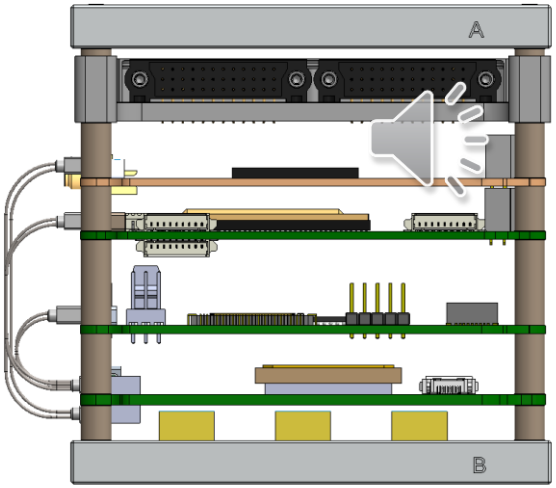
ESA ADCSS 2021

gmv INNOVATING SOLUTIONS

APPs on GOMX-5

Advanced **P**ayload **P**rocessor**s** is 1U module that will be integrated within the 12U GOMX-5 platform provided by GomSpace.





GNSS Digital + RF Front-end
Dual Frequency GNSS SDR Receiver

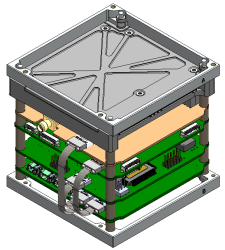
Brave Board
Reconfigurable NG-Large FPGA supported by microcontroller

GR716
Microcontroller accompanied by co-processor and radiation sensor

GR740
High performance processor

APPs cube controller, power and communication router

GNSSW Experiments on GOMX-5



APPs

Dual Frequency GNSSW Receiver

Implemented on the Zynq7030 ARM processor.

Single Frequency GNSSW Receiver

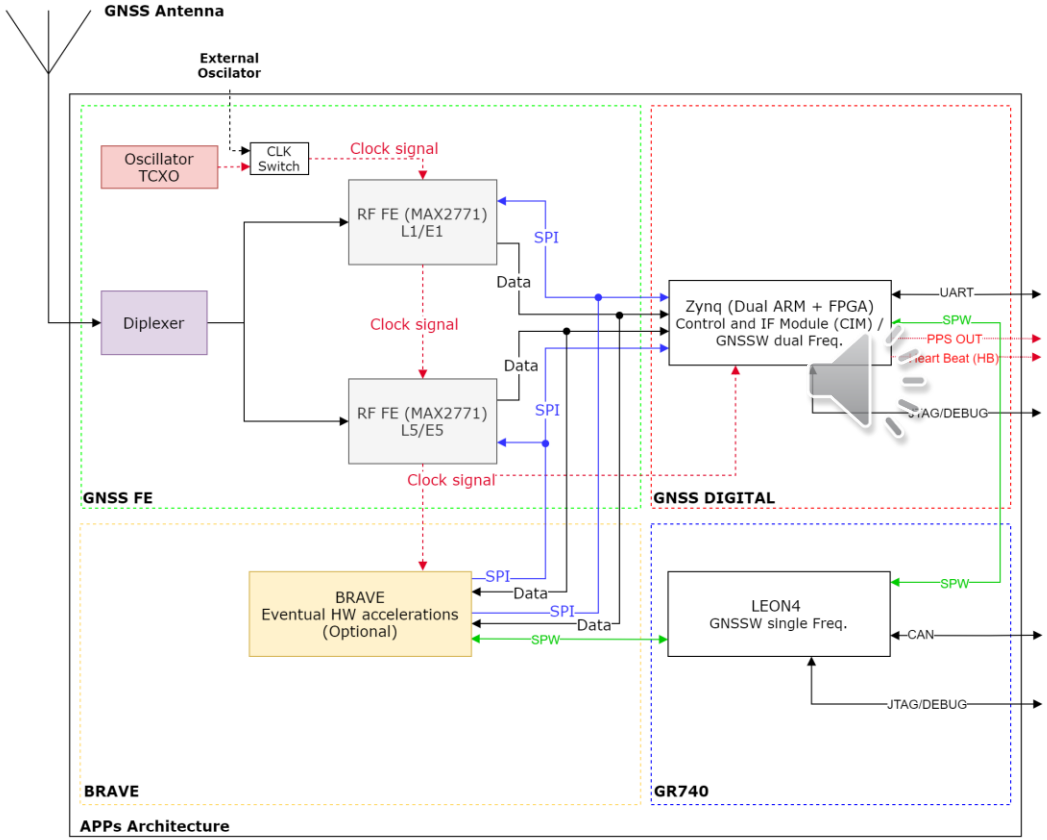
Implemented on the GR740 LEON4 processor.
Raw data samples feed through SpW by the Zynq.

FE Reconfiguration
Using Brave (optional).

FFT Acquisition in FPGA
Using Brave (optional).

Raw Data Packetizing
Using Brave (optional).

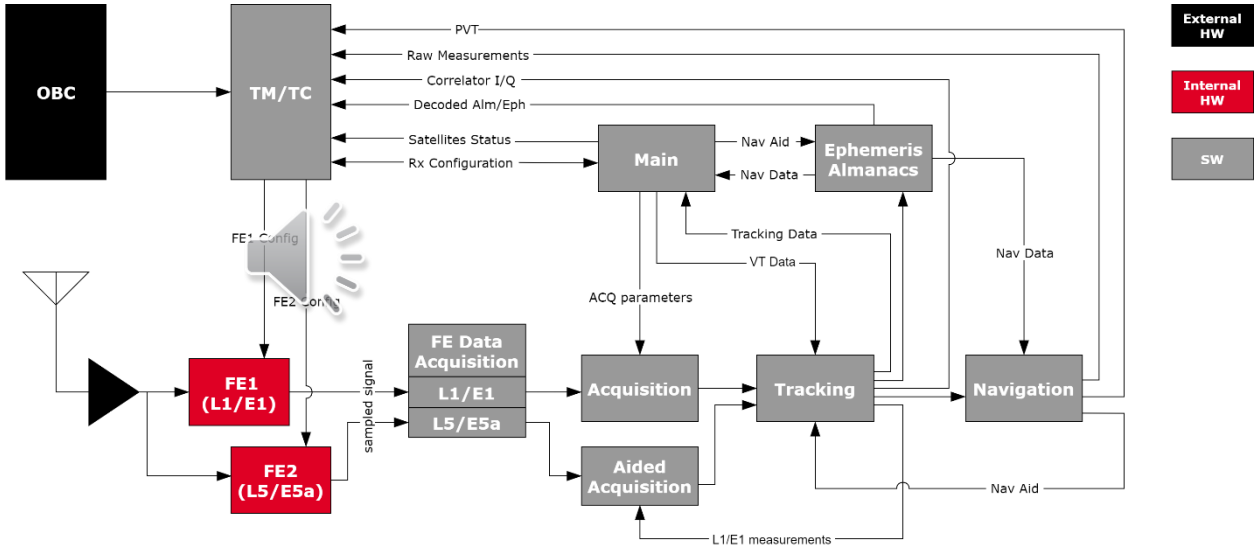
HW Platform



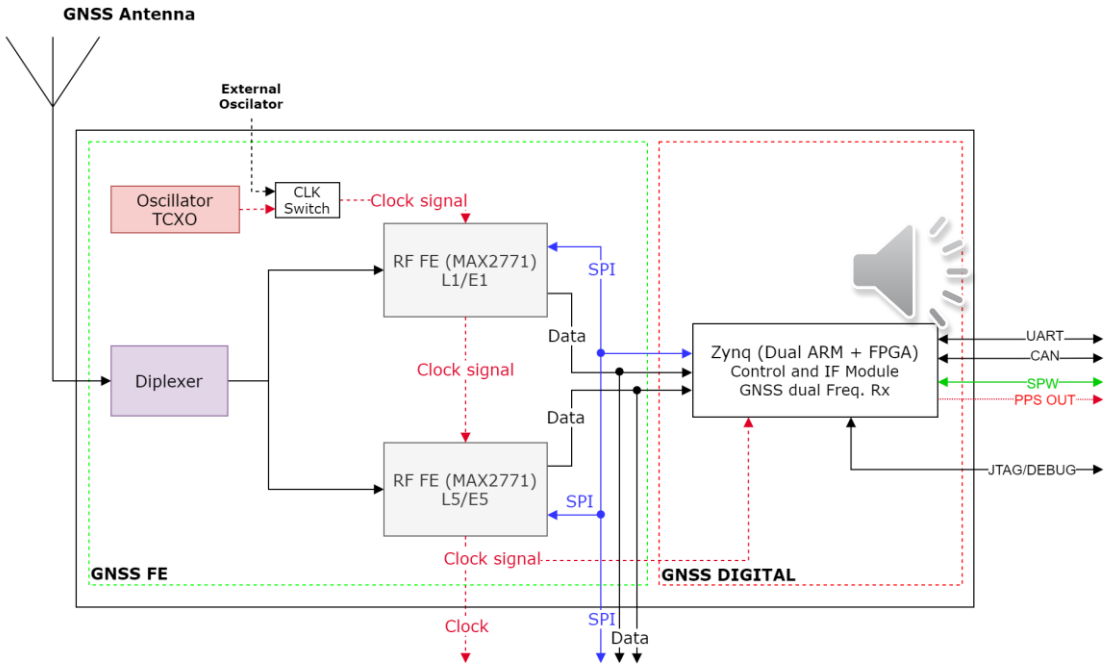
- **Modular approach** that allows to run GNSSW Receiver on multiple HW configurations
- Powerfull **ZYNQ7030** dual core processor with 1GB of SDRAM (integrated FPGA could be used as a coprocessor or allows to implement additional interfaces)
- **BRAVE** board with NG-Large FPGA that optionaly enables HW acceleration of some GNSSW functionalities or can be used for the FE interface
- **LEON4** that allows to run separate instance of GNSSW Receiver and will be used as a Management System for the whole payload
- Two **Front-end** RF channels: L1/E1 and L5/E5 (2x MAX2771)

SW Approach

- Modular approach that allows in depth configurability by TC or SW update
- Configurable monitoring through TM
- Main block is initializing and managing data processing
- NAV data can be used to aid ACQ or TCK tasks
- Acquisition of L5/E5 signals is made by L1/E1 measurements aiding
- Separate buffers for the two frequencies

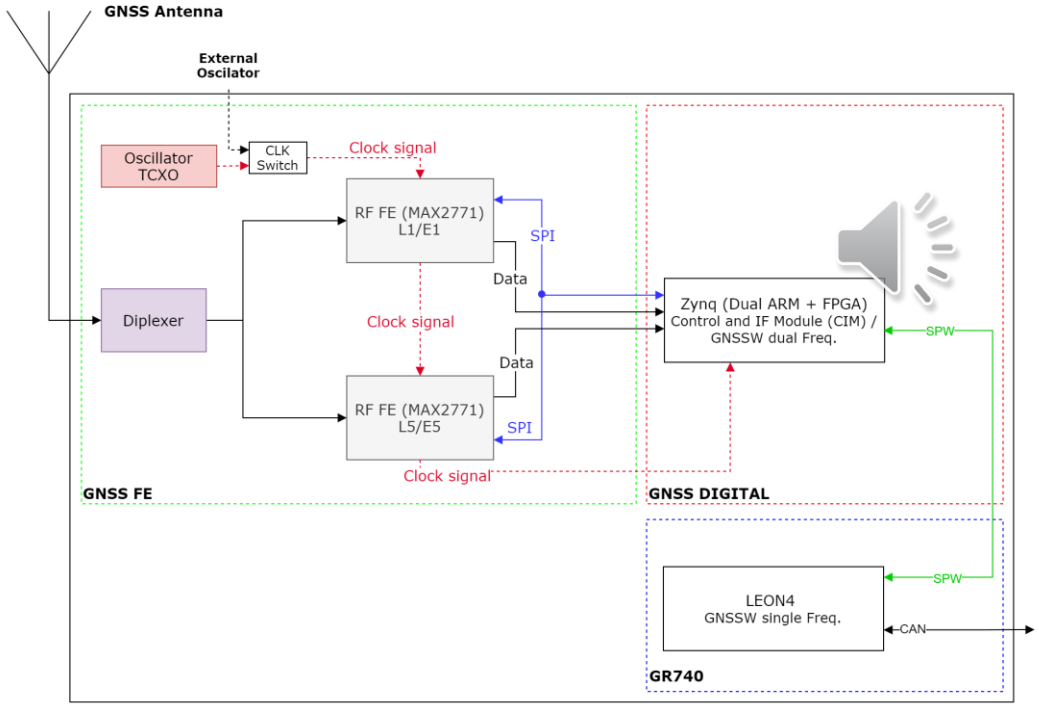


Zynq Based Dual Frequency Receiver



- **GNSS FE** developed by **CBK** for raw data acquisition and **Space Inventor Z7000-P3** processor used for signal processing
- Under **RTEMS 5 OS**
- **FPGA** of the Processor board used for the raw data packetizing
- At least **40 single frequency** and **8 dual frequency channels** (8L1+8L5)
- Acquisition of L5/E5 signals is made by L1/E1 measurements aiding
- **LSQ** + **EKF with Iono-free** Navigation
- Communication with GR740 through SpW
- Can work as **standalone solution**:
  - 2 boards, 1/3 Unit, 300 gram of weight, 5 Watt of nominal power consumption
  - Support UART / CAN / SpW
  - JTAG for debug
  - Additional connector with output of the Clock, FE data and SPI communication port

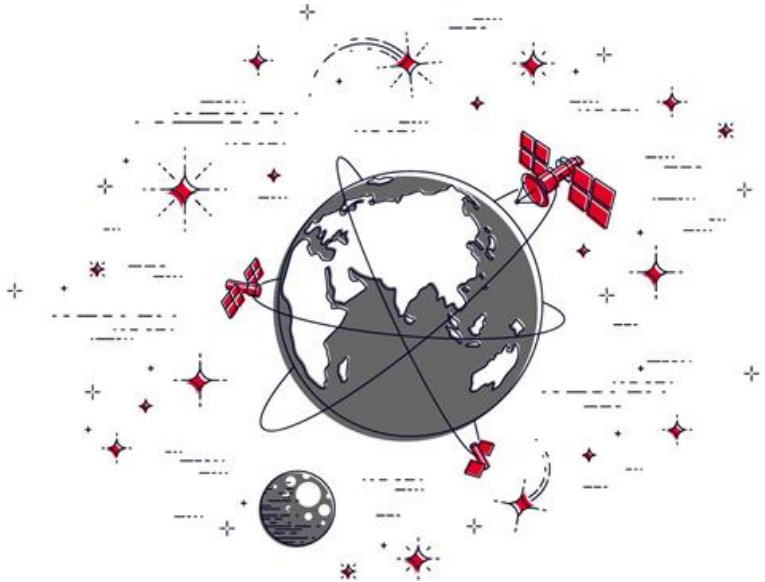
LEON4 Based Single Frequency Receiver



- **Cobham Gaisler GR740 LEON4** processor used for signal processing (only 3 cores used)
- Under **RTEMS 5 OS**
- **FPGA** of the Zynq board used for the raw data packetizing and sending them to LEON4 through SpW
- At least **9 single frequency channels**
- **LSQ + EKF Navigation**
- Communication with Payload Computer of GOMX-5 through CAN

Performance

Type	Software Defined Radio GNSS Receiver
Communication	- CAN / SpW - PUS / CSP
Supported bands	- GPS L1 / Galileo E1 - GPS L5 / Galileo E5a
Platforms	- Z7000-P3 Zynq 7030 (Dual core ARM) - GR740 (Quad Core LEON4)
Performance	- 10 m and 0.1 m/s in LSQ single frequency mode - 10 m and 0.05 m/s in EKF single frequency mode - 2 m and 0.05 m/s in IONO free EKF mode (dual frequency)
Tracking	- 40 channels (single frequency) - 8x2 channels (dual frequency) - Sensitivity of 28 dBHz
Acquisition	- 8 min TTFF in cold start - 2.5 min TTFF in warm start - Sensitivity of 40 dBHz in frequency domain - Sensitivity of 28 dBHz in time domain
Applications	- LEO Satellites : 400 to 1500 km - Microlaunchers
Navigation modes	- Least Square - Kalman Filter - IONO free (with Kalman Filter)
Outputs	- 1-10 Hz - PVT - Raw Measurements: Pseudoranges, Dopplers, Carrier Phases - Tracking outputs: Correlation IQ, Code and Phase errors - Processing status - Almanacs / Ephemerides



The BRAVE board

Eduardo.Bezerra@spacelab.ufsc.br

Universidade Federal de Santa Catarina, Brazil

Florianópolis, 11 November 2021.

Federal University of Santa Catarina

- Started in 1960
- Main Campus in Florianopolis
- 80 undergraduate courses
- 35,000 students

Florianopolis


NanoXplore
NG-LARGE
0919
077

NanoXplore

NG medium

- 34K LUTs / 3Mb RAM
- 112 DSPs
- 16x SpW & DDR2 PHY
- No HSSL
- µP: Soft IP (Leon3 @ 35MHz)

NG large

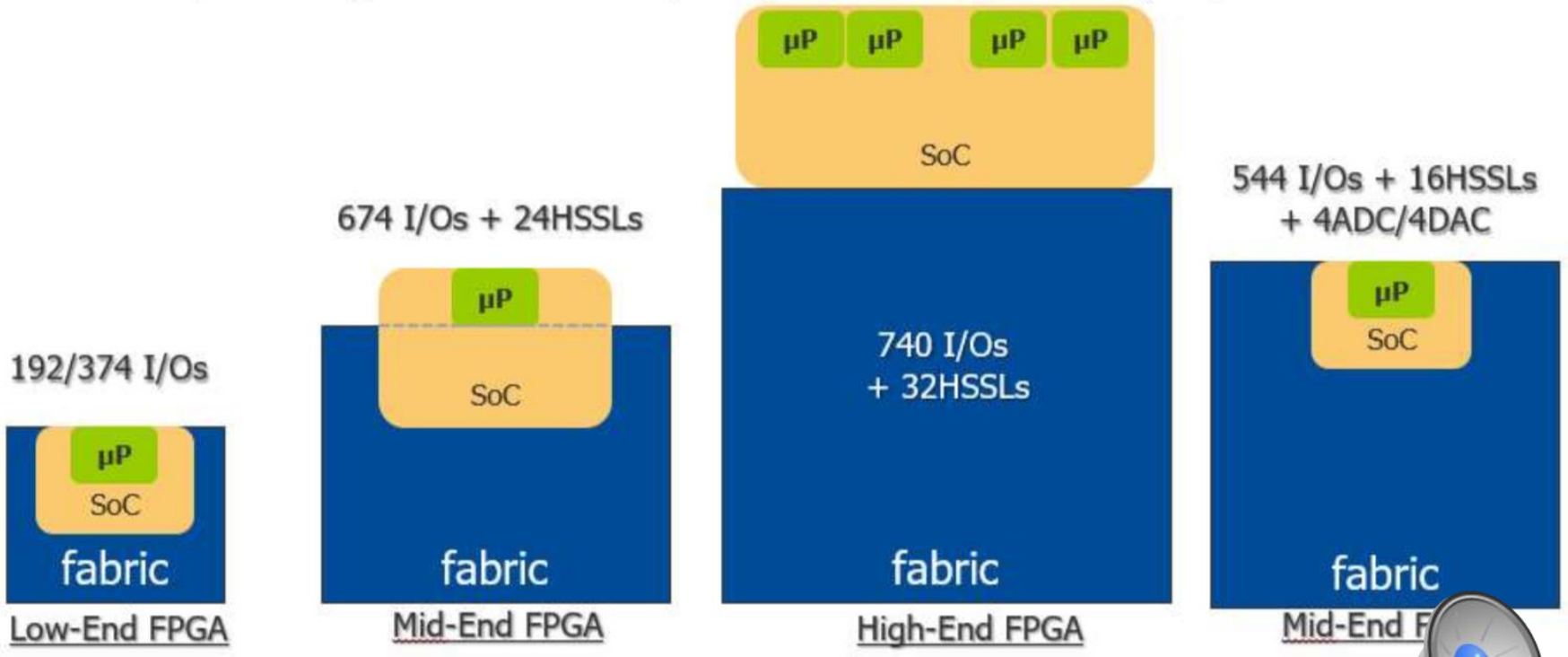
- 137K LUTs / 10Mb RAM
- 384 DSPs
- 20x SpW & DDR2 PHY
- 24x HSSL-6,25Gbps
- µP : Hard IP (ARM-R5 @ 200 MHz)

NG ultra

- 537K LUTs / 32Mb RAM
- 1344 DSPs
- 20x SpW & DDR2/3 PHY
- 32x HSSL-12,50Gbps
- µP : Hard SoC / DAHLIA (4x ARM-R52 @ 600 MHz)

NG ultra300

- 290K LUTs / 22Mb RAM
- 896 DSPs
- 20x SpW & DDR2/3 PHY
- 16x HSSL-12,50Gbps
- 4x ADC & DAC
- µP : Soft IP



BRAVE board

Goal:
- In-orbit Validation (IoV) of BRAVE FPGA;

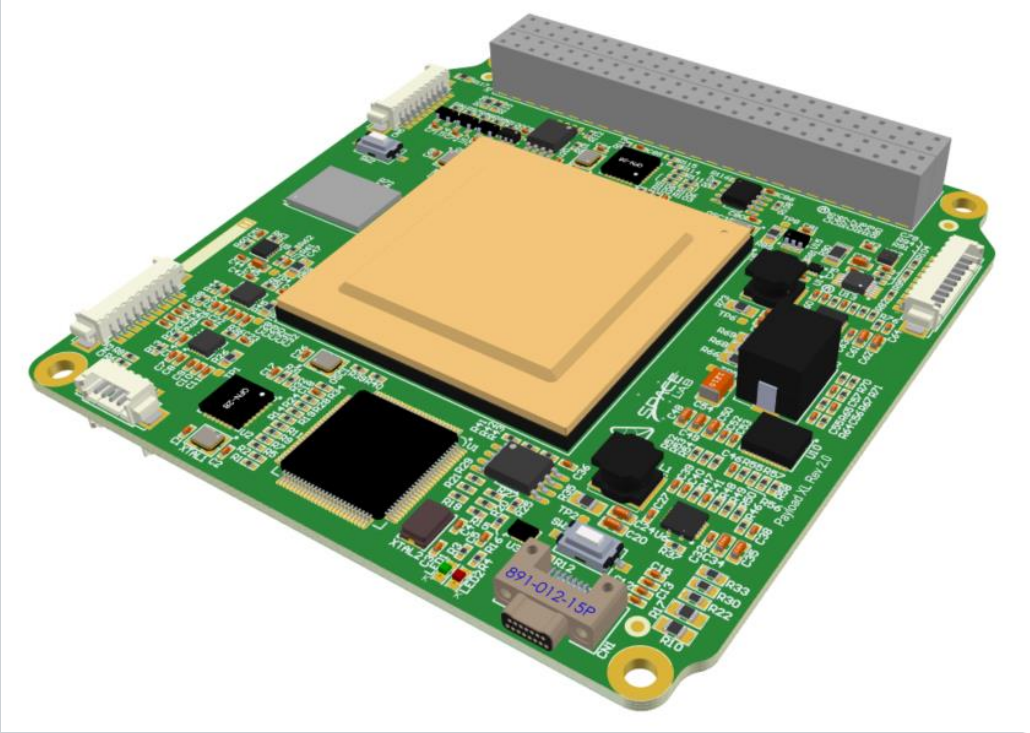
Application:
- In-orbit Reconfiguration strategy for FPGAs.

Design achievements:
- Technical skills: high-speed PCB design; advanced multilayer PCB; mitigation of electromagnetic effects on PCBs;

BRAVE board

Board specification:

- Radiation-hardened FPGA - 625 pins BGA package;
- MSP430 MCU;
- 2 x FLASH memories for the additional storage;
- 5 power converters;
- 9 layers PCB with impedance control.

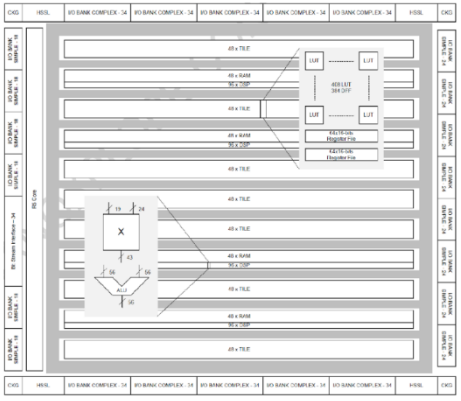


BRAVE BOARD ARCHITECTURE

NG-Large Device

Available resources:

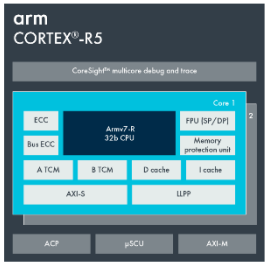
- Logic: 137088 LUT4 + 129024 DFFs + 32256 CY chains
- Memories: 192 BRAM blocks of 48kb (= 9216kb), going down 36kb with EDAC activated + 672 Register Files of 168*64bits also protected by EDAC
- DSP: The NG-Large has 384 DSP blocks which can be cascaded
- SpaceWire: The NG-Large has 1 SpW CODEC and 20 PHYs
- DDR2: The NG-Large has 20 DDR2 PHYs
- 24 SERDES operating from 0,70 to 6,25Gbps allowing to comply to many protocols
- Hard IP Processor type ARM Cortex-R5
- It has 32 clock domains splited within 4 clock generators (CKG) including their own PPL.



ARM Cortex-R5 (built-in)

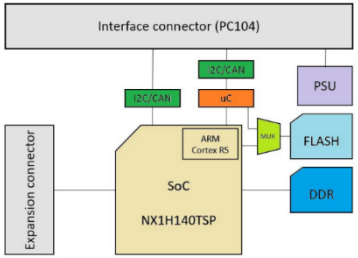
The processor is part of the BRAVE architecture as a hard-core and peripherals should be instantiated as soft-cores connected to the AMBA bus (AXI or AHB).

It is responsible for peripherals and interfaces management. Also, in order to perform the FPGA in-orbit reconfiguration, it handles all the incoming ground bitstream pakages, the storage and management of bitstreams, the actual reconfiguration process, and downlink status packages.



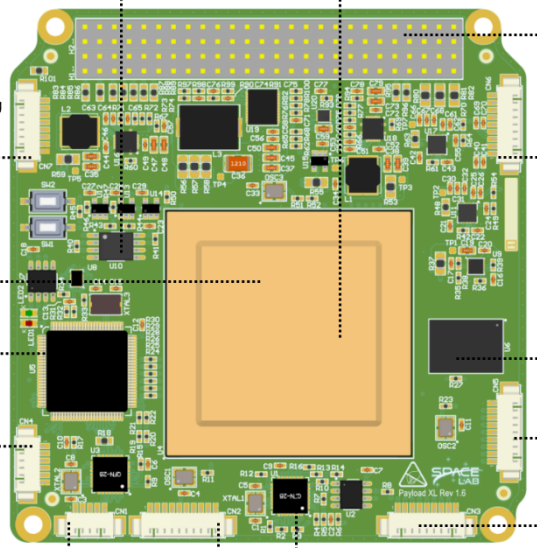
Flash Memory

This Flash memory is dedicated to store bitstreams. It has capacity for two bitstreams, one for a fallback mechanism and the other received from the ground segment.



PC-104 Interface

The PC-104 has several power, control and communication interfaces. The most important are the 5V input, the power enable and the CAN/I2C buses.



FPGA JTAG

Interface used during debug for the FPGA device programming.

SpaceWire Interface

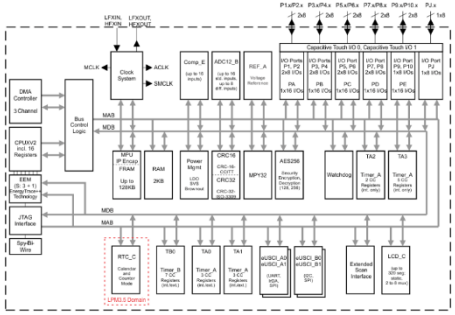
This interface is dedicated for communication with other modules. It is connected to a controller/transceiver in the FPGA device.

DDR2 SDRAM Memory (FPGA)

The DDR2 SDRAM Memory has direct access to the BRAVE FPGA, which has a DDR controller that might be connected to a AXI bus. Using the bus, it is possible to access the memory through the ARM processor or any other AXI master device.

Auxiliary Microntroller

This microcontroller (MSP430-FR6989) is an auxiliary processor to support the in-orbit reconfiguration. It is not required to the Payload-XL operation, but increases the overall reliability, since it can operates in case of a critical failure (as a fallback recovery).



uC UART

Interface used during debug for the uC logger.

FPGA GPIOs

This interface provides external access to the FPGA GPIOs, which can be controlled by any device inside the device (ARM or any softcore).

FPGA UART

Interface used during debug for the FPGA systems logger or external communications, depending on the application.

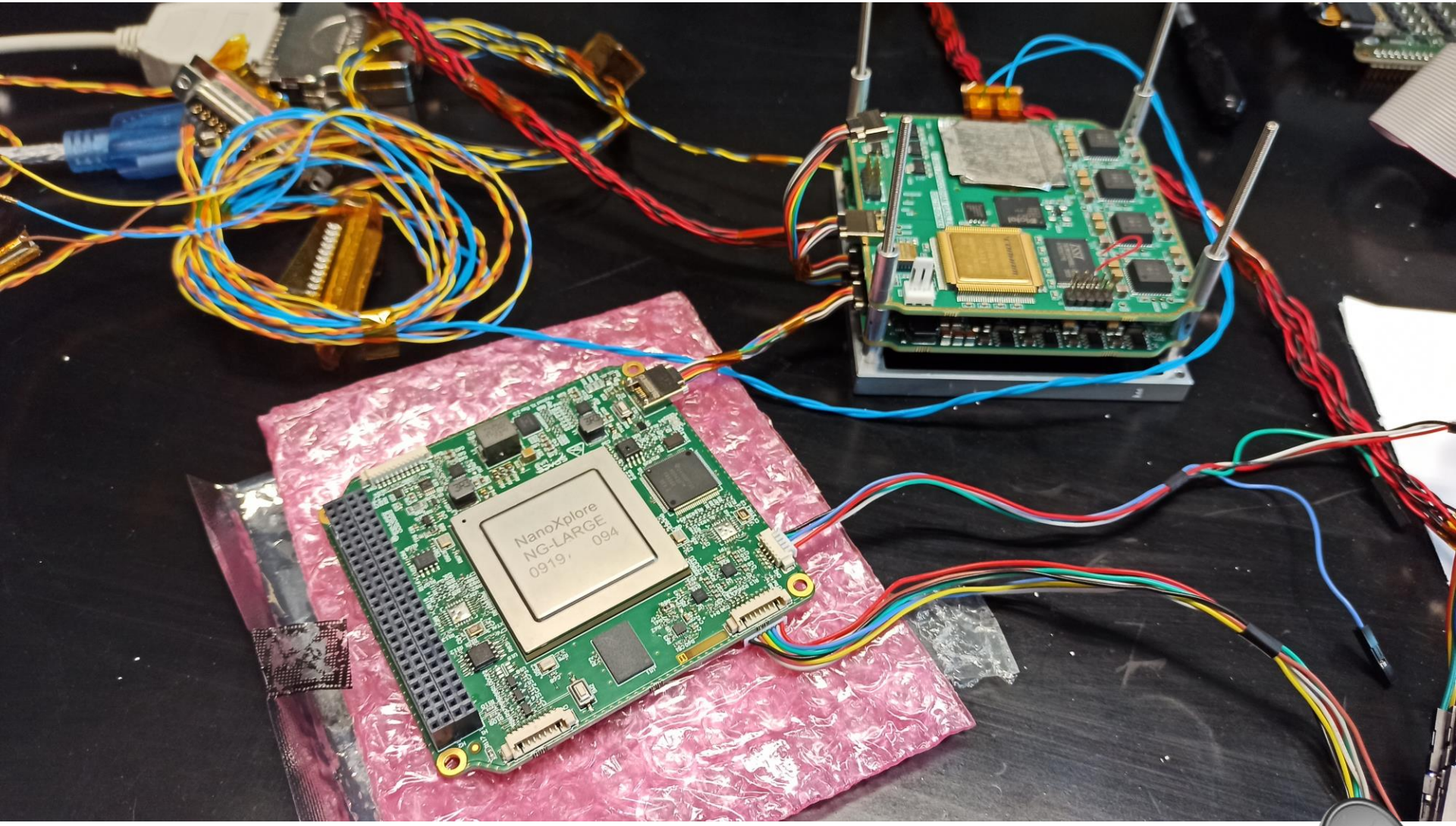
ARM JTAG

Interface used during debug for the ARM core programming.

SPI-CAN Interface (FPGA)

The SPI-CAN interface is used to convert a SPI protocol into a CAN node. The interface is connected to the PC-104 bus, allowing communication with other modules.

BRAVE BOARD



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