

Abeto Framework: a Solution for Heterogeneous IP management

The European Space Agency (ESA) provides a portfolio of soft IP cores for space missions, described in VHDL, which are used in several System-on-Chip (SoC) developments performed through various ESA contracts and other development programmes. This portfolio continues growing with more reusable cores, which can be used as building blocks inside larger designs, saving development costs and time. Each IP core provides its own database structure, including all the necessary files to re-use the IP. However, each IP core is the result from different activities and as a consequence, each one follows a different structure and implementation flow, deriving in a heterogeneous IP core database.

The re-use aspect implies that there is a know-how transfer from IP designers to users. This means that designs are required to be not only functional, but also understandable and manageable by users. However, there has been historically a lack of standardization in the way that IP core designs and their complementary elements are coded, packaged and documented. This makes IP re-usability not straightforward, having each IP core a unique learning curve and usually leading to extra efforts adding Electronic Design Automation (EDA) tool support for each design. Some solutions have been proposed to facilitate the exchange and re-use of IP cores, such as IP-XACT or FuseSoC. However, their application is not general yet.

Another key aspect is the right choice of building blocks to incorporate in a large design. In order to make the best IP core – chip technology choice, users want to know the area and resources these cores take, their operating speed and their power consumption depending on the target implementation device. Such information is essential for potential users to adequately evaluate if an IP core meets their requirements and constraints. However, this information is not always available in the IP cores documentation and, in the cases it is, technology mapping results tend to become obsolete along time as new technologies emerge. From the potential users' point of view, it is crucial to have access to up-to-date implementation results, or the capability of generating them.

This work presents Abeto (Automated benchmarking Tool), a command line tool intended to integrate heterogeneous groups of IP cores and operate with them in a unified manner. This tool has been conceived for the ESA IP cores portfolio, although it can handle any other IP core database. In order to do so, Abeto requires from every IP core some side information about its file structure and how to operate with the IP. Different stages of the IP workflow, from IP configuration to implementation, can be configured, launched and automated from Abeto in a transparent way from the user point of view. To demonstrate this extent, Abeto has been used to obtain updated implementation results for a subset of the IP cores from the ESA IP portfolio for several FPGA technologies, including the novel space-grade BRAVE FPGA family from NanoXplore. This project has been supported by ESA through the project "ESA IP cores automated benchmarking" (ESA contract 4000127452/19/NL/GLC/vr).