ProUST-FE platform

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EGSE Presentation, 12.12.2013,
A. Fuchs, Siemens CVC Space

Personal background

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- Fuchs Alfred (substituting Peter Juzl)

- 6 years at Siemens Space, Product Line Manager
- 20+ years HW and FPGA-design @ Siemens (telecom, medical, …)

Our EGSE portfolio

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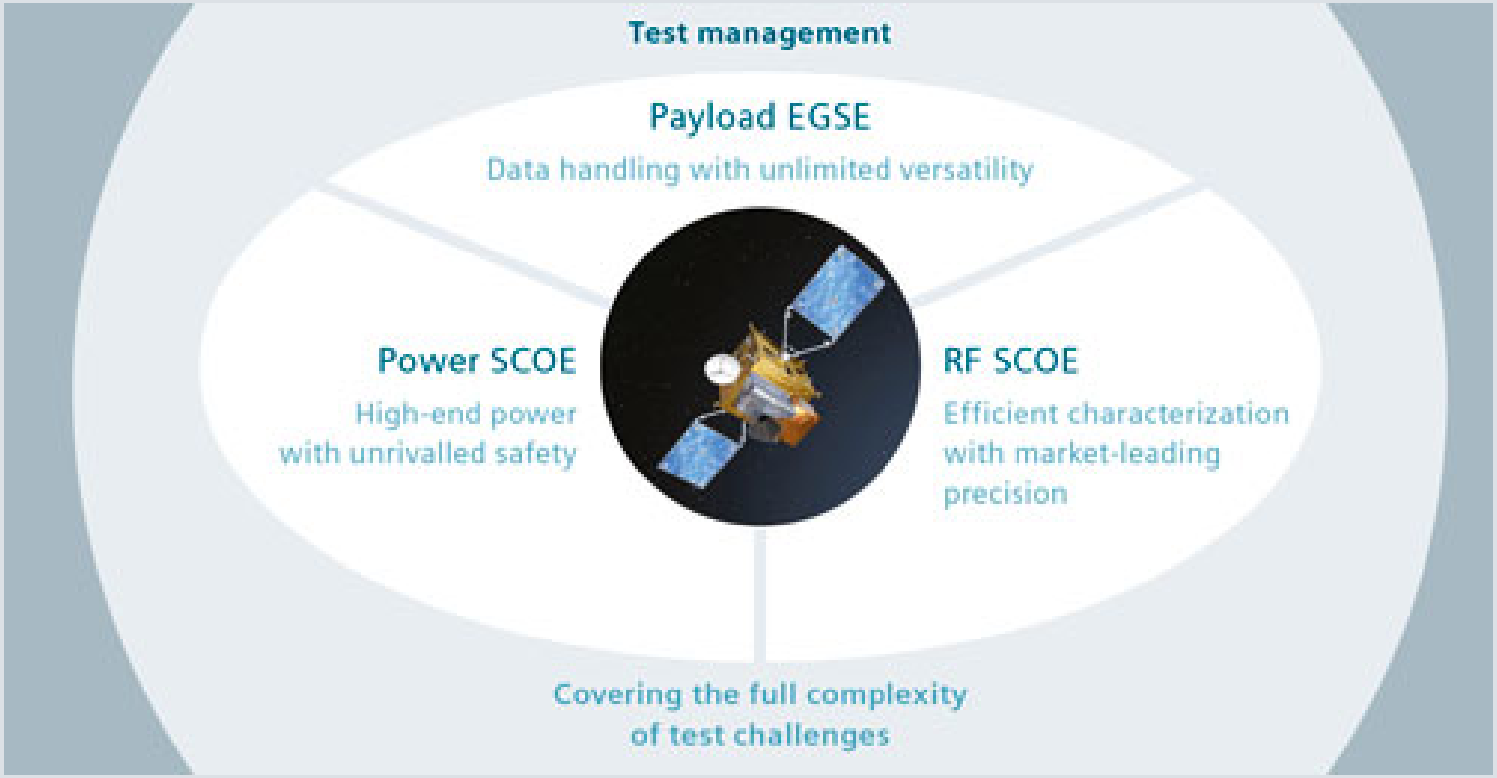
- 3 sectors



Interface Requirements

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- RF-SCOE
  - 2 LVDS / SpW
- Power SCOE
  - 10 SHP
  - 40 Pyros
  - 10 Analog inputs
  - 5 Analog outputs
  - 20 RSA
  - 10 Thermistor sim
- Instrument EGSE
  - 4 MIL1553
  - 8 SpW
  - 200 SHP/EHP/Valves
  - 40 Pyros
  - 100 Analog inputs
  - 50 Analog outputs
  - 200 RSA
  - 50 Thermistor sim

Other Requirements

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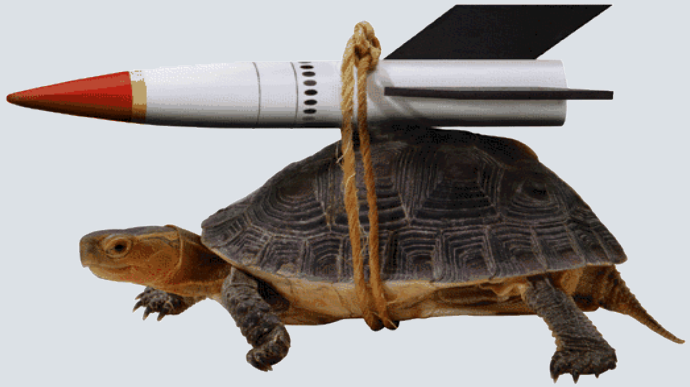
- Power
  - 30V 100A
  - 100V 30A
- Performance
  - GB/s throughput
  - µs latency
- Safety
  - OVP, OCP
  - Fault voltage emission/tolerance
- (Security)
- (High Availability)



COTS platform example

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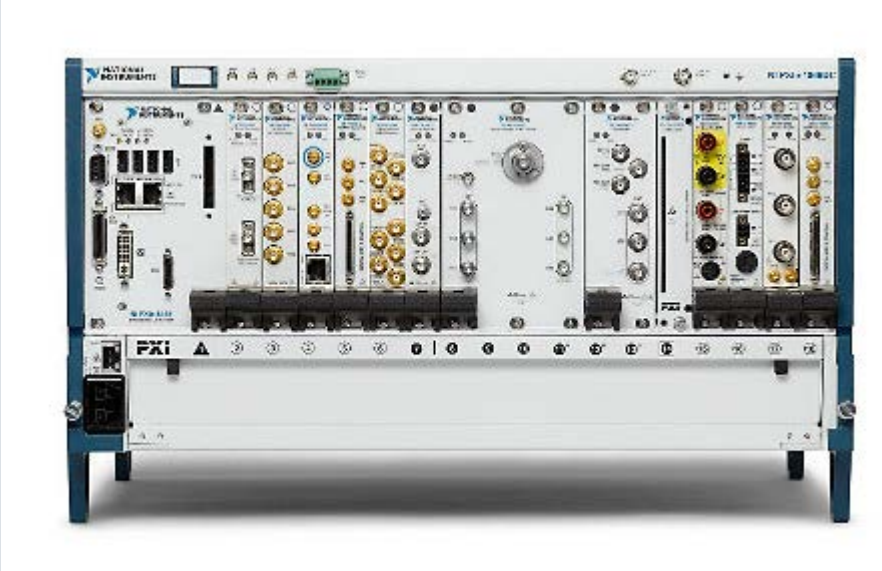
- NI PXIe
  - Industry standard, modular I/O

- Power: NA
- Performance: 3-12GB/s,
- Safety: NA
- Rf: Partly

- Still proprietary needs



ProUST SLP

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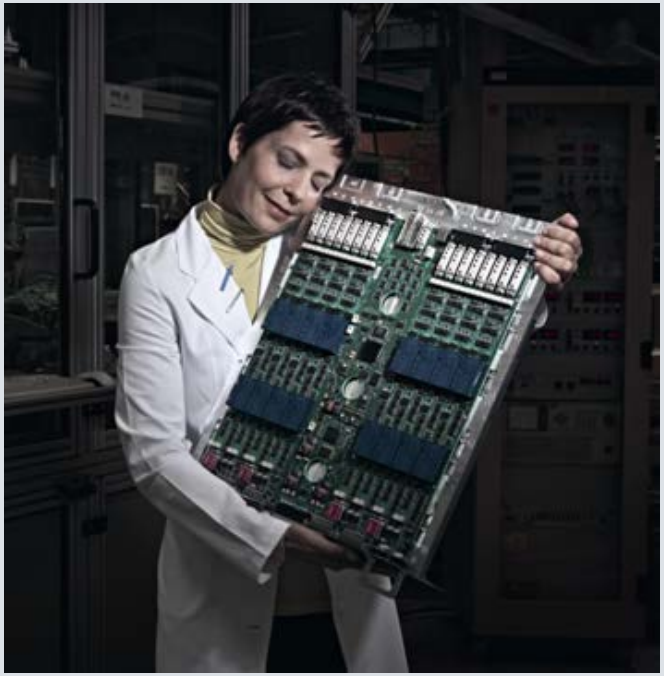
- ProUST – Protection Unit for Satellite Testing
- 8 reconfigurable power channels for SAS or battery simulator or ...
- + a bounty of discrete signal I/O
- -> single-rack solution



Make or buy

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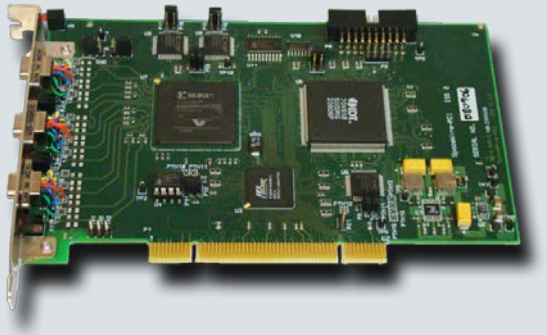
- Discrete I/O: Test/DAQ industry
- MIL-1553: Many suppliers
- SpW: Several suppliers
- Other, future I/O: TBD



- Conclusions:
- Don‘t fight COTS IT
- Maximize I/O-performance with PCIe
- Buy IP-cores

Emphasis

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- Non-functional properties
  - High-density
  - Versatility
  - RT-performance

Platform for engineers

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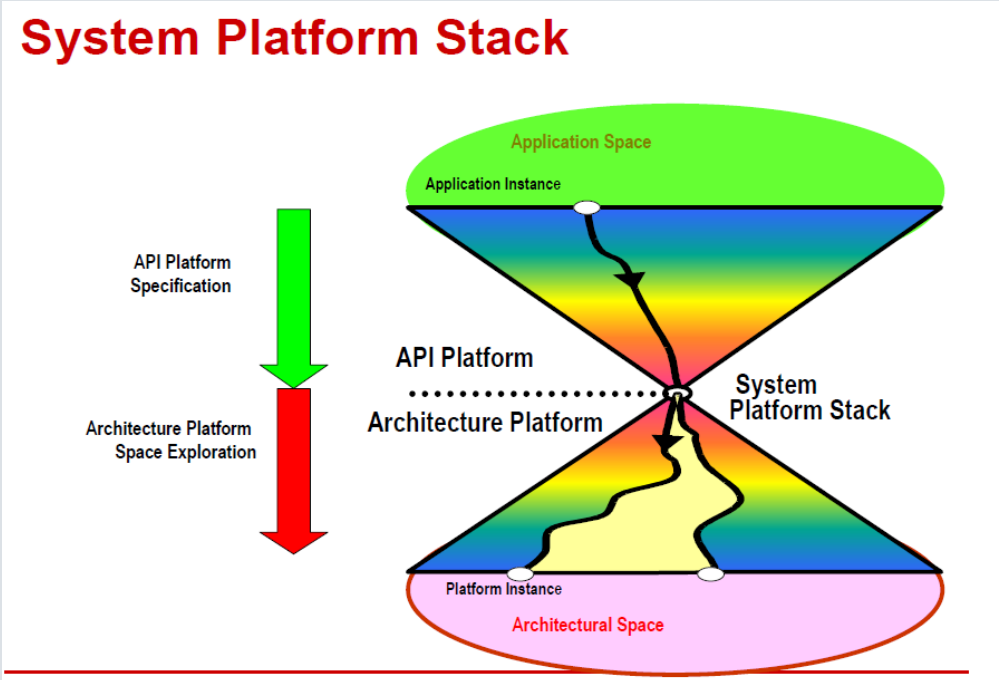
- E.g. VW car platform strategy
- Satellite „platform“
- „Platform EGSE“

- Alberto Sangiovalli-Vincentelly (Berkeley)
  - „ a platform is an abstraction layer in the design flow that facilitates a number of possible refinements into a subsequent abstraction layer (platform) in the design flow. “



Platform FPGAs

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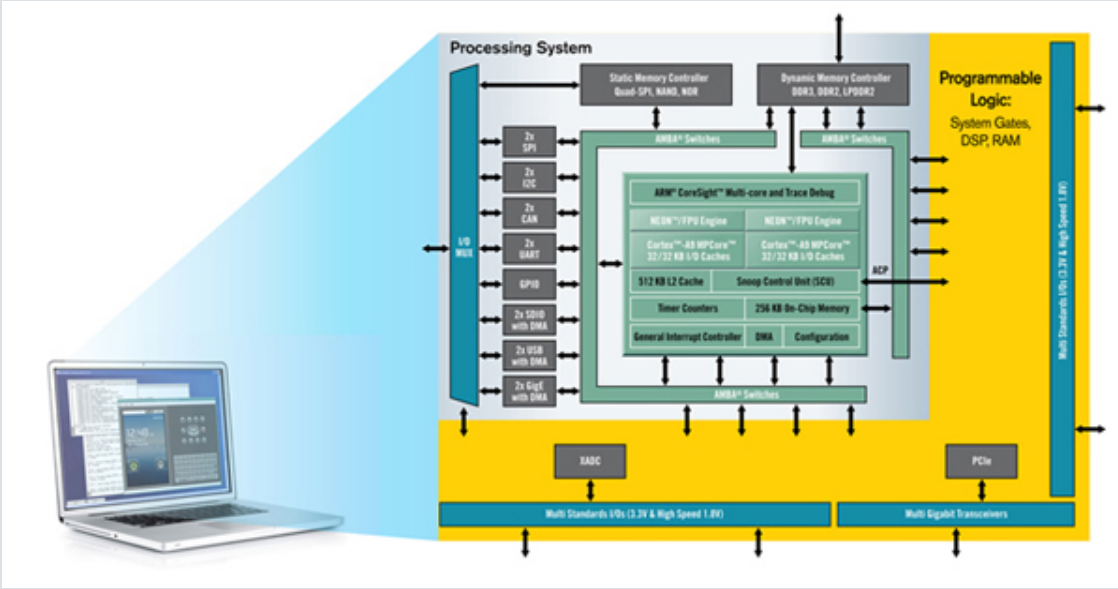
- E.g. „All-programmable“ Xilinx Zynq SOC

- Logic (LUTs)
- Memory
- DSP-ALUs
- Clock management
- High-speed serial I/O (PCIe, ETH, other)
- ADCs

- Embedded system (ARM)
- SW-Ecosystem



FPAAs

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- E.g. Anadigm

- OPAMP-array
- Filter bank
- SAR-ADC

- Typically absorbed into SOCs

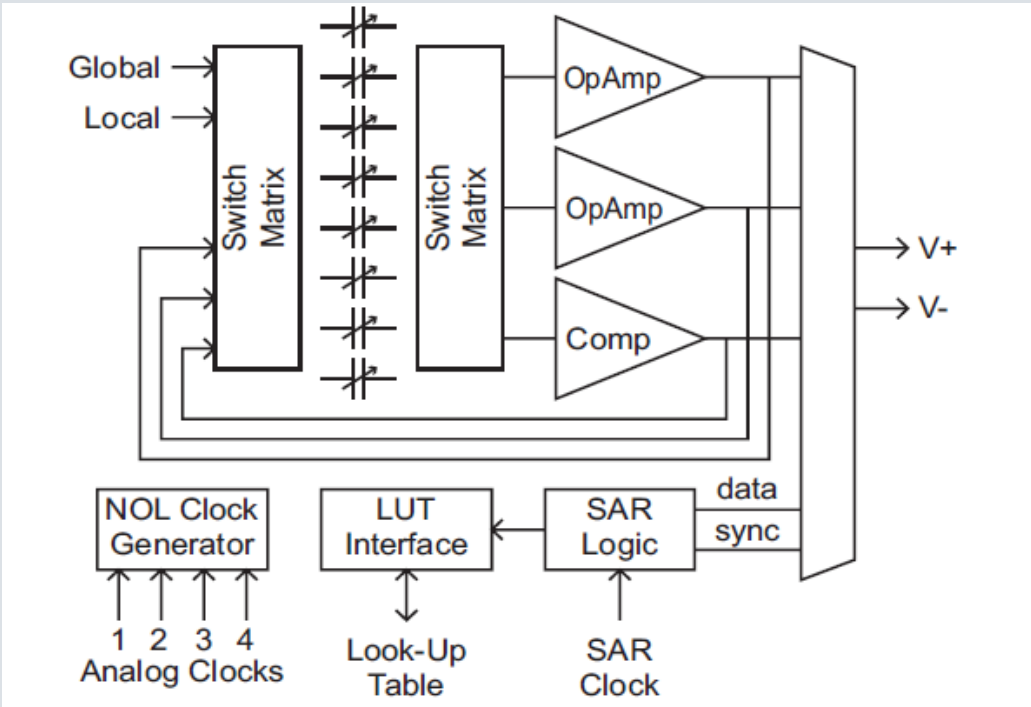
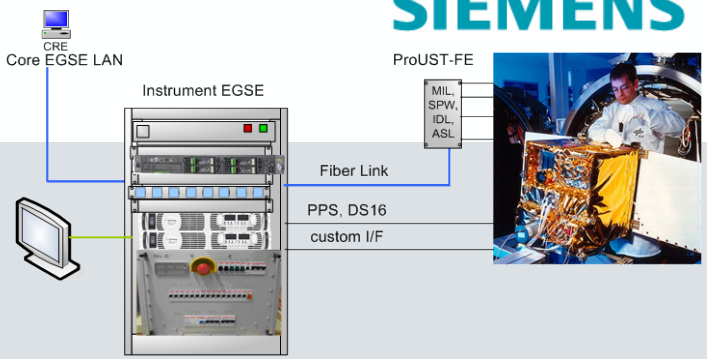
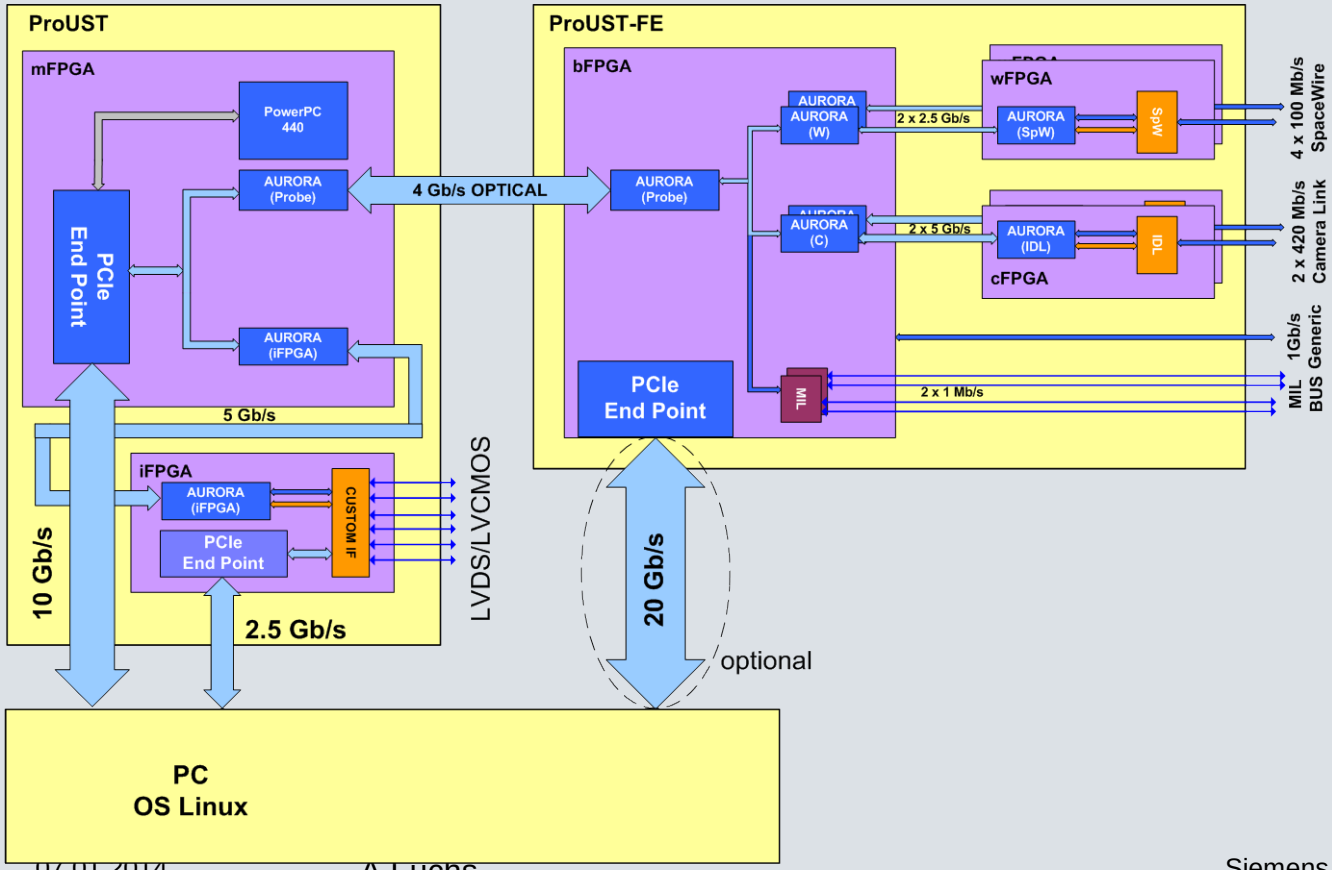


Figure 5 – Overview of a Configurable Analog Block

ProUST-*"Front-end"*



- Common communication architecture
- PCIe-over-cable
- Fiber-optic extension link



ProUST-FE design

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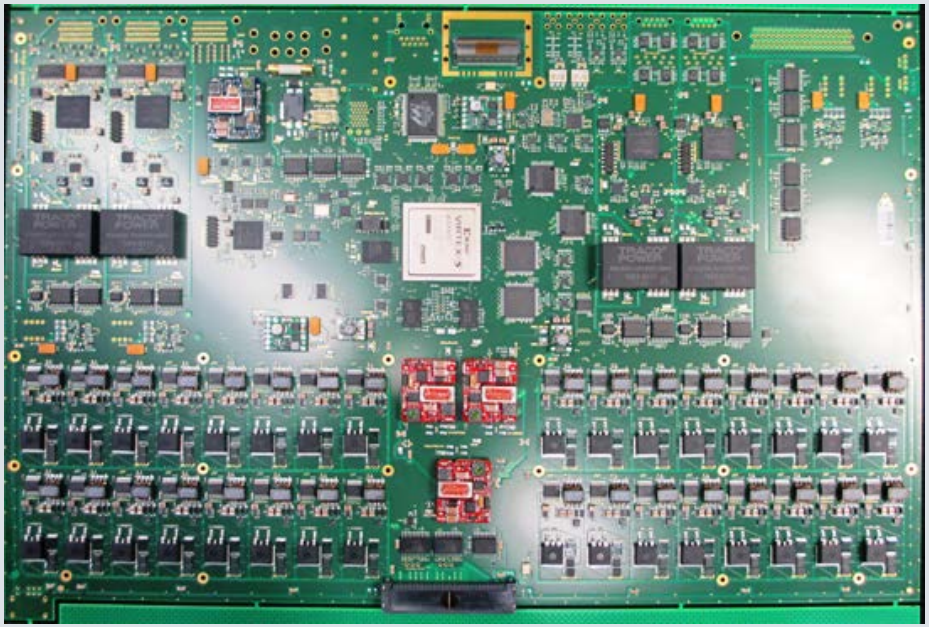
- MIL-1553, SpaceWire, Cameralink,

- + „Pyro“ Front-End platform
- + Fast ADC/QUC

- Focus: Real-Time HITL simulators



ProUST-FE design

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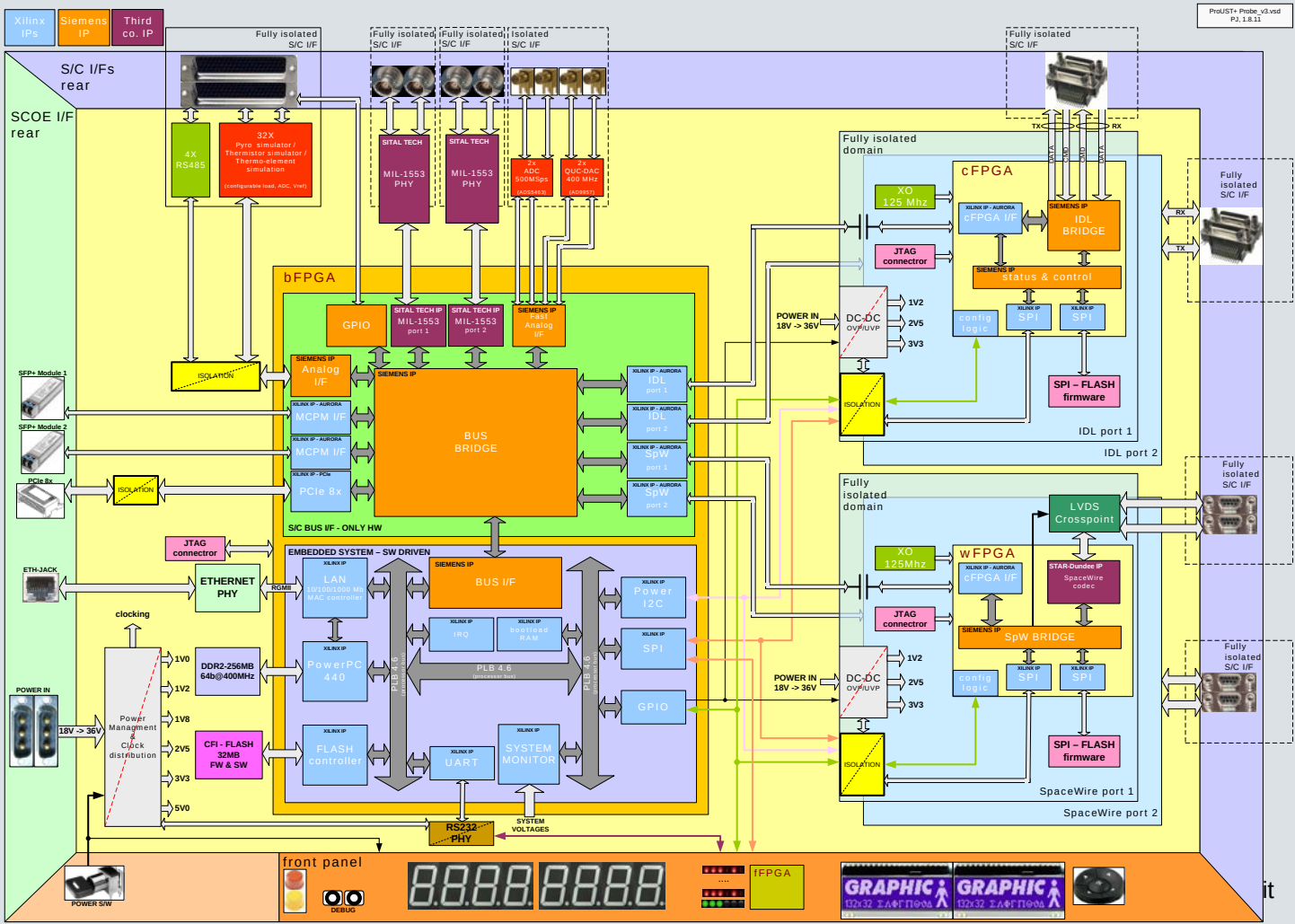
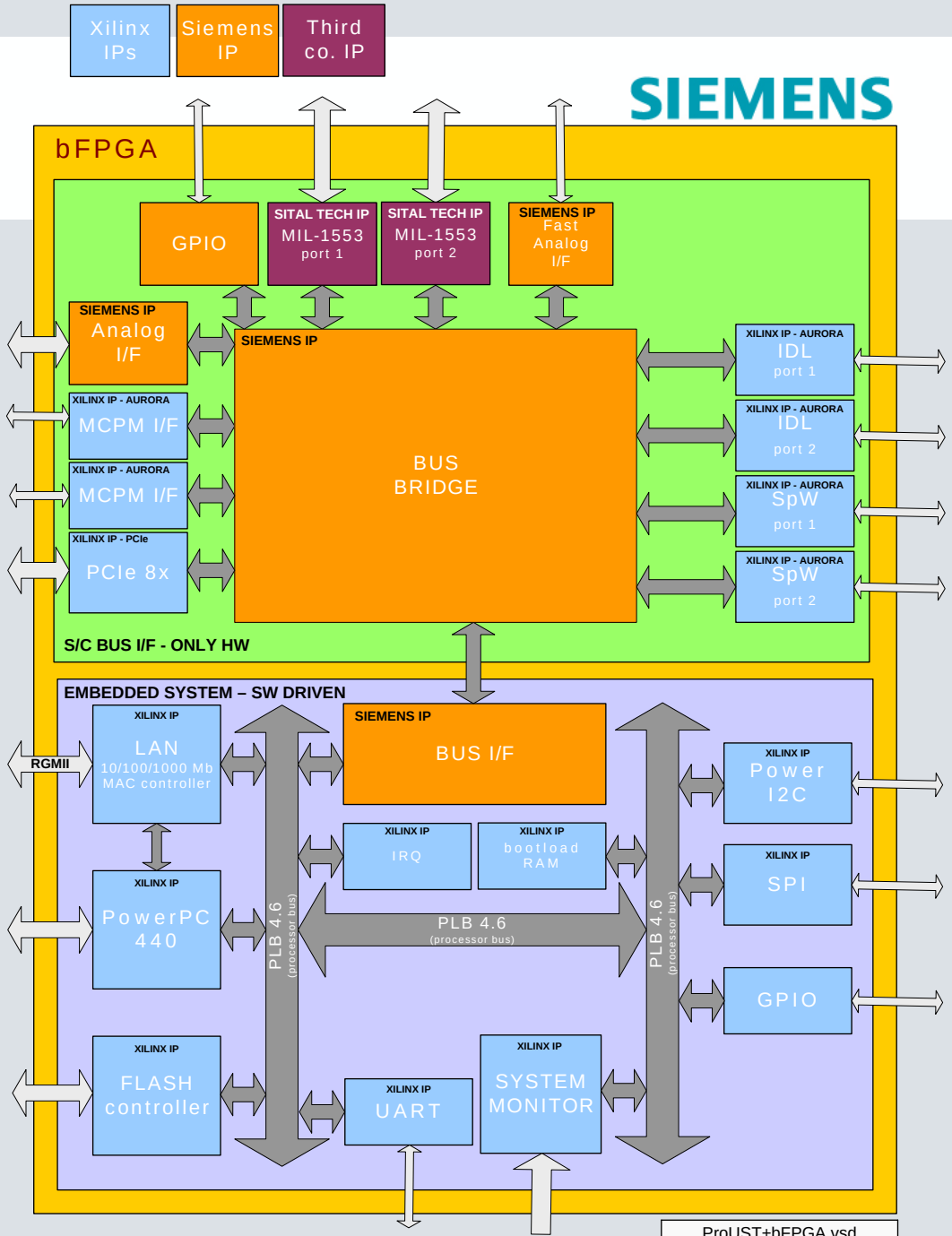
- Multiple FPGA approach with Gigabit links



ProUST-FE ES

- Virtex 5 centered
- Xilkernel
- Lwip-stack



ProUST+bFPGA.vsd
JB, 19.10.2011

ProUST-FE serial interfaces

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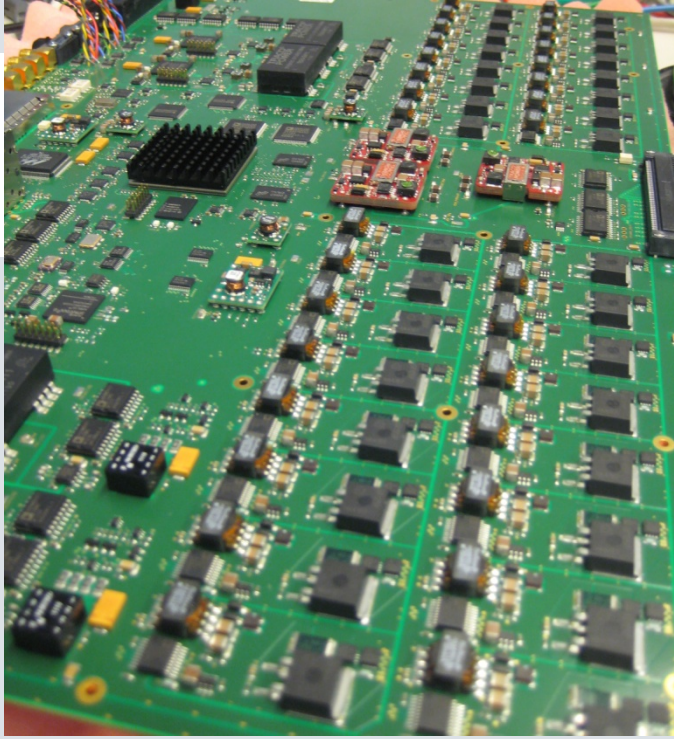
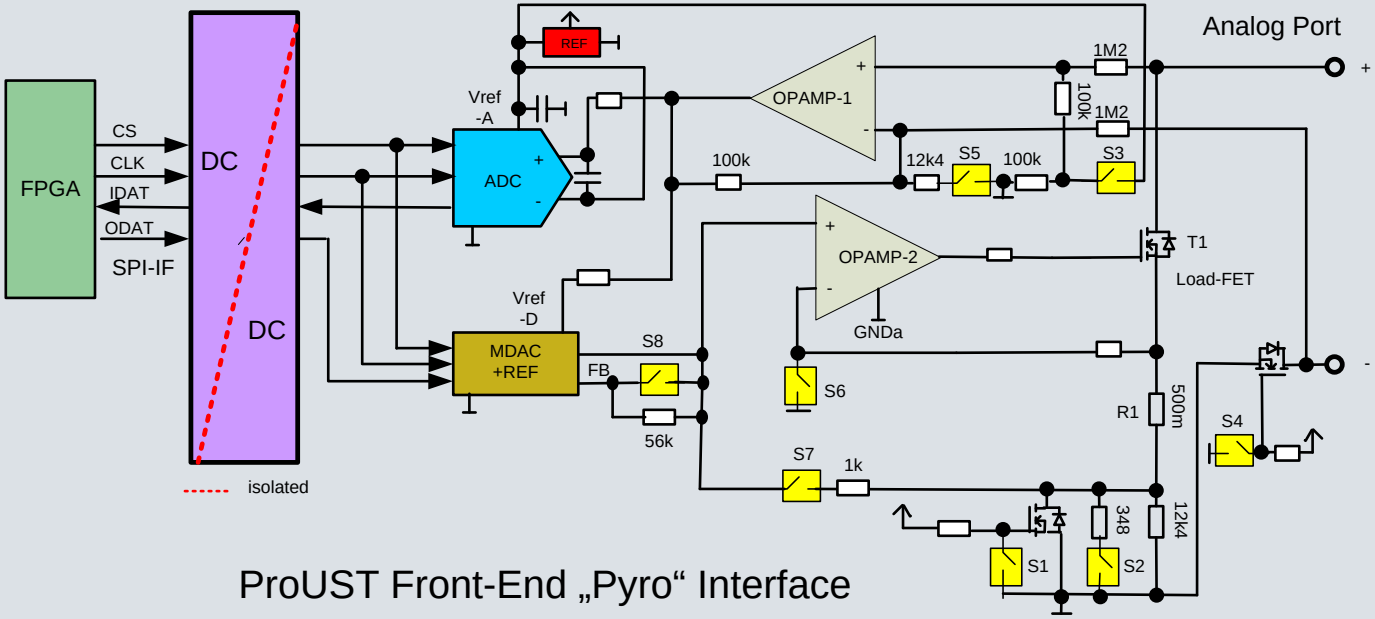
- 2+2 MIL-1553
- 4 SpaceWire
- 2 Cameralink
- 4 RS422
- Many LVDS / TTL / CMOS IOs

ProUST-FE „Pyro“



- 32 Generic, programmable analogue interfaces
  - Individually isolated
- Suitable for digital, analog, power
  - 150kS/s



ProUST Front-End „Pyro“ Interface

ProUST-FE „Pyro“

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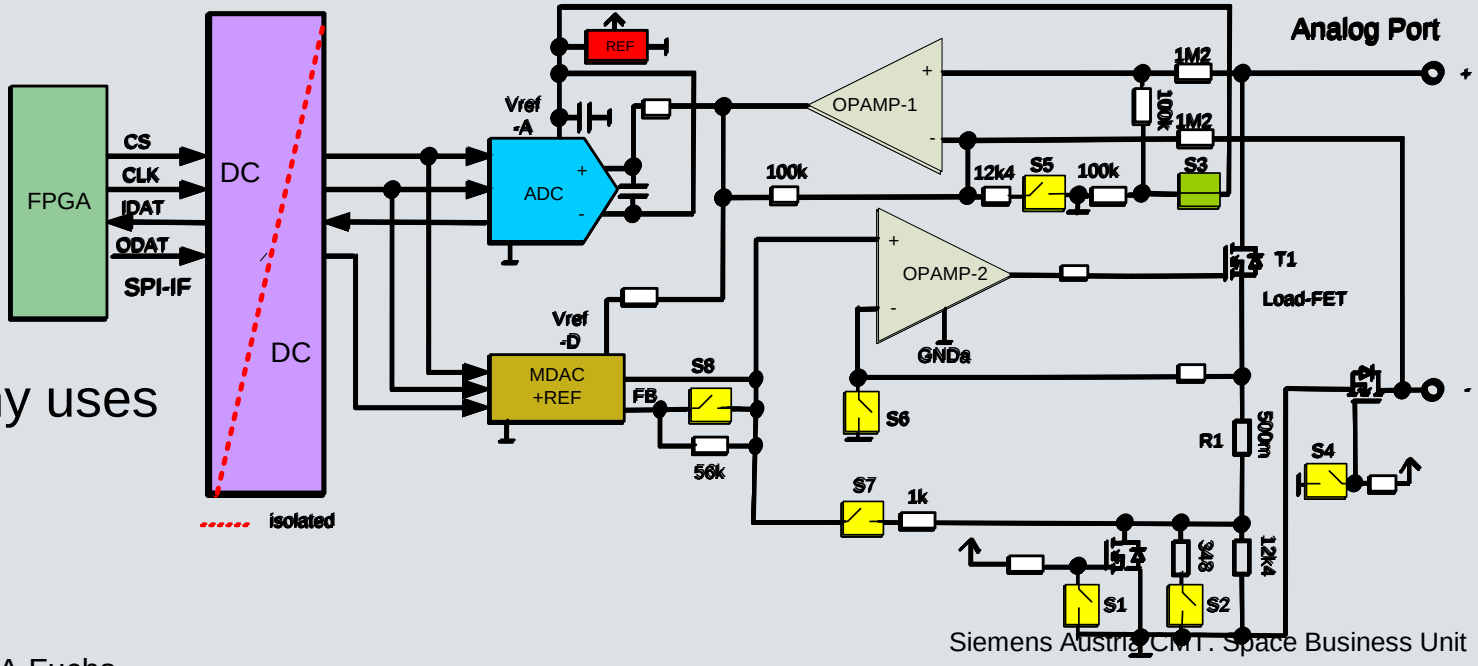
- 10+ programmable functions
  - analog voltage input (AN1/2, ..)
  - analog voltage output (AN2)
  - resistor simulation (Thermistors, Pyro &relay)
  - resistor measurement (&relay)
  - current source (FSS, HPC)
  - current measurement
  - …
- One type, many uses



ProUST-FE PQE

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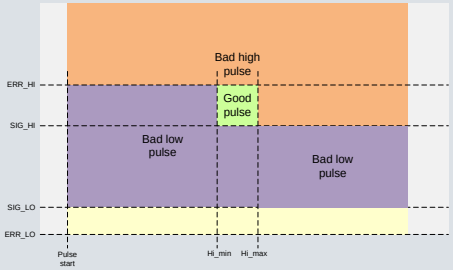
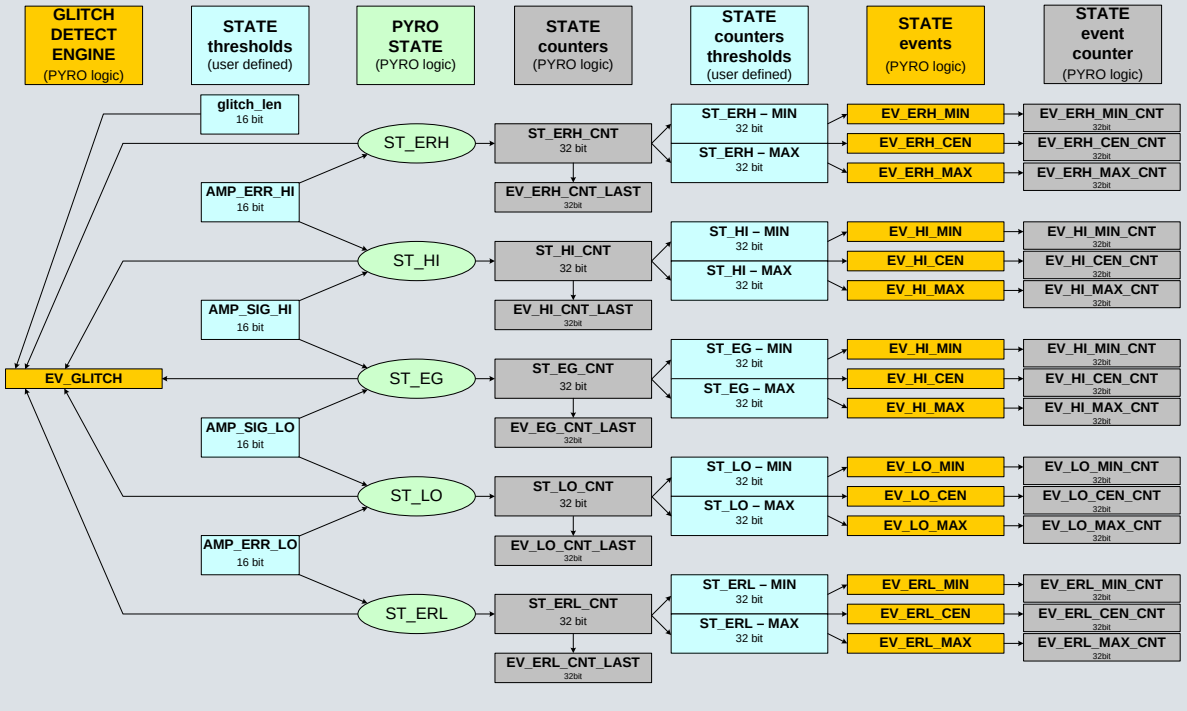
- Complex real-time pulse qualification engine for each interface



PYRO – register structure



ProUST+ bFPGA_v1.vsd
Peter Jüzl, 28.5.2012

Software

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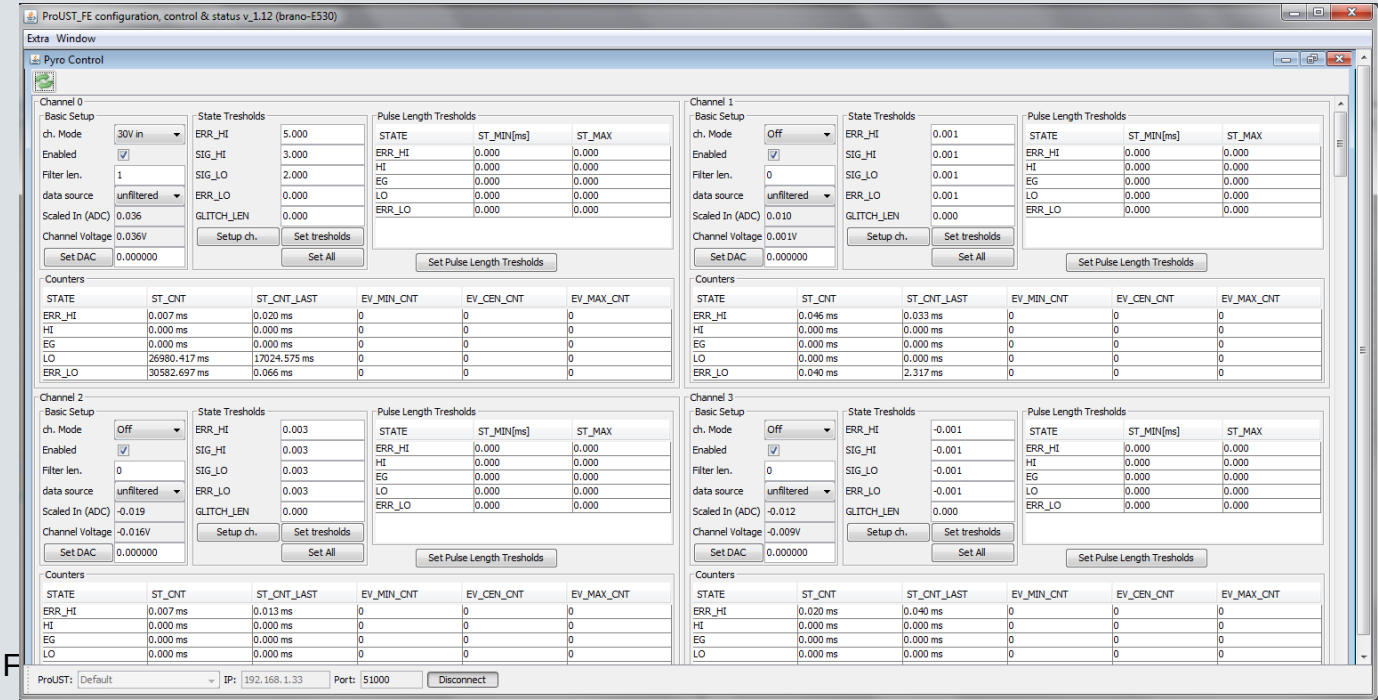
- Universal driver architecture
  - function and access is defined via configuration file
    - abstracts used device and port (P / P-FE)
    - abstracts used communication (LAN, PCIe)
    - abstracts access method (SCPI vs register-based)

- Java applications for simple interactive use

- CCS integration
  - coming



The pains of platform design

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- Wishes are ∞
- Platform is complex
  - Tedious debugging
  - Configuration trade-offs subtle
- Platform must be optimized
  - PCB layout tricky (Xtalk)
  - Performance tuning across hierarchy

Model-based verification

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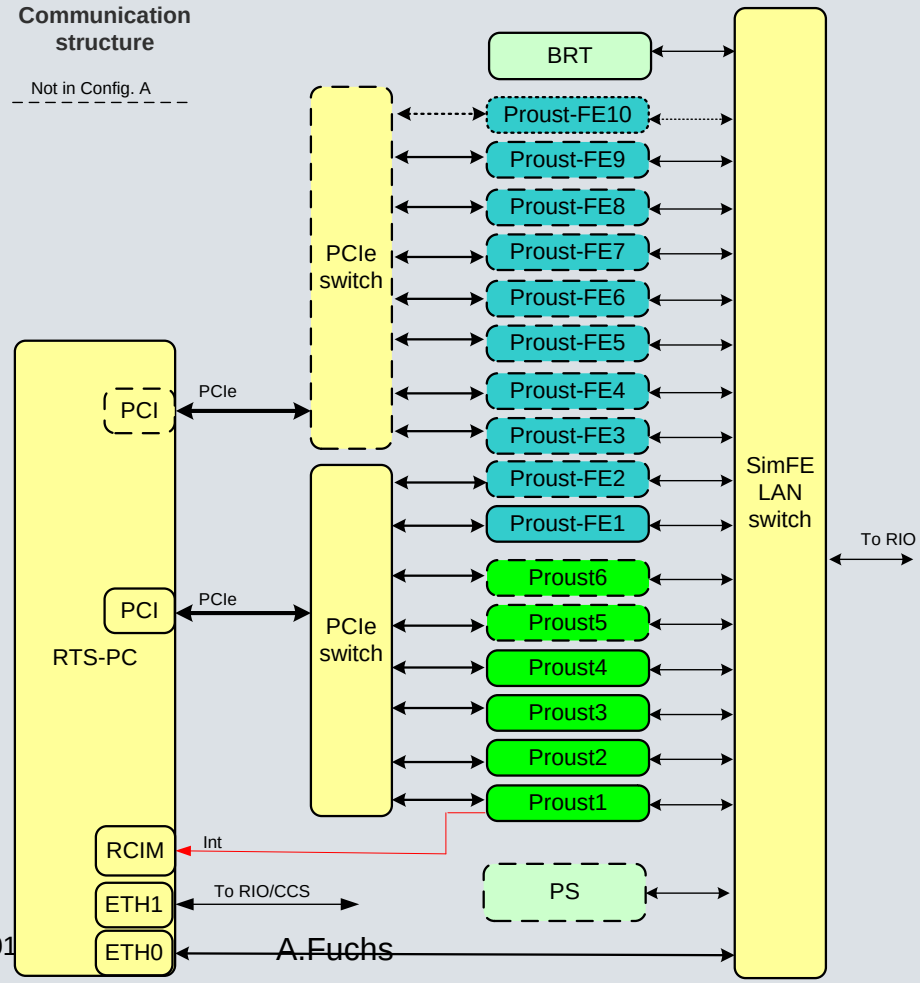
- Solar Orbiter OBC testbench
  - 700+ interfaces
  - 16 ms simulation cycle



Mission experiences

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- S5 Precursor „TROPOMI“ Instrument-EGSE
  - Partly needed fallback
- SOLO PWR SCOE
  - More „Pyro“ current capability requested
- SOLO SIMFE
- Display modes added, calibration refined,
  - Don‘t exaggerate density …
- GFO PWR
  - Event-Trigger-Action feature added
- MTG DHS
  - MIL functionality enhanced (EI, mRT)
  - Lack of RS422 IFs
- MTG PDD
  - SpW/LVDS switch added
- Exomars
  - Bad fit, small EGSEs, CAN-bus, …

More features

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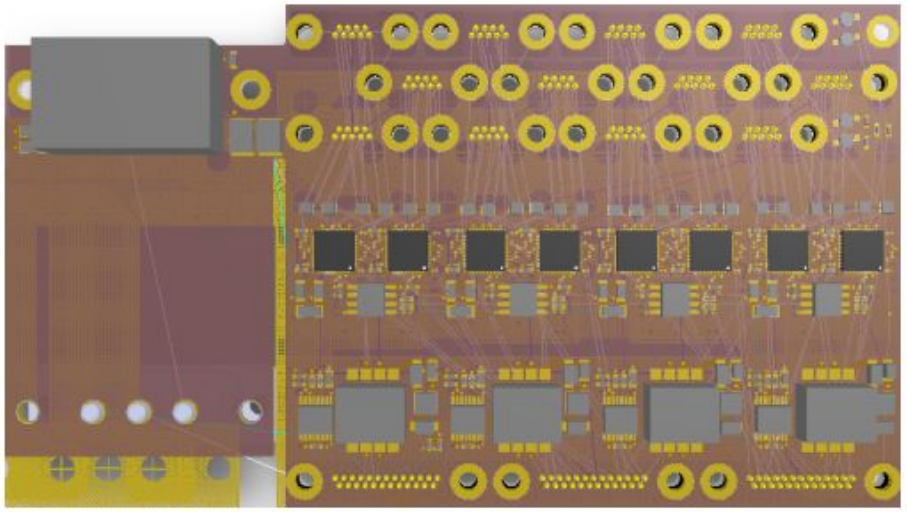
- UARTs added
- ISD/OSD added

- SpW-crossconnect added
  - 4 + 4x3 ports
  - With Equalizer for added cable length

- Timestamp synchronisation (IRIG) added



Lessons learned

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- Dedicated HW effort can help SW
  - Discrete I/O times : 0.4µs write, 1.8µs read, low jitter
- IP-cores may not be the best solution for test equipent
  - Quality ok, but details missing e.g. error insertion
- PCIe-over-cable is a small market
  - Substitute with FO-net

Surprising benefits

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- Good self-test capability

- Trivial spare policy,
- Low risk of obsolescence

- Easy post-delivery changes
  - Can procure EGSE before S/C settled

  „Please one more“ proves attractiveness of versatility

As Marx said …

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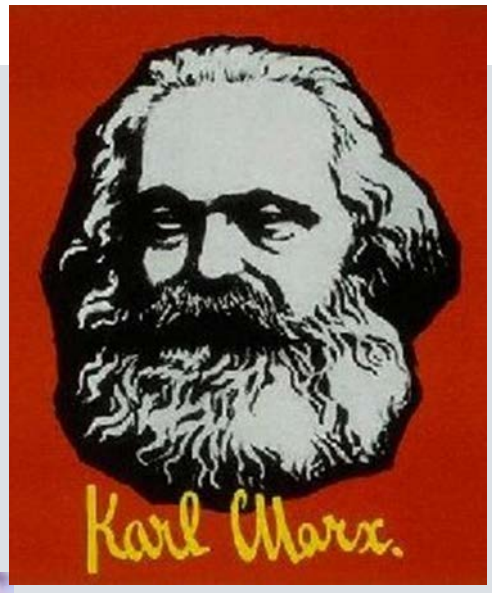
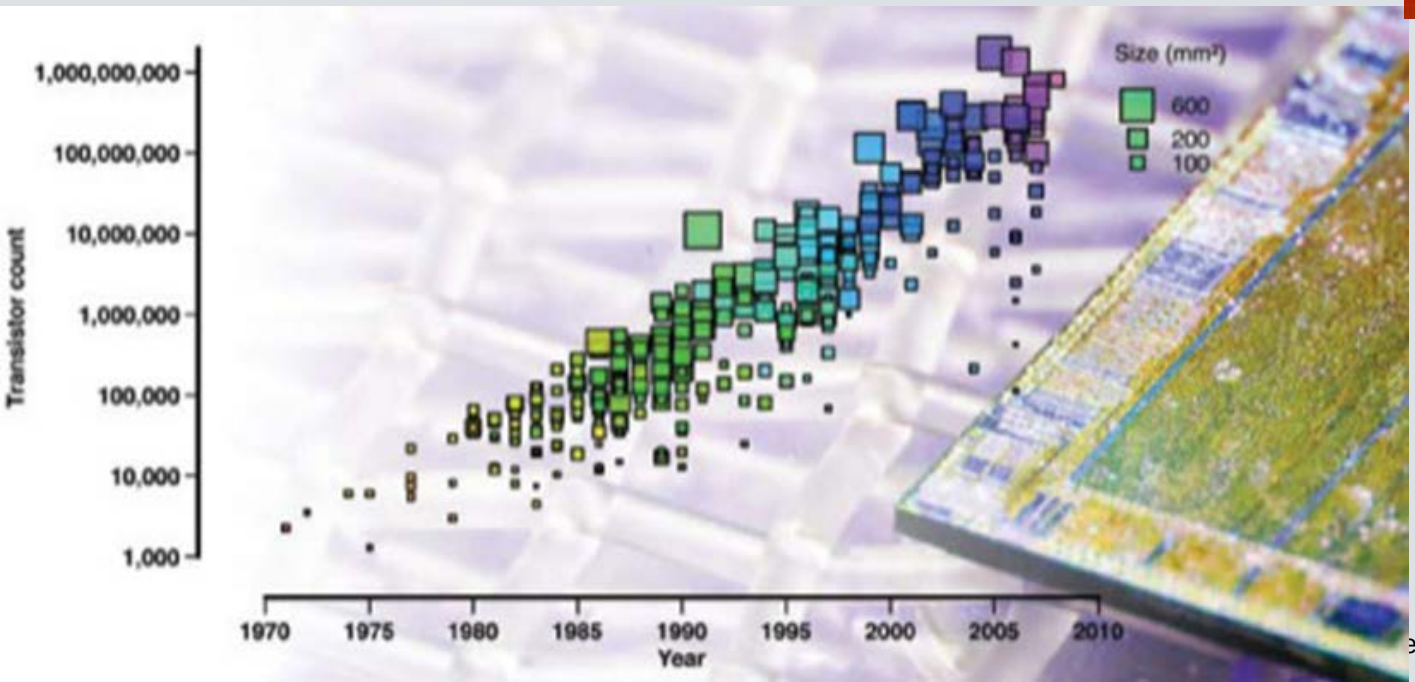


- „Das Sein bestimmt das Bewusstsein.“
- Moore‘s law describes the technical essence of our time
- Progammable logic, analogue, power
- The logical conclusion: **A *soft* EGSE**



Platform of platforms

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- Reconfigurable platform ProUST for scalable power protection
- Reconfigurable platform ProUST-FE for discrete and serial interfaces
- Reconfigurable platform ProUST-CSAS for bidirectional power

Green „Chameleon SCOE“

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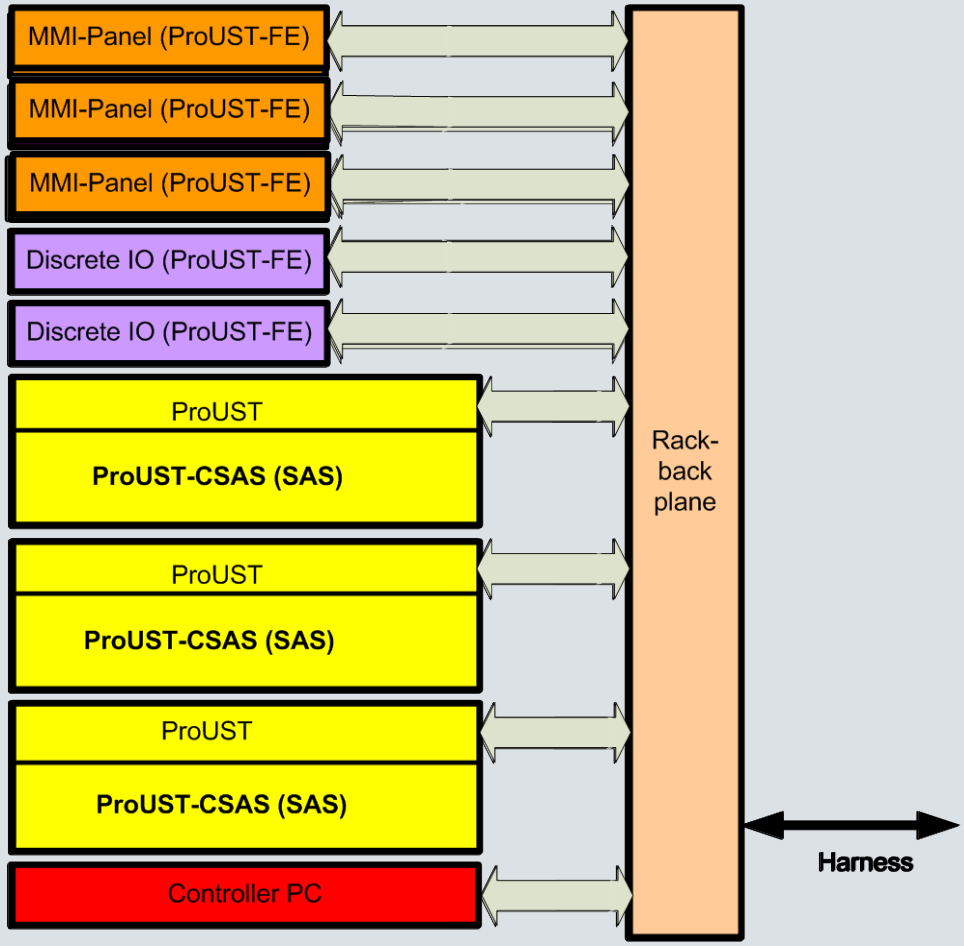
- Transform EGSE as you like



Rack-level PCB platform

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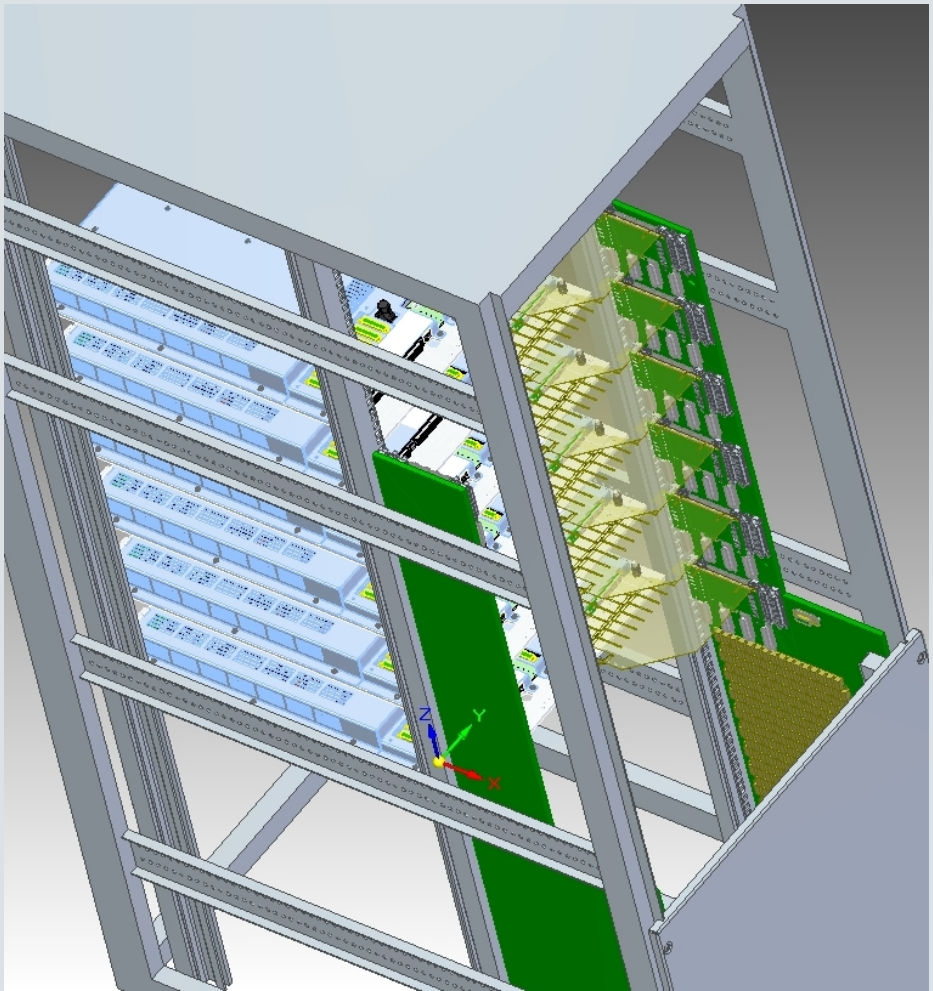
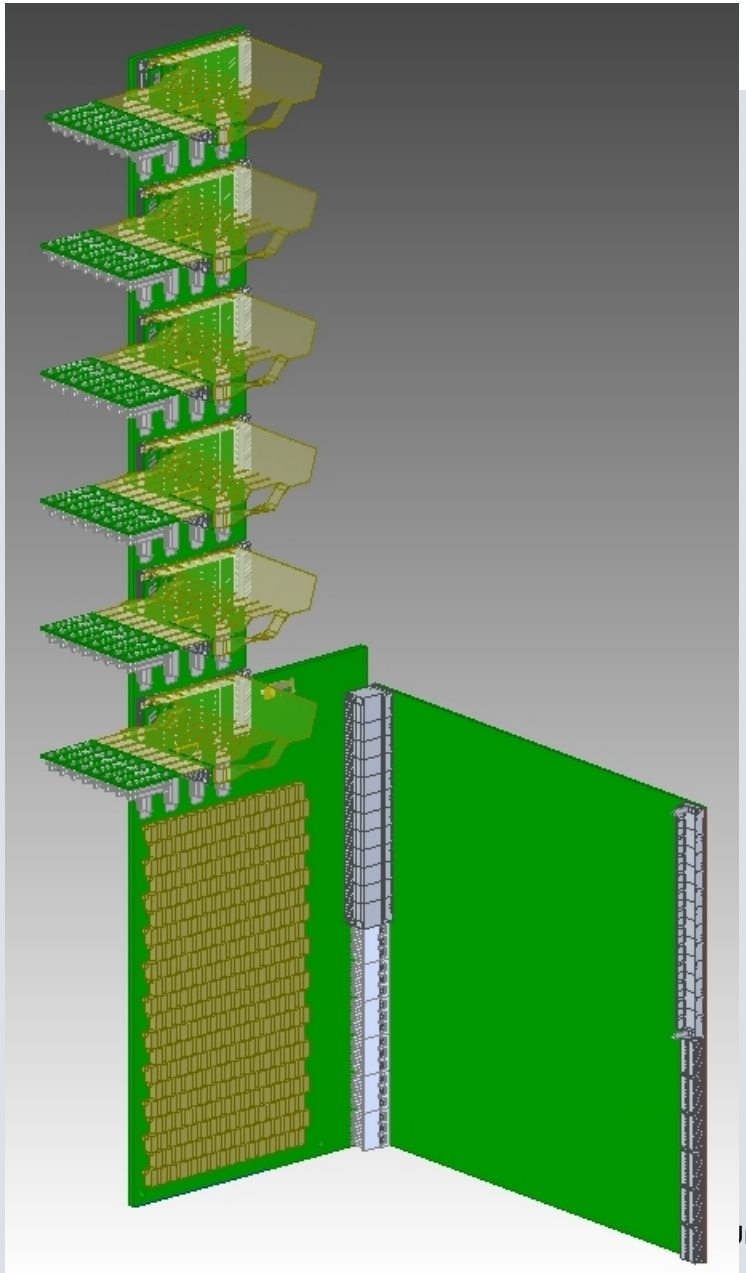
- High-density XXL-Power-PCBs





Rack-level PCB platform

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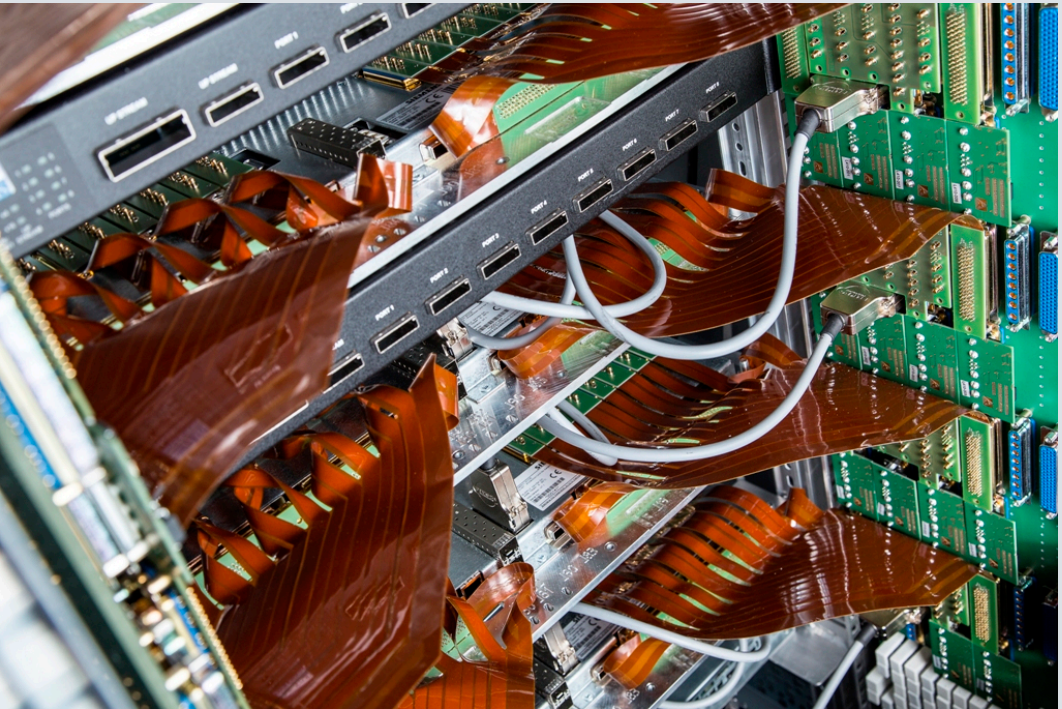
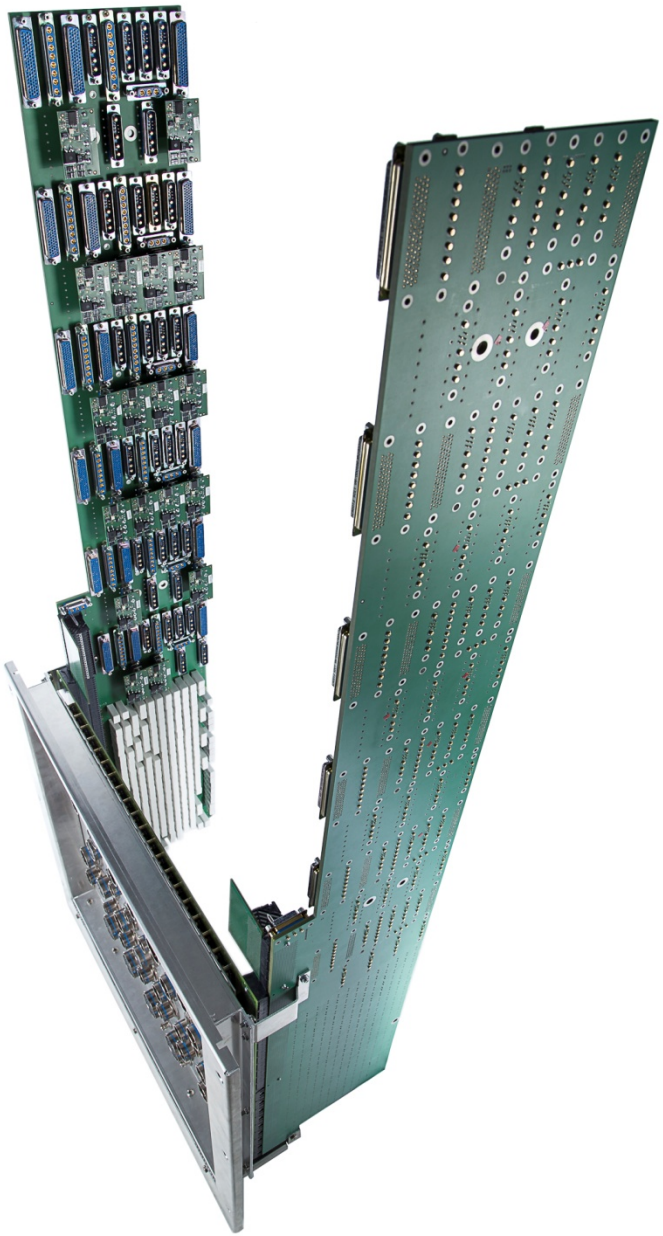
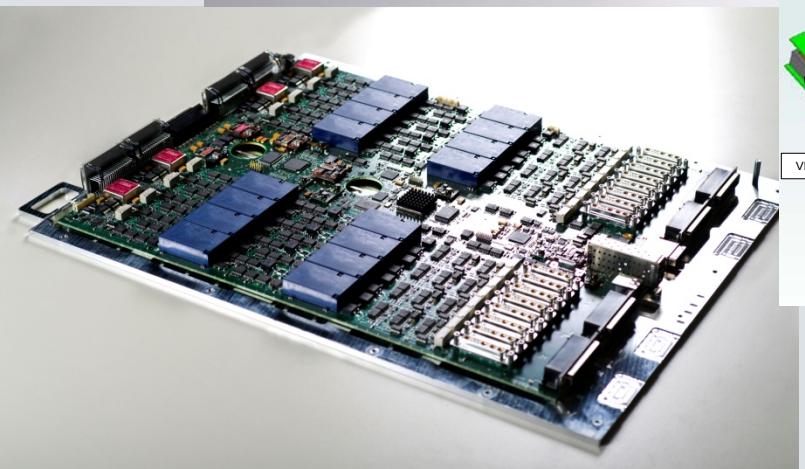
- Rack-level wiring solution incl. power
- „Sideplane“ thermally optimal
- Flex-PCB

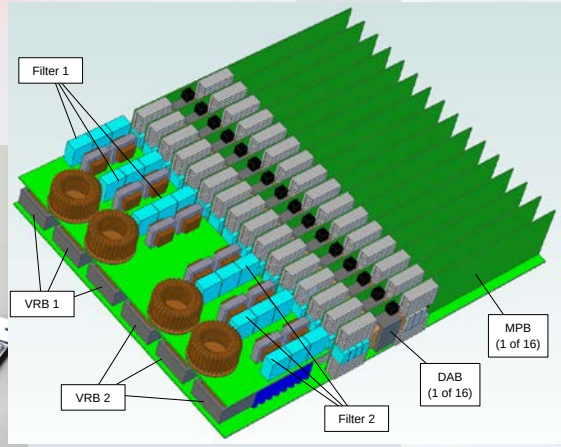




Roadmap

- ProUST-FE is a platform within a platform (w





Thank you for your Attention!

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