Contribution ID: **1** Type: **not specified**

Timing Properties of the LEON3-based GR712RC Board. Implications on Task Scheduling

Wednesday, 11 December 2013 10:30 (50 minutes)

Actitvity: Laboratory (R&D)
TO: Marco Zulianello/Software Systems Division

Multicore processors have been considered as an effective solution to cope with the increasingly performance requirements of Critical Real-Time Embedded (CRTE) systems, like those used in space, aerospace, automotive and railway domains. Multicores enable consolidating several functions on the same chip reducing overall system SWaP costs. It is also the case that multicore chips challenge providing timing guarantees on the execution of applications, which, in turn, challenges the timing validation and verification of the whole system. In the space domain we observe a clear trend towards multicores with LEON3 multicore-based chips such as the GR712RC and LEON4 multicore-based boards such as the NGMP. In this presentation I will cover time predictability and time composability properties of the GR712RC and compare it with the NGMP (ML510 board). In particular I'll cover the work of this activity has done on covering how inter-task conflicts in the access to hardware shared resources, such on-chip buses or shared caches, affect applications timing behaviour. As part of this activity, special emphasis has been also been put on understanding how inter-task conflicts at chip level affect both timing analysis and schedulability of applications on multicores.

Presenter: Mr J. CAZORLA, Francisco (Barcelona Supercomputing Center)